Wavelet Energy-based Mahalanobis Distance Metric for Testing Analog and Mixed-Signal Circuits

Alexios D. Spyronasios, Michael G. Dimopoulos, *Member, IEEE*, and Alkis A. Hatzopoulos, *Senior Member, IEEE*

***Abstract*—In this paper a test method based on the wavelet transformation of the measured signal, be it supply current (I_{PS}) or output voltage (V_{OUT}) waveform, is presented. In the wavelet analysis, a *Mahalanobis* distance test metric is introduced utilizing information from the wavelet energies of the first decomposition level of the measured signal. The tolerance limit for the good circuit is set by statistical processing data obtained from the fault-free circuit. Simulation comparative results on benchmark circuits for testing both hard faults and parametric faults are presented showing the effectiveness of the proposed testing scheme.**

***Index Terms*—Analog and Mixed-Signal Testing, Circuit Test, Wavelets, Mahalanobis Distance.**

I. Introduction

TESTING of analog and mixed-signal circuits is long-lasting active and attractive research topic basically due to the difficulties inherent to the nature of analog signals [1]. Apart from the output voltage measuring based techniques, supply current testing techniques have been investigated for several years and various approaches have been proposed [2]-[6]. Both techniques can be easily implemented, since they incorporate a single measurement on the circuit under test (CUT). For the measured signal processing different approaches have been proposed, like RMS value calculation, Fast Fourier Transform (FFT), amplitude and phase, correlation functions and others. The exploitation of the wavelet transform, which resolves a signal in both time and frequency simultaneously has also been investigated [7]-[9]. In [4] the authors use the wavelet transform as a preprocessing step of a more complex test methodology. In [8] the presented test method is based on an Euclidean test metric applied to I_{PS} current waveforms and no systematic way for computing the tolerance limits is presented. Also the results are for hard faults. In [9] the authors present a comparative sensitivity analysis between the wavelet and Fourier transforms. Wavelet transform gives a better approximation of a transient current waveform than the Fourier transform for a certain limiting high frequency of the signal, which is already imposed by the measurement setup in practical situations.

In this paper, a fault detection method based on the wavelet analysis of the measured waveform (I_{PS} or V_{OUT}) is proposed. The metric that is used in the test method is based on the Mahalanobis distance [10],[11]. Information from the two wavelet energies of the first wavelet decomposition level of the measured signal provides the necessary information for the Mahalanobis distance computation. Also, a systematic way of selecting the tolerance limits exploiting statistical data from fault-free circuits is developed. Simulation results are given for testing parametric and hard circuit faults.

In the following, a brief introduction to wavelets is outlined in section II. An explanation of the Mahalanobis distance is given in section III. The proposed test method is described in section IV. Experimental results are presented in section V. Discussions and directions for further work in section VI are concluding the paper.

II. Introduction to Wavelets

The wavelet transform [12]-[14] is a transform that provides both time and frequency representation. The wavelet transform of a time-domain signal results in portions of the signal, either high frequency or low frequency, being filtered out though a procedure called decomposition. The decomposition procedure is repeated until a predefined decomposition level producing a set of signals which actually represent the original signal.

The continuous wavelet transform (CWT) of a function $x(t)$ is defined as follows:

$$CWT_{\psi}^{\chi}(\tau,s)=\Psi_{\psi}^{\chi}(\tau,s)=\frac{1}{\sqrt{|s|}}\int_{-\infty}^{\infty}x(t)\psi^{*}(\frac{t-\tau}{s})dt \qquad (1)$$

The transformed signal is a function of two variables, τ which represents the time shift (translation) and s which represents the amount of time scaling or dilation. $\Psi(t)$ is called the mother wavelet and it is the transforming function (a prototype) for generating the other window functions. An

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Alexios D. Spyronasios, and Alkis A. Hatzopoulos are with the Dept. of Electrical and Computer Eng., Electronics Lab., Aristotle University of Thessaloniki, Thessaloniki 54124, GREECE (e-mail: aspyrona@ee.auth.gr, niikos@ee.auth.gr, alkis@eng.auth.gr).

Michael G. Dimopoulos is with the Department of Electronics, Alexander Technological Educational Institute of Thessaloniki, Thessaloniki, P.O. BOX 141, 57400, GREECE (corresponding author to provide phone: +306972645452; e-mail: mdimop@ieee.org).

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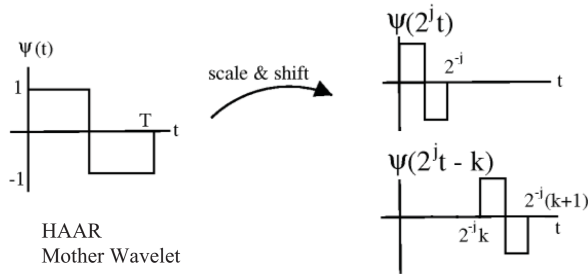


Figure 1. HAAR Mother Wavelet function

example of a mother wavelet, the Haar wavelet is shown in Fig. 1. Haar wavelet [12]-[14] is a step function taking values 1 and -1, on [0, 1/2) and [1/2, 1), respectively.

For sampled signals (as in our case) the *Discrete Wavelet Transform* (DWT) is used. The main idea remains the same as with the CWT. Here, the Haar transform [12]-[14] decomposes a discrete signal into two subsignals of half its length. One subsignal is a running average or trend; the other subsignal is a running difference or fluctuation.

In the wavelet analysis, two energy values are computed E_{T1}, and E_{F1}. For the computation of E_{Ti} (i=1,2,3,…), the trend coefficients T_{ij} of the i decomposition level (see equation 2) are considered:

$$E_{Ti} = \sum_{j=1}^{n} T_{ij}^{2} \quad (2)$$

and for E_{F1} the fluctuation or detail coefficients of the first decomposition level are taken into account:

$$E_{F1} = \sum_{j=1}^{n} F_{1j}^{2} \quad (3)$$

III. The mahalanobis Distance

Suppose we have two groups (fault-free and faulty circuits). Consider a number of relevant characteristics (say p) of individuals in these groups. We let X denote a (random) vector that contains the measurements made on a given individual or entity under study. Often in practice we are interested in measuring and then summarizing the differences between groups. A common assumption is to take the p-dimensional random vector X as having the same variation about its mean within either group. Then the difference between the groups can be considered in terms of the difference between the mean vectors of X in each group relative to the common within-group variation. A measure of this type is the Mahalanobis distance. The statistical distance or Mahalanobis distance [10], [11], [15] between two points $x = (x_1,...,x_p)^t$ and $y = (y_1,...,y_p)^t$ in the p-dimensional space R^p is defined as:

$$MD_{xy} = \sqrt{(x-y)\cdot S_{x,y}^{-1}\cdot (x-y)^{T}} \quad (4)$$

where $S_{x,y}^{-1}$ is the inverse of the covariance matrix between x and y. Here, we are interested in the distance of an observation x (CUT observation) from the center y of a set (cluster) of points namely the fault-free cluster (fault-free or reference circuit). The Mahalanobis distance is used since we want to take into account the correlation between variables when computing statistical distances. The Mahalanobis distance has the effect of transforming the variables to uncorrelated standardized variables Y and computing the Euclidean distance between the mean vectors of Y.

The Mahalanobis distance is therefore a weighted Euclidean distance where the weighting is determined by the range of variability of the sample point x; expressed by the covariance matrix.

IV. Proposed Test Method

In the test method a Mahalanobis distance test metric is introduced which uses the energy values [12]-[14] E_{T1} and E_{F1} of the wavelet transform of the measured waveform (I_{PS}, V_{OUT}). For the wavelet energy computation, the trend and detail coefficients of the first level decomposition are considered. Since generally we are dealing with measurements on many known fault-free circuits with variations on parameter values, the notion of the nominal circuit is replaced by the notion of the reference circuit. The value of a parameter of the nominal circuit is substituted by the mean of the values of all fault-free circuit instances in the reference circuit.

The proposed test method is a two phase process. At the first phase (*Initial Phase*), statistical processing of the fault-free circuit data takes place in order to compute the wavelet energy values E_{T1} and E_{F1} for the reference circuit and the tolerance limits $MD_{T1,0}^{\lim}$ and $MD_{F1,0}^{\lim}$. In the second phase (*Main Test Phase*) the Mahalanobis distances $MD_{T1,t}$ and $MD_{F1,t}$ for the t CUT are computed and compared with the corresponding tolerance limits of the reference circuit. A faulty circuit instance t will be successfully detected when either of its Mahalanobis distance values exceeds the corresponding reference tolerances.

The algorithm phases are described in the following:

Initial Phase: Multiple measurements for a number N of known fault-free circuits are performed only in this phase.

For fault-free circuit i (i=1,…,N) do **begin**

1) Measure the waveform z={I_{PS}, V_{OUT}}.
2) Compute and store $E_{T1,0-i}(z)$: the energy value from the trend coefficients of the first decomposition level,
3) Compute and store $E_{F1,0-i}(z)$: the energy value from the detail coefficients of the first decomposition level.

end

4) Compute $E_{T1,0}(z)$: the energy value from the trend coefficients of the first decomposition level for the reference circuit (the mean value of all $E_{T1,0-i}(z)$ values).
5) Compute $E_{F1,0}(z)$: the energy value from the detail coefficients of the first decomposition level for the reference circuit (the mean value of all $E_{F1,0-i}(z)$ values).

For fault-free circuit i (i=1,…,N) do **begin**

6) Compute the Mahalanobis distance $MD_{T1,0-i}(z)$ from the $E_{T1,0-i}(z)$ energy:

$MD_{T1,0-i}(z) =$

$$\sqrt{(E_{T1,0-i}(z) - E_{T1,0}(z)) \cdot S^{-1}_{0-i,T1-0} \cdot (E_{T1,0-i}(z) - E_{T1,0}(z))^T}$$

($S^{-1}_{0-i,T1-0}$ is the inverse covariance matrix between the i energy value ($E_{T1,0-i}(z)$) and the center of $E_{T1,0}(z)$).

7) Compute the Mahalanobis distance $MD_{F1,0-i}(z)$ from the $E_{F1,0-i}(z)$ energy:

$MD_{F1,0-i}(z) =$

$$\sqrt{(E_{F1,0-i}(z) - E_{F1,0}(z)) \cdot S^{-1}_{0-i,F1-0} \cdot (E_{F1,0-i}(z) - E_{F1,0}(z))^T}$$

($S^{-1}_{0-i,F1-0}$ is the inverse covariance matrix between the i energy value ($E_{F1,0-i}(z)$) and the center of $E_{F1,0}(z)$).

end

8) Compute the Mahalanobis distance limits $MD^{\lim}_{T1,0}(z)$ and $MD^{\lim}_{F1,0}(z)$

Main Test Phase:

for CUT *t* (*t*=1,..,*num*) do **begin**

9) Measure the waveform z={I_{PS}, V_{OUT}}.

for *z*={I_{PS}, V_{OUT}} do **begin**

10) Compute $E_{T1,t}(z), E_{F1,t}(z)$.

11) Compute the Mahalanobis distance $MD_{T1,t}(z)$:

$MD_{T1,t}(z) =$

$$\sqrt{(E_{T1,t}(z) - E_{T1,0}(z)) \cdot S^{-1}_{t,T1-0} \cdot (E_{T1,t}(z) - E_{T1,0}(z))^T}$$

12) **if** $MD_{T1,t}(z) > MD^{\lim}_{T1,0}(z)$)

then declare as faulty the *t* CUT.

else begin

13) Compute the Mahalanobis distance $MD_{F1,t}(z)$:

$MD_{F1,t}(z) =$

$$\sqrt{(E_{F1,t}(z) - E_{F1,0}(z)) \cdot S^{-1}_{t,F1-0} \cdot (E_{F1,t}(z) - E_{F1,0}(z))^T}$$

14) **if** $MD_{F1,t}(z) > MD^{\lim}_{F1,0}(z)$

then declare as faulty the *t* CUT.

else the *t* CUT is declared fault-free.

end

end

end

Generally, selection of the tolerance limits for the reference circuit has a strong effect on the circuit's fault detectability resulting in faulty circuits under test (CUTs) that escape detection and fault-free CUTs being erroneously considered as faulty. The first case results in a lower fault detectability of the test method used and the second case results in a number of fault-free CUTs being discarded as faulty. The term "Fault-free CUT losses" is used throughout this paper to characterize the discarded fault-free CUTs. Here we propose that the tolerance limits should be chosen by selecting the percentage of the *fault-free CUT losses*. So, when a selected tolerance limit turns out in *a*% *fault-free CUT losses* this means that from a lot of 100 fault-free CUTs, (100-*a*) pass the test process, whereas *a* fault-free CUTs are encountered as faulty.

The tolerance limit $MD^{\lim}_{T1,0}(z)$ ($MD^{\lim}_{F1,0}(z)$) at step 8 of initial phase is computed from the cumulative probability distribution $cpdf_{MD_{T1,0}}(z)$ ($cpdf_{MD_{F1,0}}(z)$) of $MD_{T1,0-i}(z)$ ($MD_{F1,0-i}(z)$) values and considering in each case an *empirical cpdf*. For a sufficiently large sample size the *empirical cpdf* will approach the true *cpdf*. For example, for the $cpdf_{MD_{T1,0}}(z)$ distribution, if the *i observed value* (x_i= $MD_{T1,0-i}(z)$) is selected, then $MD^{\lim}_{T1,0}(z)$= $MD_{T1,0-i}(z)$ and the percentage of *fault free CUT losses* is equal to the value [1- $cpdf_{MD_{T1,0}}(z)\Big|_{MD_{T1,0-i}(z)}$]·100%. Similar analysis to the above is applied for the computation of limit $MD^{\lim}_{F1,0}(z)$.

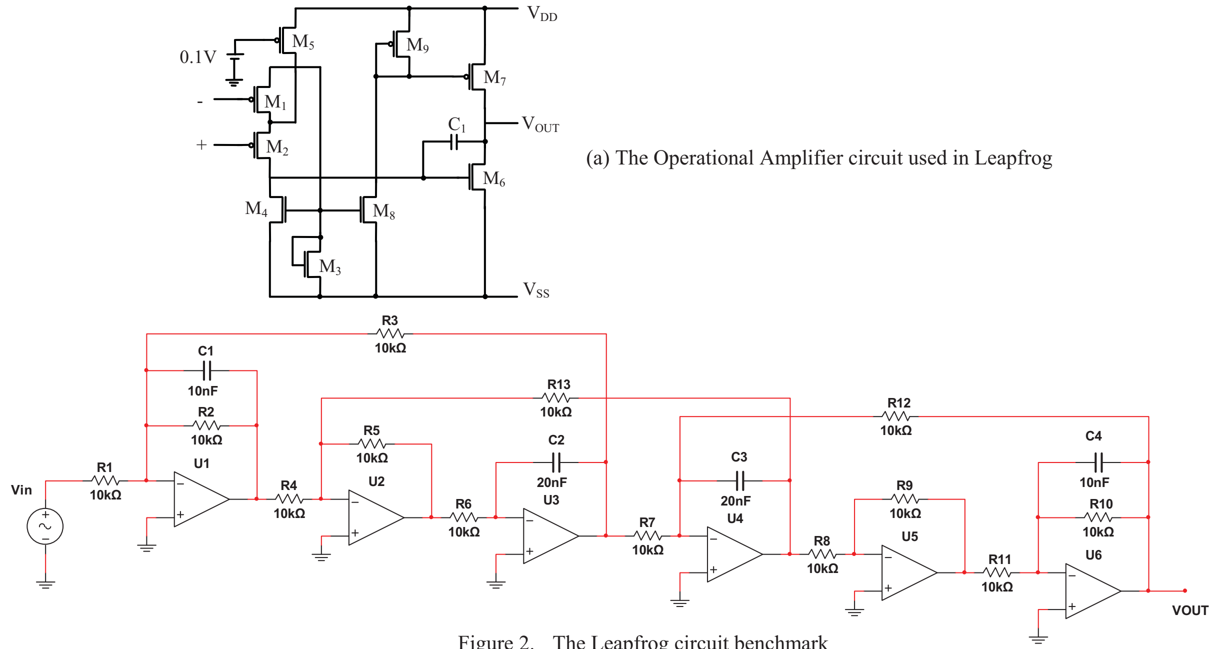
A value of 1% *fault-free CUT losses* is selected in the experiments and this gives the appropriate tolerance limit values for $MD^{\lim}_{T1,0}(z)$ and $MD^{\lim}_{F1,0}(z)$.

Although, in the experimental results that follow, the Haar mother function is used in the wavelet analysis, various other mother functions have also been tried without any appreciable difference in the presented results.

V. Simulation Results

The test method of section IV is has been implemented in C++ and has been applied for testing various circuits, two of which, a leapfrog circuit, and an elliptical filter circuit are presented here. Both circuits have been selected from a proposed suite of benchmark circuits [16]. Simulations have been performed using the *HSPICE* circuit Simulator. The HSPICE netlists for the circuits have been scaled down to 350nm AMS technology from the original description of the benchmarks in Mitel Semiconductor's 1.2u technology [16]. The single fault model is considered.

Opens are implemented by a resistor of 100 MEG Ohm and shorts by a resistor of 1 Ohm. The σ value (with σ being the standard deviation) of component variation is determined in such a way that the component is allowed to vary up to 3σ, yet the analog circuit will meet its specification.



(a) The Operational Amplifier circuit used in Leapfrog

Figure 2. The Leapfrog circuit benchmark

In parametric fault analysis, V_{tn} (threshold voltage for NMOS transistors), V_{tp} (threshold voltage for PMOS transistors) and internal to operational amplifier passive components variations are taken into account. Also, variations to passive circuit components (outside the operational amplifier) are considered. Faulty parameters are allowed $\pm 6\sigma$ variation for the high and low parametric fault values. A total of 20000 parametric faulty cases are taken.

The first circuit under test, leapfrog filter circuit, is depicted in Fig. 2. It consists of 6 bipolar-supply operational amplifiers (opamps), 4 capacitors and 13 resistors. Each operational amplifier consists of 9 MOS transistors and a capacitor.

All hard faults (shorts and opens) on passive components are taken into account thus giving 51 faulty cases. For each opamp, are also considered internal hard faults; alls opens and shorts in MOS transistors (Gate-Open (GOP), Drain Open (DOP), Source-Open (SOP), Gate-Drain short (GDS), Gate-Source short (GSS), Drain-Source short (DSS)) and shorts and opens for the internal capacitor C_1. Thus a total of 57 faults per opamp are added to the examined fault set.

The total set of faults consists of (6x57)+51=393 hard faults (opens and shorts) and 20000 parametric faults. A low-frequency sinusoidal input of 700 Hz with an amplitude of 3V is applied to input V_{in}. The tolerance limits for the good circuit are obtained from a set of 10000 Monte Carlo simulations. For all fault-free circuits, the I_{PS} (I_{VDD} and I_{VSS}) and V_{OUT} waveforms are stored and the test method of section III is applied.

The wavelet energy values using the trend ($E_{T1,0}$) and detail ($E_{F1,0}$) coefficients, respectively, for the good circuit case and the Mahalanobis distances $MD_{T1,0}$ and $MD_{F1,0}$ are computed (*Initial Phase* of section III). Next the energy values $E_{T1,t}$, and $E_{F1,t}$ and the discrimination factor Df^{t} for the faulty circuits are computed (*main test Phase* of section III). Afterwards the Mahalanobis distances $MD_{T1,t}$ and $MD_{F1,t}$ are computed and compared with the corresponding values for the fault-free circuit (*main test Phase* of section IV).

Indicative results for three hard circuit faults namely *Opamp2_M1-DSS*, *C4-Open* and *Opamp2_M1_SOP* are shown in Table I. In this Table are presented for each fault the $MD_{T1,t}(z)$ (z={I_{VDD}, I_{VSS}, V_{OUT}}) distances. The tolerance limits for the fault-free circuit instance are:

$MD_{T1,0}^{\lim}(I_{VDD}) = 0.17474$, $MD_{T1,0}^{\lim}(I_{VSS}) = 0.10533$ and $MD_{T1,0}^{\lim}(V_{OUT}) = 0.28521$. It is observed that according to step 14 of main test phase on section IV, the *Opamp2_M1-DSS* fault is not detectable using the negative supply current I_{VSS} ($MD_{T1,t}(I_{VSS}) = 0.06671 < 0.10533 = MD_{T1,0}^{\lim}(I_{VSS})$) while it can be detected using the positive supply current I_{VDD} and the V_{OUT} signal. The *C4-Open* fault is detectable using either one of the I_{VDD} or I_{VSS} signals but fails detection when the V_{OUT} signal is used. Finally, for the *Opamp2_M1-SOP* fault we have that it is detectable in every case.

TABLE I. DATA FOR INDICATIVE HARD CIRCUIT FAULTS

Fault type	$MD_{T1,t}(I_{VDD})$	$MD_{T1,t}(I_{VSS})$	$MD_{T1,t}(V_{OUT})$
Opamp2_M1-DSS	80.97470	0.06671	80.40674
C4-Open	13.13357	2.02336	0.00157
Opamp2_M1-SOP	1.059217	0.97447	84.56835

Results regarding the detectability of hard faults are presented in Table II. In this table, row 'T1' corresponds to results obtained from $MD_{T1,t}(z)$ alone (step 12 of main test phase in section IV), row 'F1' has results from $MD_{F1,t}(z)$ alone (step 14 of main test phase in section IV) and row 'Total' the total cumulative results from $MD_{T1,t}(z)$ and $MD_{F1,t}(z)$. Columns 'V_{OUT}', 'I_{VDD}', 'I_{VSS}' correspond to the detectability percentage contribution of V_{OUT}, I_{VDD}, I_{VSS}, signals respectively. Column 'I_{VDD}/I_{VSS}' presents results where the Mahalanobis distance is computed by considering both I_{VDD} and I_{VSS} datasets.

From Table II we see that the proposed test method succeeds in detecting all hard faults for the cases of I_{VDD}, I_{VSS} and 70.99% of faults when the V_{OUT} signal is utilized. Another observation is the fact that the combination of I_{VDD} and I_{VSS} signals results in higher fault detectability percentage when compared to V_{OUT}, I_{VSS} and I_{VDD} (for the T1 case) signals.

Results concerning the efficiency of the proposed method in testing parametric faults are presented in Table III. From Table III it is seen that the proposed test method succeeds in detecting all parametric faults for the cases of I_{VDD}, I_{VSS} and only 12.83% of faults when the V_{OUT} signal is utilized. Again it is seen that the combination of I_{VDD} and I_{VSS} signals results in higher fault detectability percentage when compared to V_{OUT}, I_{VSS} (F1 case) and I_{VDD} (F1 case) signals. It must be noted also the low fault coverage of V_{OUT} signal (only 12.83% in total) with respect to the one obtained by the I_{PS} signal (either I_{VDD} or I_{VSS}) which is over 99% (100% in total).

The second circuit under test is the elliptical filter circuit of Fig. 3. It consists of 3 bipolar-supply operational amplifiers (opamps), 7 capacitors and 15 resistors. Each operational amplifier consists of 9 MOS transistors and a capacitor.

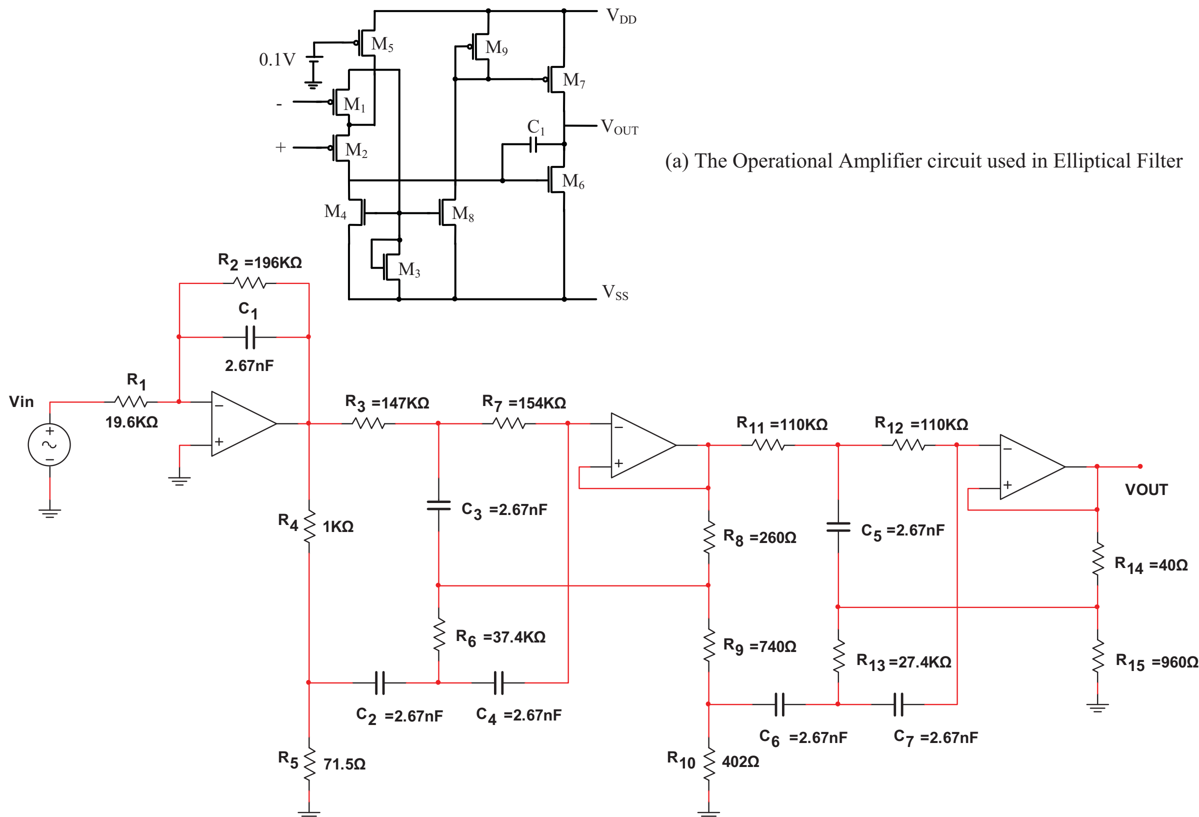
All hard faults (shorts and opens) on passive components are taken into account thus giving 44 faulty cases. For each opamp, are also considered internal hard faults; alls opens and shorts in MOS transistors (Gate-Open (GOP), Drain Open (DOP), Source-Open (SOP), Gate-Drain short (GDS), Gate-Source short (GSS), Drain-Source short (DSS)) and shorts and opens for the internal capacitor C_1. Thus a total of 57 faults per opamp are added to the examined fault set.

TABLE II. DATA FOR HARD FAULTS FOR LEAPFROG FILTER

	V_{OUT} (%)	I_{VDD} (%)	I_{VSS} (%)	I_{VDD}/I_{VSS} (%)
T1	70.99	65.9	63.35	98.72
F1	66.41	100	95.42	100
Total	70.99	100	100	100

TABLE III. DATA FOR PARAMETRIC FAULTS FOR LEAPFROG FILTER

	V_{OUT} (%)	I_{VDD} (%)	I_{VSS} (%)	I_{VDD}/I_{VSS} (%)
T1	9.83	99.86	99.85	98.19
F1	12.21	99.99	96.06	100
Total	12.83	100	100	100



(a) The Operational Amplifier circuit used in Elliptical Filter

Figure 3. The Elliptical Filter circuit benchmark

The total set of faults consists of (3x57)+44=215 hard faults (opens and shorts) and 20000 parametric faults. A low-frequency sinusoidal input of 700 Hz with an amplitude of 2V is applied to input V_{in}. The tolerance limits for the good circuit are obtained from a set of 10000 Monte Carlo simulations. For all fault-free circuits, the I_{PS} (I_{VDD} and I_{VSS}) and V_{OUT} waveforms are stored and the test method of section III is applied.

Results regarding the detectability of hard faults are presented in Table IV. From this table we see that the proposed test method succeeds in detecting all hard faults for the cases of I_{VDD}, I_{VSS} and 70.56% (for T1) of faults when the V_{OUT} signal is utilized.

Results concerning the efficiency of the proposed method in testing parametric faults are presented in Table V. As it is seen, the proposed test method succeeds in detecting all parametric faults for the cases of I_{VDD}, I_{VSS} and only 43.02% (for T1) of faults when the V_{OUT} signal is utilized. Again it is seen that the combination of I_{VDD} and I_{VSS} signals results in higher fault detectability percentage when compared to V_{OUT} signals. It must be noted also the low fault coverage of V_{OUT} signal (only 43.02% in total) with respect to the one obtained by the I_{PS} signal (either I_{VDD} or I_{VSS}) which is 100% in total.

VI. Conclusions and Further Work

In this work, the wavelet transformation of the measured I_{PS} current and output voltage V_{OUT} waveforms for mixed-signal circuit test is studied. Also, a test metric based on the Mahalanobis distance is introduced based on wavelet energies that exploit info from the first wavelet decomposition level for both the trend and detail coefficients. The tolerance limits for the reference (good) circuit whose selection plays important role in test detectability are carefully chosen from the distribution of Mahalanobis distances of fault-free circuits.

Simulation results from the application of the proposed method for testing two circuits from the suite of ITC'97 analog and mixed signal benchmarks are presented. Both, I_{PS} and V_{OUT} waveforms are utilized to examine the efficiency of the test method. HSPICE simulation results are presented, where the proposed wavelet-based test method attains high fault coverage for both hard and parametric circuit faults.

Work is under way to examine the efficiency of the proposed test method on other fault models, explore other test metrics and apply the presented method for testing other complex mixed-signal circuits.

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TABLE IV. Data for hard faults for elliptical Filter

	V_{OUT} (%)	I_{VDD} (%)	I_{VSS} (%)	I_{VDD}/I_{VSS} (%)
T1	70.56	100	100	100
F1	95.79	100	100	100
Total	100	100	100	100

TABLE V. Data for parametric faults for elliptical Filter

	V_{OUT} (%)	I_{VDD} (%)	I_{VSS} (%)	I_{VDD}/I_{VSS} (%)
T1	43.02	100	100	100
F1	91.39	100	100	100
Total	100	100	100	100

Alexios D. Spyronasios was born in Ioannina, Greece in 1983. He received the Diploma in Electrical and Computer Engineering from the Aristotle University of Thessaloniki in 2006 and is currently working towards the PhD degree at Electrical and Computer Engineering department of Aristotle University of Thessaloniki.

His special fields of interest include integrated-inductor modeling in RF frequencies and design and fault diagnosis of integrated circuits and systems.

Michael G. Dimopoulos (M'04) was born in Kastoria, Greece. He received the B.Sc. degree in Physics, the Master's degree in Electronics, and the Ph.D. degree in Informatics from Aristotle University of Thessaloniki, Thessaloniki, Greece, in 1993, 1996, and 2004, respectively. From 2004 to 2010, he was an Adjunct Lecturer with the Department of Informatics, Aristotle University of Thessaloniki, teaching courses on digital systems, digital circuit design, and advanced digital design and test. From 2006 to 2007, he was a Project Manager with Olympia Electronics S.A. Research and Development Department. From 2008 he is an Adjunct Assistant Professor with the Department of Electronics, Alexander Technological Educational Institute of Thessaloniki, Thessaloniki, Greece.

His research interests include the design and fault diagnosis of integrated circuits and systems (analog, digital, mixed-signal and radio frequency), development of computer-aided design tools for very large scale integration, and design and test of embedded and reconfigurable systems. He is the author or co-author of more than 30 scientific papers in international journals and conference proceedings. He serves as member of the editorial board of SIMULATION MODELING PRACTICE AND THEORY (SIMPAT) journal.

Dr. Dimopoulos is a member of the Greek Physics Society, the Association for Computing Machinery (ACM), the IEEE Solid State Circuits Society and the IEEE Computer Society.

Alkis A. Hatzopoulos was born in Thessaloniki, Greece. He received his Degree in Physics (with honours), his Master Degree in Electronics and his Ph.D. Degree in Electrical Engineering from the Aristotle University of Thessaloniki, Greece, in 1980, 1983 and 1989 respectively.

He was a research associate in the Department of Electrical and Computer Engineering at the Aristotle University of Thessaloniki for seven years and in 1989 he was elected as a Lecturer. Since Feb. 2010 he has been elected as an Professor at the same Department and also as the Director of the Electronics Laboratory.

Dr. Hatzopoulos is a member of the Greek Physics Society and the Greek Computer Society. He is also a senior member of IEEE. He is actively involved in educational and research projects and he is the author or co-author of more than 100 scientific papers in international journals and conference proceedings. His research interests include: design and fault diagnosis of integrated circuits and systems (analog, mixed-signal, RF), electronic communication circuits, instrumentation electronics.