Design of a 3rd Order 1.5-bit Continuous-Time (CT) Sigma-Delta (ΣΔ) Modulator Optimized for Class D Audio Power Amplifier

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***Abstract*—This paper presents a 3rd order 1.5-bit ΣΔ modulator with distributed feedback and local resonator feedback for a Class D audio amplifier. In order to improve the signal-to-noise-and-distortion ratio (SNDR), without increasing the oversampling ratio (OSR) or the order of the modulator, the modulator uses transmission zeros and 1.5-bit quantization. High level simulations of the modulator architecture show that it has a maximum SNDR value of 81 dB, for a signal bandwidth of 18 kHz and a sampling frequency of 1.2 MHz. An electrical circuit is designed to implement the proposed architecture and the electrical simulations show that it has a maximum SNDR value of 76.1 dB. The influence of the constituting blocks of the circuit in the performance of the modulator is investigated using electrical simulations.**

***Index Terms*—Continuous-Time (CT) Sigma-Delta (ΣΔ), Class D amplifier, Audio.**

I. Introduction

DUE to the major concerns of global sustainability, there is a growing need for energy saving. The energy efficiency of audio amplifiers can be an important contribution to this end.

The traditional Class AB continuous-time power amplifiers have a maximum theoretical efficiency of 78.5% [1] while Class D amplifiers can approach 100% in theory. The efficiency advantage of the Class D amplifiers is irrefutable and, through this trait, switching-amplifier topologies have earned much of their market share. The basic idea of a Class D amplifier is that the devices of the output stage work as switches, therefore, under ideal conditions, the power dissipation of the output devices is zero (because when the device is ON its current is large but its voltage is zero). In order for a Class D amplifier to work it is necessary to transform the input analog signal into a digital signal that controls the switching of the output devices.

Sigma-Delta (ΣΔ) modulators are the most suitable A/D converters for low-frequency, high-resolution applications, in view of their inherent linearity, reduced anti-aliasing filtering requirements and robust analog implementation. Moreover, by trading speed for accuracy, ΣΔ modulators allow high performance to be achieved with low sensitivity to analog component imperfections and without requiring component trimming [2].

This paper describes a 3rd order 1.5-bit continuous-time (CT) ΣΔ modulator with distributed feedback and local resonator feedback intended for use in a Class D full-bridge audio power amplifier, in order to obtain a large SNDR value while using a moderately low switching frequency. The use of local resonator feedback in the modulator, allows to implement a Chebyshev type II filter, which results in a large SNDR value even for a low oversampling ratio (OSR) value. The use of 1.5-bit in the quantizer can eliminate some the inherent drawbacks of a binary switching scheme. With this technique, the output stage provides current to load only when needed, and the switching activity of output stage is greatly reduced, especially when input signal has a small amplitude value. These features increase the power efficiency of the amplifier [3].

The paper is organized as follows. Section II gives a general overview of the Class D amplifier. In Section III several architecture options for the modulator will be studied. The Section IV proposes a combination of two architectures studied in Section III in order to improve the SNDR value, without increasing the OSR or the order of the modulator (not greater then 3). Section V explains the steps necessary to design a the circuit implementation of the proposed ΣΔ modulator, as well as electrical simulations results of the modulator circuits. Finally, Section VI concludes the paper.

II. Class D Amplifiers

Typically, a Class D amplifier (Figure 1) consists of two stages. The first stage is a signal processing stage that converts the input audio signal into a two-level (1-bit) signal. This two-level signal represents a Pulse-Width Modulation (PWM) signal or a Pulse-Density Modulation (PDM) signal. The second stage of the amplifier is a power output stage, in which the two-level signal drives the output power MOSFETs (half-bridge or full-bridge).

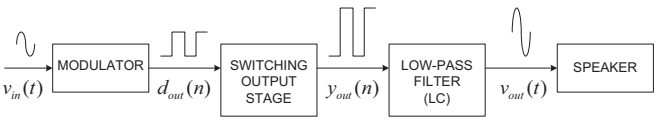

Fig. 1. Class D open-loop-amplifier block diagram.

The Class D amplifier dissipates much less power than the traditional Class A/AB. The output stage devices switches

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between the positive and negative power supplies so as to produce a train of voltage pulses. This waveform reduces the power dissipation of the amplifier, because the output transistors have zero current when not switching, and have low V_{DS} when they are conducting current, thus resulting in a smaller power dissipation $(V_{DS} \times I_{DS})$ in the amplifier. Due to the binary switching of the output devices of the amplifier, therefore the output signal of the amplifier contains high frequency components. These components must be filtered in order to reduce the electromagnetic energy radiated by the amplifier, typically, a LC filter is used for this function.

A. Important Factors in Audio Class D Design

The strongest motivation to use Class D for audio applications is the low power dissipation, but there are important challenges in the design of this type of amplifiers. These include:

- Sound quality
- Modulation techniques
- EMI
- LC filter design
- System cost

B. Modulation Technique

Perhaps the first step in designing a switching amplifier is the choice of the modulation technique.

There are a variety of modulator topologies used in Class D amplifiers, the most basic topology utilizes pulse-width modulation (PWM) with a triangle-wave (or sawtooth) oscillator. However, there are other techniques with a little more complexity such as Pulse Density Modulation (PDM) and Hysteresis switching. In this paper only the fundamental concepts of these techniques will be discussed.

1) Pulse Width Modulation (PWM): PWM is the most common modulation technique. Conceptually, PWM compares the input audio signal to a triangular or ramping waveform with a fixed carrier frequency. This creates a stream of pulses at the carrier frequency. Within each period of the carrier, the duty ratio of the PWM pulse is proportional to the amplitude of the audio signal.

2) Pulse Density Modulation (PDM): A PDM signal can be generated using a $(\Sigma\Delta)$ modulator. The modulator uses a low resolution quantizer (typically 1-bit) to produce a digital signal from the input signal. The filter in the modulator has a high-pass transfer function that removes the quantization noise from the lower frequencies and transfers it to the higher frequencies. The high frequency quantization noise can eliminated by a low pass filter. Sigma-Delta modulators are very well known and are the architecture of choice for A/D converter for audio signals and therefore the design of these type of circuits is very well understood [4].

3) Hysteresis switching: Self-oscillating amplifiers have been developed recently. This type of amplifier always includes a feedback loop, with properties of the loop determining the switching frequency of the modulator, instead of an externally provided clock.

The obvious shortcoming of this circuit is the variability of the switching frequency in function of the power supply voltage. A minor modification is to use the switching waveform itself as the hysteresis feedback. Amplifiers constructed along these lines typically produce fairly respectable performance, accounting for the popularity of this arrangement. This still leaves two rather serious drawbacks. The most important problem is the lack of control over the output filter. The other is that the minimum pulse width produced is only half that of the idle pulse width [5].

C. Output Power Stage

The output stage of the Class D amplifiers are usually implemented using two topologies: half-bridge or full-bridge (depicted in Figure 2) configurations. Each topology has advantages and disadvantages. In brief, a half-bridge is potentially simpler and requires a simpler low pass filter, however the current drawn from the power supplies is signal dependent and therefore a signal replica can appear in the power supply voltages which can cause distortion. In order to reduce this effect it is necessary to filter the signal from the power supply using large decoupling capacitors. The full-bridge topology requires two half-bridge amplifiers and a more complicated output filter. The full-bridge draws a constant current from the power supply and therefore does not introduce the signal in the power supply, which improves the circuit performance and simplifies the design of the power supply circuit.

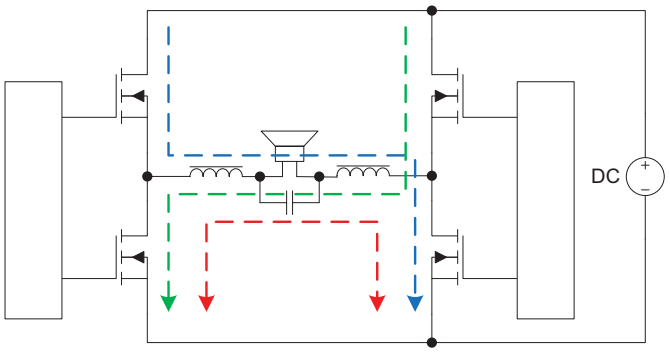

Fig. 2. Differential switching output stage with LC low-pass filter.

D. EMI Considerations

The high-frequency components of the switching signal in a Class D amplifier outputs requires serious consideration. If not properly understood and managed, these components can generate large amounts of electromagnetic interference (EMI) and disrupt operation of other equipment.

The EMI can have two sources of origin: signals that are radiated into space and those that are conducted via speaker and power-supply wires. A useful principle is to minimize the area of loops that carry high-frequency currents, since the strength of associated EMI is related to loop area and the proximity of loops to other circuits [6]. The amount of power radiated from these loops is dependent of the loop area when compared to the wavelength of the signals, therefore it is also

important to reduce the maximum frequency of the signals in the amplifier. This means that it is very important to use a switching frequency as low as possible, corresponding to using a low OSR in the ΣΔ modulator.

III. 3RD ORDER CONTINUOUS-TIME (CT) ΣΔ MODULATOR

The first step in the design of the modulator is choosing the order modulator and the clock frequency value.(ΣΔ) modulators of orders higher than 2 are possible to design but they cannot simply be made by adding further stages because the resulting system would, most likely, be unstable. In view of this problem, the design procedure for finding the optimal 3rd ΣΔ modulator coefficients was based on the described in [4]. Briefly, this methodology describes an empirical method based on ordinary filter design that can be used to design high-order loops.

The sensitivity of the human ear is biased toward the lower end of the audible frequency spectrum, around 3 kHz. Being 50 Hz, the bottom end of the spectrum, and being 17 kHz, the top end, the sensitivity of the ear is down by approximately 50 dB on that at 3 kHz [7]. Taking advantage of these features of the ear and considering that most people will not be able to hear above 16 kHz, the bandwidth of an audio amplifier, in reality, does not need to be higher than 18 kHz. Therefore the modulator will be designed to have a signal bandwidth of 18 kHz and a peak SNDR value larger than 80 dB (the SNDR is defined for a bandwidth of 18 kHz).

As previously stated, it very important to use a low sampling frequency value in order to reduce the EMI of the amplifier and also to avoid non-ideal effects in the output devices during the switching. A ideal 3rd ΣΔ modulator (assuming that will be stable) with an OSR value of 32 could theoretically produce an SNDR value of around 95 dB. Therefore a sampling frequency value of 1.2 MHz is selected, resulting in a OSR about 33.3.

However, due to the inherent instability of the modulator it is necessary to use a transfer function that limits the noise shaping resulting in a lower SNDR value. Therefore, several architecture options for the modulator in order to improve the SNDR value, will be studied.

A. 1-bit with Distributed Feedback

The block diagram of the 3rd order 1-bit ΣΔ modulator with distributed feedback, implemented using CT integrators, is shown in Figure 3. The signal transfer function (STF) of this structure is given by Equation 1 and will be essentially a 3rd order Butterworth low pass filter. The cut-off frequency of this filter function is selected in order to limit the maximum gain of the NTF and eliminate the instability of the modulator.

The noise transfer function (NTF) given by Equation 2 was designed to be a 3rd order Butterworth high-pass filter with a cut-off frequency of 99.6 kHz. The values of the coefficients b_1, b_2 and b_3 were calculated in order to implement the selected Butterworth transfer function. The modulator was simulated using $SIMULINK^{®}$. Each simulation was calculated using 2^{19} points and a fast Fourier transformation using a Blackman-Harris window was applied.

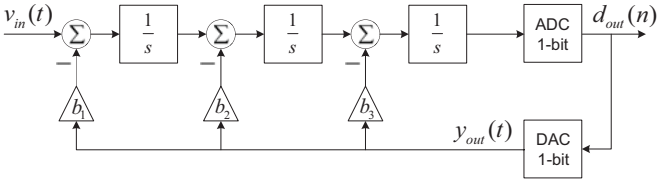

Fig. 3. Block diagram of the 3rd order 1-bit ΣΔ modulator with distributed feedback.

$$STF = \frac{1}{s^3 + s^2 \cdot b_3 + s \cdot b_2 + b_1} \tag{1}$$

$$NTF = \frac{s^3}{s^3 + s^2 \cdot b_3 + s \cdot b_2 + b_1} \tag{2}$$

Figure 4 shows the output spectrum of the traditional 3rd order 1-bit ΣΔ modulator, obtained by simulation, in this case a maximum SNDR value of 64.2 dB was obtained. The frequency of the sine wave input signal is 1 kHz.

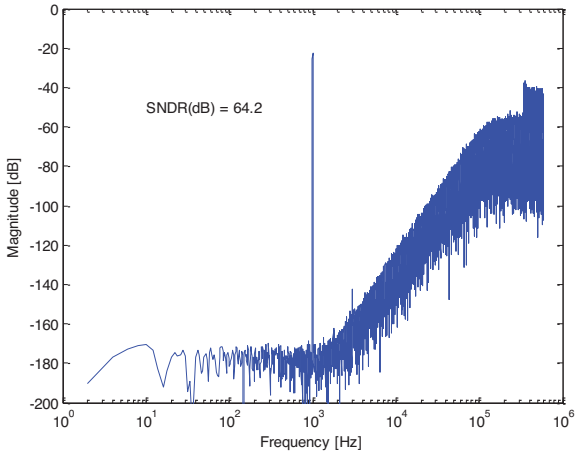

Fig. 4. Output spectrum of the 3rd order 1-bit ΣΔ modulator with distributed feedback (2^{19} points FFT using a Blackman-Harris window).

B. 1-bit with Distributed Feedback and Local Resonator Feedback

One technique to improve the SNDR is to optimally distribute the zeros of NTF inside the signal bandwidth, unlike the traditional design described above where NTF zeros are all placed at DC. The architecture shown in Figure 5 allows distributing the zeros of NTF inside the signal bandwidth and can be designed using a Chebyshev type II filter, in this case the stopband edge frequency of the filter is 18 kHz. The coefficients b_1, b_2 and b_3 fix the position of the poles and α the position of the zeros of the NTF (Equation 4). Note that the zeros do not appear in the STF (Equation 3).

$$STF = \frac{1}{s^3 + s^2 \cdot b_3 + s \cdot (\alpha + b_2) + b_1} \tag{3}$$

$$NTF = \frac{s \cdot (s^2 + \alpha)}{s^3 + s^2 \cdot b_3 + s \cdot (\alpha + b_2) + b_1} \tag{4}$$

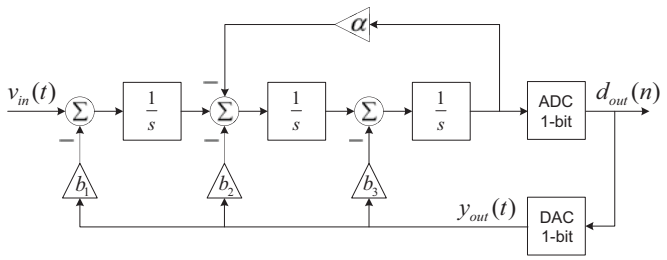

Fig. 5. Block diagram of the 3rd order 1-bit ΣΔ modulator with distributed feedback and local resonator feedback.

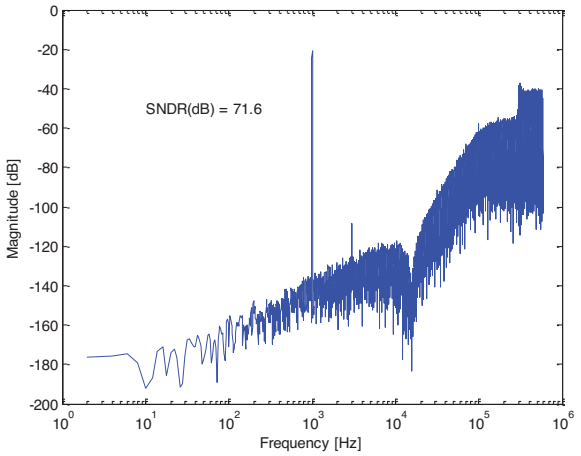

Fig. 6. Output spectrum of the 3rd order 1-bit ΣΔ modulator with distributed feedback and local resonator feedback (2^{19} points FFT using a Blackman-Harris window).

The Figure 6 shows the output spectrum of the 3rd order 1-bit ΣΔ modulator with distributed feedback and local resonator feedback, obtained by simulation, in this case a maximum SNDR value of 71.6 dB was obtained. As expected, the shift of the zeros from DC to the signal bandwidth improved the maximum SNDR value.

C. 1.5-bit with Distributed Feedback

Another option to improve the SNDR is use a 1.5-bit quantizer (corresponding to three-level quantization) instead of 1-bit quantizer. The increase of the resolution of the quantizer improves the linearity of the feedback in the modulator. Since this results in a more stable loop, it is possible to use a larger cut-off frequency in the modulator and therefore improve the maximum SNDR value. In this case a cut-off frequency of 133.2 kHz was used. The use of three levels also reduces unnecessary switching of the full-bridge output stage so that the switching loss is minimized.

Figure 8 shows the simulated output spectrum of the 3rd order 1-bit ΣΔ modulator with a 1.5-bit quantizer, in this case a maximum SNDR value of 76.9 dB was obtained. As expected the increase in the resolution of the quantizer improved the maximum SNDR value of the modulator.

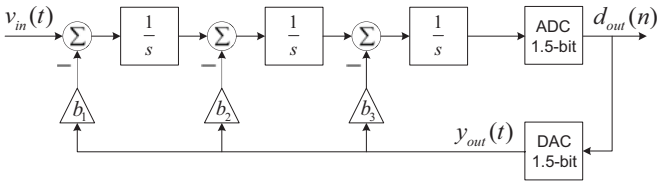

Fig. 7. Block diagram of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback.

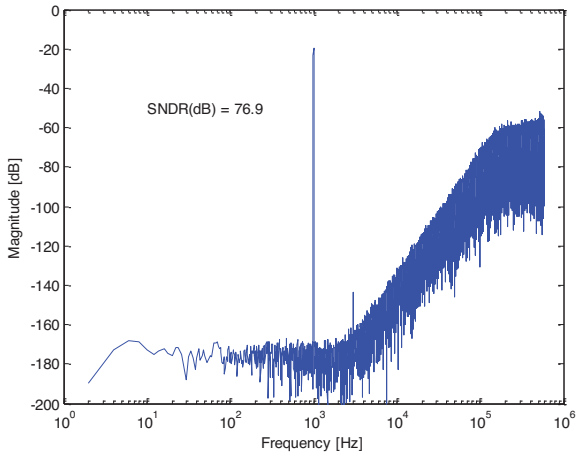

Fig. 8. Output spectrum of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback (2^{19} points FFT using a Blackman-Harris window).

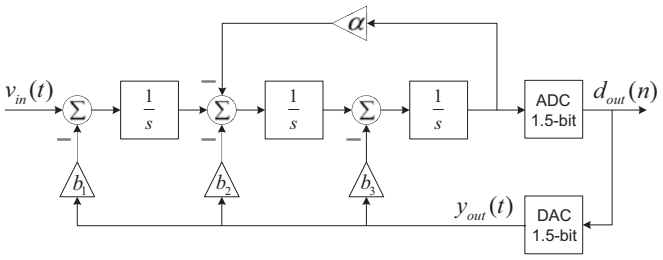

Fig. 9. Block diagram of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback and local resonator feedback.

IV. Proposed Architecture for the ΣΔ Modulator

In order to obtain a maximum SNDR value larger than 80 dB, the topologies described above (3rd order 1-bit ΣΔ with distributed feedback and local resonator feedback and the 3rd order 1.5-bit ΣΔ with distributed feedback) were combined into one modulator (Figure 9). The loop filter in the modulator was designed to have a stopband edge frequency of 18 kHz.

Figure 10 shows the output spectrum of the modulator, obtained by simulation, in this case a maximum SNDR value of 81 dB was obtained. The combination of all the previous techniques allowed to obtain a maximum SNDR value larger than 81 dB using a 3rd order ΣΔ modulator with an OSR value of approximately 32.

V. Circuit Design

It is necessary to design an electrical circuit that has the same behavior as the architecture that was developed

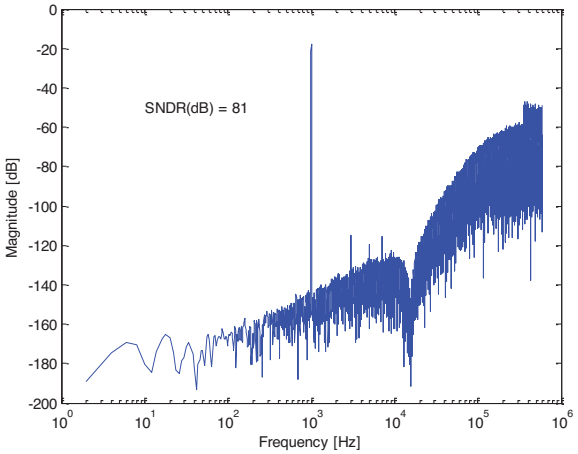

Fig. 10. Output spectrum of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback and local resonator feedback (2^{19} points FFT using a Blackman-Harris window).

in the previous section. During this design, as it will be explained next, it was realized that due to the variations of the components of the filter (capacitors, resistors, and operational amplifiers), the modulator circuit could become unstable. In order to increase the yield of the design it was necessary to reduce the gain of the NTF in order to make the modulator more stable.

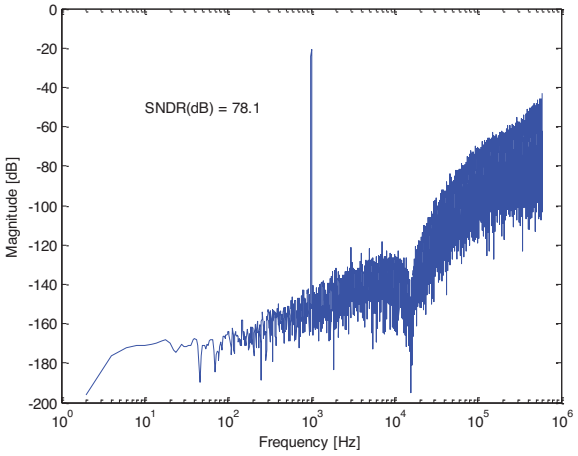

Fig. 11. The new output spectrum of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback and local resonator feedback (2^{19} points FFT using a Blackman-Harris window).

The modulator with the new NTF was simulated and the new output spectrum of the 3rd order 1.5-bit ΣΔ modulator with distributed feedback and local resonator feedback is shown in Figure 11, in this case the maximum SNDR value is 78.1 dB, as expected, the added stability of the modulator resulted in a lower value for the SNDR. However, with increased stability margin due to reduced gain of the NTF, the harmonics are attenuated.

The Table I gives the coefficients values of the simulated architecture.

TABLE I
COEFFICIENTS OF THE PROPOSED ARCHITECTURE.

Coefficients					
k_0	$k_1 = k_2 = k_3$	b_1	b_2	b_3	α
0.0415	1	0.1173	0.4772	0.9701	0.0066

The Figure 12 shows a simple method to convert the mathematical model into the electrical model. Note that the T_S ($\frac{1}{F_S}$) is the period of the sampling frequency (F_S = 1.2 MHz).

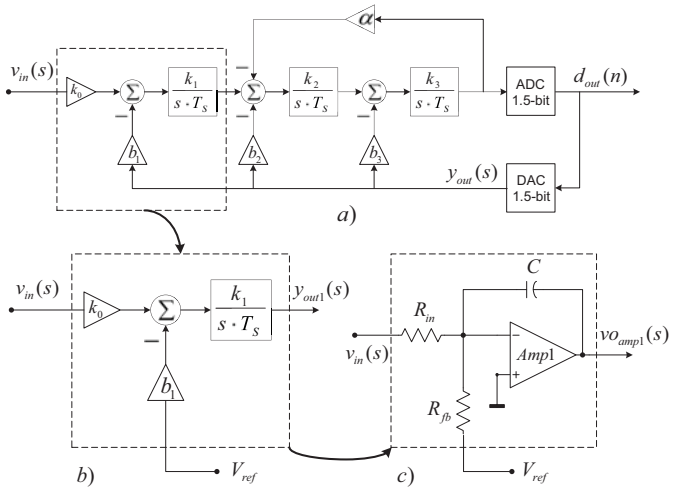

Fig. 12. Conversion of the mathematical model into the electrical model.

Analyzing the Figure 12.b) an equation for the $y_{out1}(s)$ can be written as:

$$y_{out1}(s) = \frac{k_0 \cdot k_1}{s \cdot T_S} \cdot v_{in}(s) - \frac{b_1 \cdot k_1}{s \cdot T_S} \cdot v_{ref}(s) \quad (5)$$

The equation for the output ($vo_{amp1}(s)$) of the integrator (depicted in Figure 12.c)) is given by:

$$vo_{amp1}(s) = \frac{1}{s \cdot R_{in} \cdot C} \cdot v_{in}(s) - \frac{1}{s \cdot R_{fb} \cdot C} \cdot v_{ref}(s) \quad (6)$$

Equaling Equation 5 to Equation 6 ($y_{out1}(s) = vo_{amp1}(s)$) is possible to obtain an expression for R_{in} and R_{fb}. Note that the operational amplifier is considered ideal in this approach.

$$R_{in} = \frac{T_S}{k_0 \cdot k_1 \cdot C} \quad (7)$$

$$R_{fb} = \frac{T_S}{b_1 \cdot k_1 \cdot C} \quad (8)$$

The same idea can be applied to the other integrators blocks of the modulator resulting in the modulator circuit shown in Figure 13. The values of the components can be obtained using the approach previously described, assuming that all the capacitors have a 1nF value.

Table II gives all passive component values for the modulator.

In order to confirm the correct design of the modulator, the STF (Figure 14) and NTF (Figure 15) of the modulator are

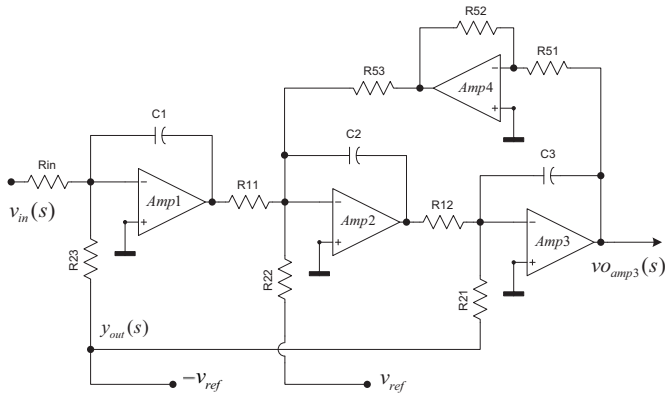

Fig. 13. Schematic design of the modulator.

TABLE II
SELECTED PASSIVE COMPONENT VALUES.

Components		
Id.	Value	Units
$C_1 = C_2 = C_3$	1	nF
R_{in}	20.5	kΩ
$R_{11} = R_{12}$	825	Ω
R_{23}	7.15	kΩ
R_{22}	1.74	kΩ
R_{21}	845	Ω
$R_{51} = R_{52}$	10	kΩ
R_{53}	127	kΩ

obtained by performing two AC simulations of the circuit of Figure 13.

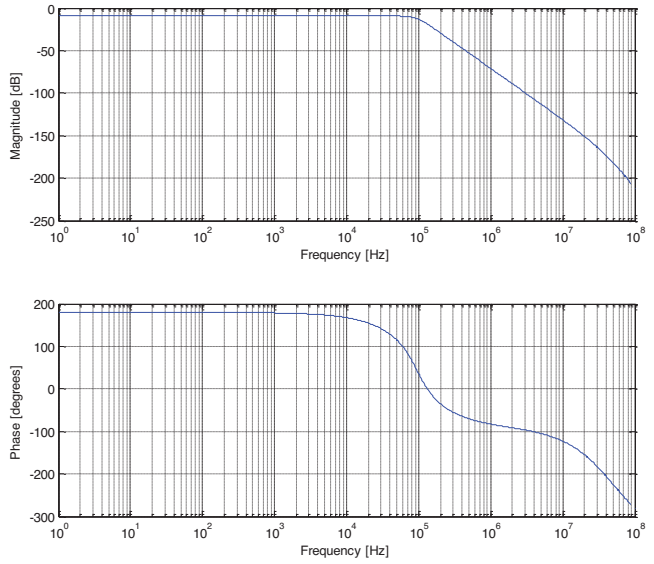

Fig. 14. Bode diagram of the STF of the modulator.

A. ADC Design

The 1.5-bit quantizer (three levels) is realized by two comparators and is showed in Figure 16. The output of the comparators is encoded to 1.5-bit representation using the

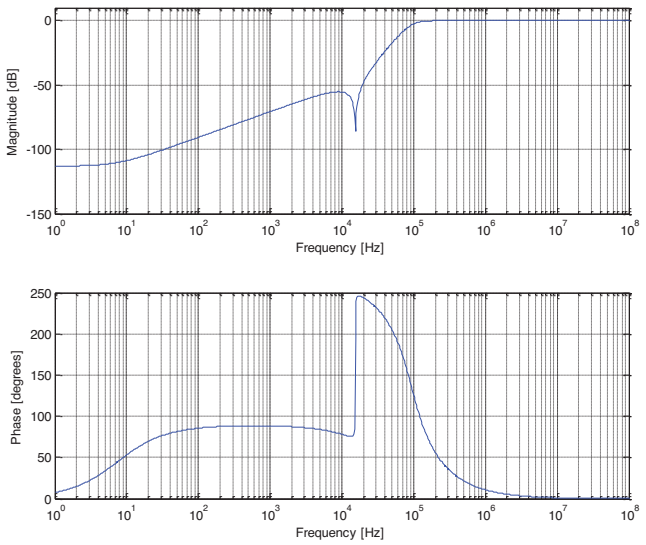

Fig. 15. Bode diagram of the NTF of the modulator.

circuit shown in Figure 19. The threshold voltage for comparison is determined by several simulations of the propose architecture in order to obtain the max point of the SNDR as function of the threshold voltage. The Figure 17 shows the measured SNDR as function of threshold voltage (V_t) and the selected value was 0.33V.

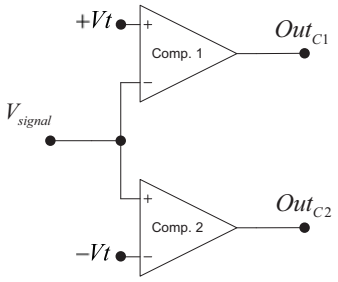

Fig. 16. Schematic design of 1.5-bit quantizer.

TABLE III
ADC CODIFICATION.

V_{Signal}	State	Out_{C1}	Out_{C2}
$V_{Signal} > V_t$	+1	0	1
$-V_t < V_{Signal} < V_t$	0	1	1
$V_{Signal} < V_t$	-1	1	0

Since the threshold voltage of the comparators has a random error, a Monte Carlo simulation where the V_t voltage of the comparators was randomly changed with a 3σ value of 10 mV was performed for 500 cases. The histogram of the SNDR values obtained in this analysis is shown in Figure 18, this histogram shows that the SNDR in worst case only degrades about 0.7 dB with the variation of the offset of the comparators.

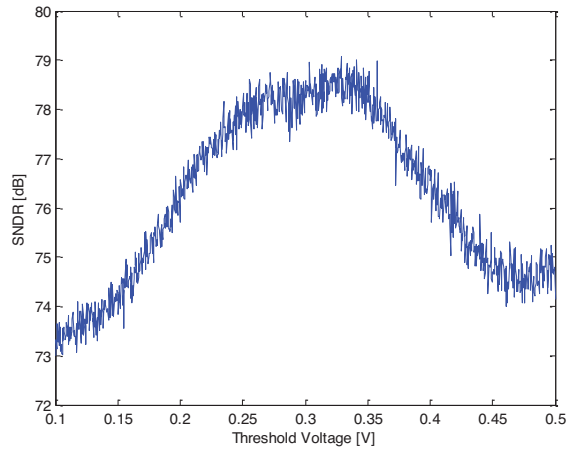

Fig. 17. Measured SNDR as function of threshold voltage (V_t). Data obtained by running 1000 simulations with a Vt step of 0.4 mV.

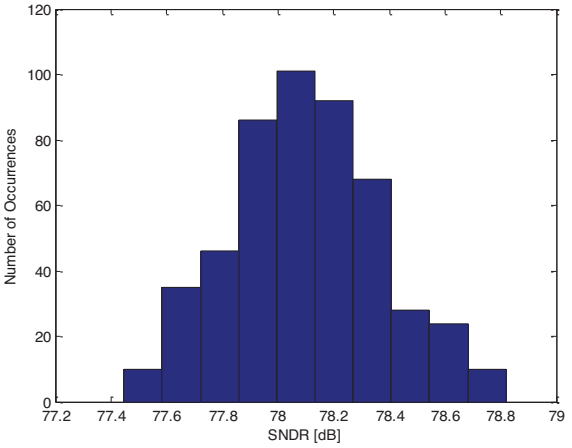

Fig. 18. Histogram of the behavioral simulated SNDR of the proposed ΣΔ modulator ($3\sigma_{vt} = 10$ mV) . Data obtained by running 500 Monte-Carlo simulations of the proposed architecture.

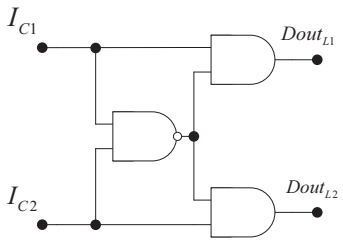

Fig. 19. Encoding logic for 1.5-bit quantizer.

TABLE IV
LOGIC CODIFICATION OF THE 1.5-BIT QUANTIZER.

I_{C1}	I_{C1}	State	$Dout_{L1}$	$Dout_{L2}$
0	0	x	0	0
0	1	+1	0	1
1	0	-1	1	0
1	1	0	0	0

B. Important Parameters in Operational Amplifiers

In the previous analysis it was assumed that the operational amplifiers were ideal, when real amplifiers are used the non-ideal effects can change the behavior of the modulator. In order to understand what is the required performance of the different parameters of the amplifiers, such as: gain-bandwidth product (GBW), slew rate and DC gain, the modulator circuit was simulated using a first order electrical model for the amplifiers. This model includes DC gain, a single pole and the slew rate effect. In these simulations the amplifier parameters were set to different values in order to determine the minimum required values for the different parameters.

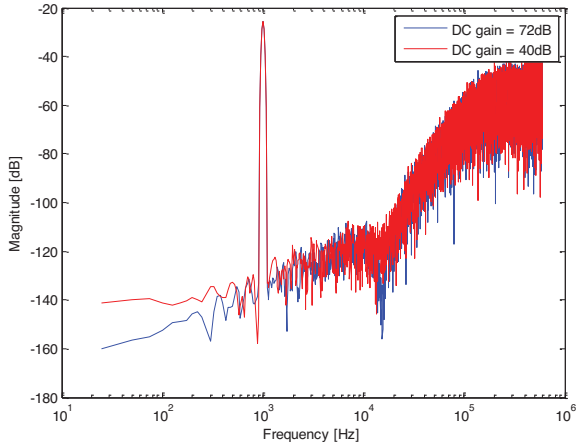

Fig. 20. Influence of the DC gain in the output spectrum of the modulator (results obtained with electrical simulations with first order model amplifier with a GBW = 50 MHz, and a slew rate = 10 V/μs).

To investigate SNDR degradation due to variation of the parameters of the operational amplifiers, different electrical simulations with variations in the DC gain, the GBW, and the slew rate were performed. In these simulations a first order model for the amplifier with a DC gain = 72 dB, a GBW = 50 MHz, and a slew rate = 10 V/μs was used. The output of the circuits was analyzed using a 2^{16} points FFT with a Blackman-Harris window, these results are shown in Figures (20, 21, and 22).

Observing Figure 20 it is clear that a reduction of the DC gain of the first amplifier causes a reduction of noise shaping at low frequencies. The reduction of the gain in the second and third operational amplifier decreases notch attenuation due to zeros in the NTF.

As it can be observed in Figure 21, the decrease of the GBW of the amplifiers decreases the frequency of the zeroes, resulting in added noise in the upper part of the signal band, therefore degrading the SNDR.

From Figure 22 it is possible to conclude that a low slew rate in the amplifier results in added distortion and a degradation of the notch produced by the zeroes.

These simulations show that if the amplifiers have a DC gain of 72 dB, a GBW of 50 MHz and a slew rate of 10 μV they do not affect the performance of the modulator significantly.

C. Simulation Results

In order to verify the stability of the design, a 500 cases Monte Carlo analysis where the value of the components were

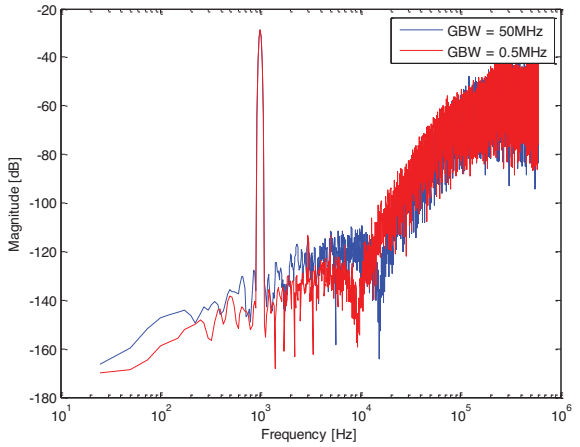

Fig. 21. Influence of the GBW in the output spectrum of the modulator (results obtained with electrical simulations with first order model amplifier with a DC gain = 72 dB, and a slew rate = 10 V/μs).

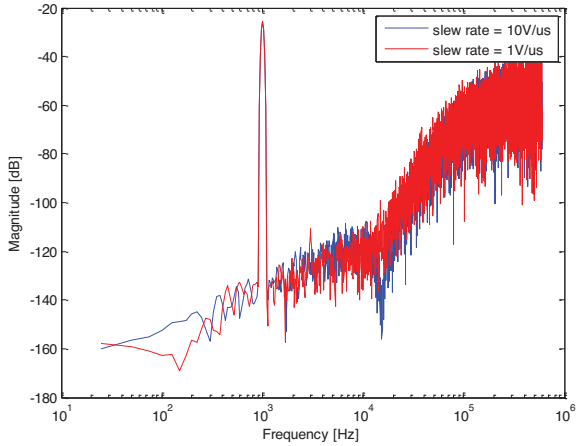

Fig. 22. Influence of the slew rate in the output spectrum of the modulator (results obtained with electrical simulations with first order model amplifier with a DC gain = 72 dB, and a GBW = 50 MHz).

randomly selected around the nominal values with a normal distribution with $3\sigma = 5\%$ for the capacitors and with $3\sigma = 1\%$ for the resistors. Figure 23 shows the histogram of the SNDR values obtained in this analysis, and shows that the SNDR in worst case degrades about 1.5 dB due to components mismatch.

The output swing of the three integrators in the modulator was verified using behavioral simulations. The histogram of each output voltage is depicted in Figure 25, these histograms show that the output voltages are smaller than $\pm$ 1.2V, therefore the operational amplifiers should not approach saturation during the operation of the circuit.

Figure 24 shows the circuit implementation of the proposed architecture. This circuit was simulated using an electrical simulator and the output spectrum was calculated, this is shown in Figure 26. The electrical simulations used a first order model amplifier with a DC gain = 72 dB, a GBW = 50 MHz, and a slew rate = 10 V/μs.

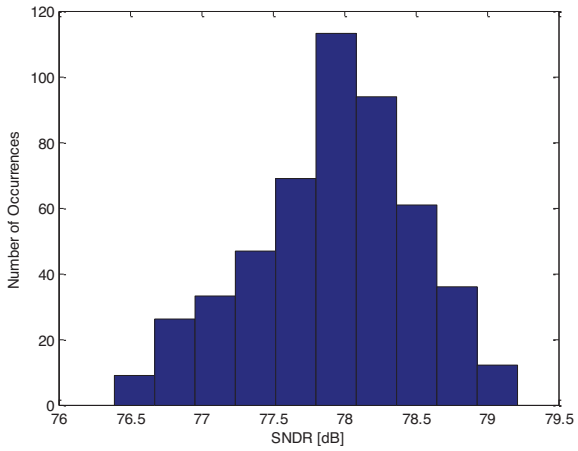

Fig. 23. Histogram of the behavioral simulated SNDR of the proposed $\Sigma\Delta$ modulator with component values mismatch of $3\sigma\frac{\Delta R}{R} = 1\%$ and $3\sigma\frac{\Delta C}{C} = 5\%$. Data obtained by running 500 Monte-Carlo simulations of the proposed architecture.

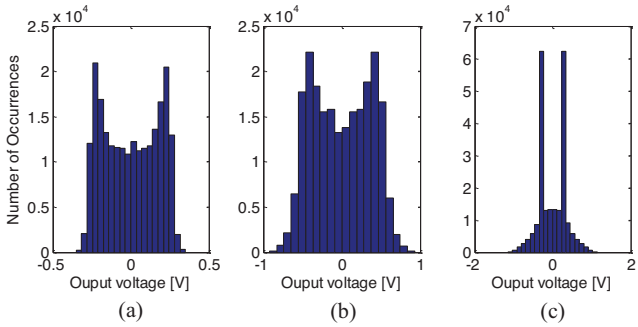

Fig. 25. Histogram of the behavioral simulated output voltage of the (a) first integrator, (b) second integrator, and (c) third integrator for the proposed $\Sigma\Delta$ modulator.

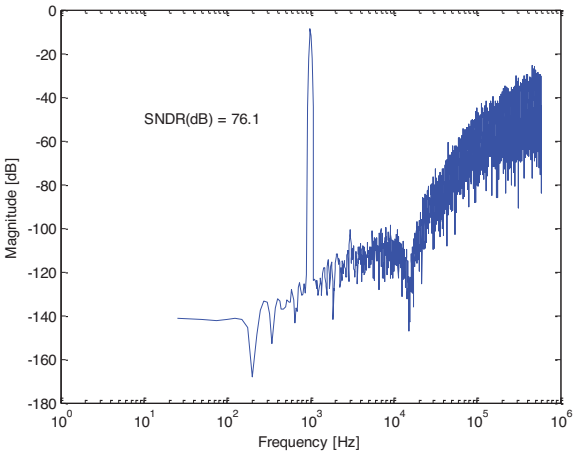

Fig. 26. Output spectrum of the proposed architecture obtained with electrical simulations with first order model amplifier with a DC gain = 72 dB, a GBW = 50 MHz, and a slew rate = 10 V/μs (2^{16} points FFT using a Blackman-Harris window).

VI. Conclusion

This paper presents a 3rd order 1.5-bit $\Sigma\Delta$ modulator with distributed feedback and local resonator feedback for

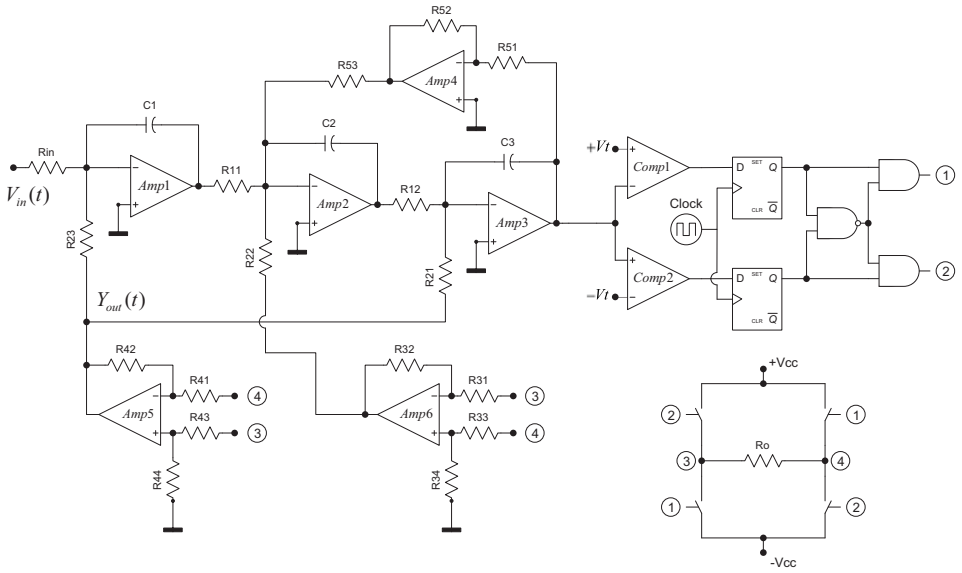

Fig. 24. Class D audio amplifier implementation.

a Class D audio amplifier. In order to improve the SNDR, without increasing the OSR or the order of the modulator (not greater then 3), the modulator uses transmission zeros and 1.5-bit quantization. High level simulations of the modulator show that it has a maximum SNDR value of 81 dB for a signal bandwidth of 18 kHz and a sampling frequency of 1.2 MHz. The increase of the resolution of the quantizer (1.5-bit quantizer instead of 1-bit quantizer) improves the linearity of the feedback in the modulator. Since this results in a more stable loop, it is possible to increase the stopband ripple in the modulator and therefore improve the maximum SNDR value. An electrical circuit was designed to implement the proposed architecture and the electrical simulations showed that it has a maximum SNDR value of 76.1 dB. The influence of the constituting blocks of the circuit in the performance of the modulator was investigated using electrical simulations.

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