Application of Digital Potentiometers in Multifunctional Active Filters at Frequencies above 1 MHz

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***Abstract*—The practical performance results of digital potentiometers compared with Spice-based macro model at frequencies above 1 MHz are discussed in the paper. Verification and validation checks have been performed on the new Spice compatible macromodel developed on the basis of extensive testing of the models behavior from different reputable companies such as Maxim, Analog Devices, Intersil, Texas Instrument, etc. The real properties of these digital devices are compared in several types of programmable universal active filters. Subsequently the possibilities of using chain structure for the creating of a digital potentiometer with high resolution and applicable to frequencies exceeding 1MHz frequency band are presented. Finally, the control software is introduced.**

***Index Terms*—Digital potentiometer, chain structure, macromodel, universal filter, I^{2}C, SPI, parasitic influences**

I. Introduction

THE resistor potentiometers can be found in electronic circuits across a wide spectrum of applications. Most typically, they function in a voltage divider configuration in order to execute various types of tasks, such as offset or gain adjusts. Digital potentiometers or digpots exhibit the same fundamental operation as the mechanical parts with only one exception, namely the wiper position is digitally adjusted. Digital trimming of variable impedances is one of the most popular methods for adjusting the functions and performance parameters of modern analog and mixed signal systems. The demand for higher resolution and increased tuning accuracy is driving the research efforts toward developing multistage potentiometer architectures that employ special techniques for achieving high precision with fewer components. The attainable stability and accuracy of digital potentiometers tends to continuously improvement and is still in research.
Currently, it is possible ensuring less than 1% end-to-end resistor tolerance error, for example at AD5271 [1]. During the last two decades, the extensive development of integrated potentiometers which provide well-determined impedances as a result of processing a digital sequence, made possible the introduction of digitally controlled adjustments within all types of electronic products ranging from consumer electronics, mobile communication devices, computers and PDAs, to industrial, automotive and medical applications. Digital potentiometers are suitable for electronic systems that require digital control of currents, voltages, impedances, gain and frequency, and even for adjusting the variations with temperature of certain electrical parameters [2]. The basic structure of the digital potentiometer is shown in Fig. 1 and is described in detail in the next chapter.

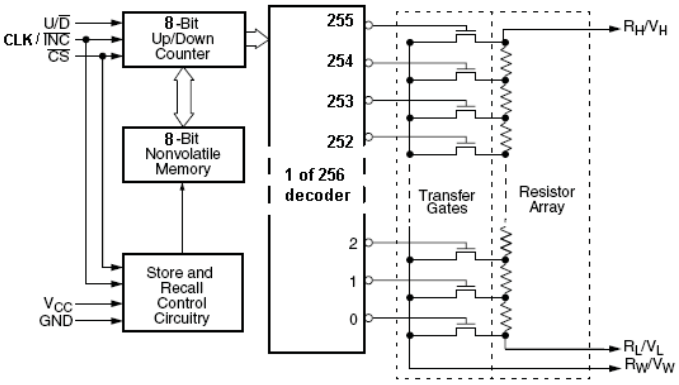

Fig. 1. The basic structure of the digital potentiometers

Today's modern digital potentiometers have a user memory for storing positions of wiper and useful premium features as a register of short commands for easy handling with multiple channels. It can be used in applications for the calibration of various devices.

II. Macromodel Description

A. Basic Structure

There are three most commonly used types of interfaces for communication with digital potentiometers. It is SPI, I^{2}C [3] and Up & Down. One of the newer potentiometer under test has a parallel interface [4]. This means that for errorless communication with proposed device described in Chapter IV

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below it is necessary to use one of the I^2C expanders [5]. The selected type of interface to create a macro model is not a primary issue in this case but is important for the overall design of the considered application. However, a brief description that follows describes the basic guidelines for creating functional interface in PSpice environment. Digitally controlled input interface can be formed as a system of several J-K flip-flops that store the tap position on their non-inverting outputs [6]. In the case of the Up & Down interface, three control signals (digital inputs) are used. These digital inputs are INC, CS and U/D. The INC input is the wiper increment control input. A high to low transition on this input increments or decrements the wiper position depending on the states of CS and U/D. The CS input is the chip select input. When this input is low (log. 0), the wiper position may be changed through INC and U/D. The U/D input is the up/down control input. When this input is high, a high-to-low transition on INC increments the wiper position, and when the input is low, a high-to-low transition on INC decrements the wiper position. This type of digital control is very similar to SPI Interface in which the digital input CS performs the same function and digital input INC is replaced by CLK. In most cases, a control byte containing a number of wiper position and also a channel number in the case of multi-channel potentiometers is usually transmitted. The I^2C bus uses two wires called SCL and SDA. SCL is the clock line and it is equivalent to CLK. It is used to synchronize all data transfers over the I^2C bus. SDA is the data line. All transmissions over the bus are controlled by specific rules typical for this type of interface. The basic model of the digital potentiometer macro consists of a 256 bit counter whose outputs are sent to a D/A converter (DAC). The output of the DAC is then used to determine the value of a pair of resistors. Validations and verification of DAC is implemented in detail in [7] and basic specification of parameters for dynamic and static characteristics are very similar to the digital potentiometer. Two resistors of the potentiometer then use the output voltage of the DAC for determining their own resistance values. When the counter is incremented, the resistance value of the R_L resistor is increased, and subsequently, the R_H resistor value is decreased. The value attributes of the R_L and R_H resistors are defined for the potentiometer with 256 steps as

$$R_L = R_{DAC}\frac{D_W}{256} + R_W \ , \tag{1}$$

$$R_H = R_{DAC}\left(1 - \frac{D_W}{256}\right) + R_W \ , \tag{2}$$

where R_{DAC} is the macro parameter which represents the nominal resistance value for the potentiometer, D_W is the number of tap position of the potentiometer and its maximal range is represented by the value 256 in this case (D_W value can be used as a macromodel parameter and varies from 32 to 1024 according to a selected potentiometer), R_W is a wiper resistance.

The equation above describes an idealized model which is valid in DC or low frequency applications. The three outputs of the potentiometer can be identified as the outputs H, W, and L. These correspond to the high terminal, wiper terminal and low terminal of the potentiometer, see Fig. 2.

B. Real Properties of Digital Potentiometers

Digital potentiometers are extremely useful for controlling of adjusting circuit parameters. Normally they are only used in DC or low frequency applications due to the inherent bandwidth limitations of the digital pots. In such cases the model described above is valid. In AC applications, it is necessary to take into account a typical -3dB bandwidth parameter that determines the maximum frequency application and stability of the digital potentiometer. This parameter is listed in datasheets and its value varies from 50 kHz to 10 MHz [3], depending on resistance value and the number of positions of digital potentiometer. The accuracy of digital potentiometers is affected by multitude of factors. Identifying a root causing the errors is essential for improving the design performance. Thus, the on-resistance of the switches, the device matching, the parasitic devices, the spread of the technological parameters, the variations with the operating conditions, are all affecting the precision of digital potentiometers.

The on-resistance of electronic switches and parasitic capacitance of wiper are the most important sources of errors in digital potentiometers. A typical potentiometer parasitic simulation model has been developed and is shown in Fig. 2.

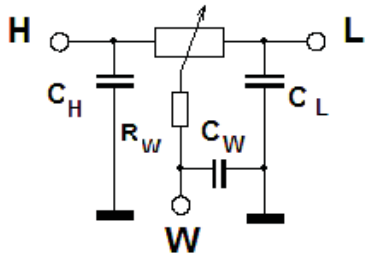

Fig. 2. Simplified parasitic model of digital potentiometer.

An example of the wiper switch resistance variation measurement with the number of positions set from 0 to 256 is shown in Fig. 3. Two types of digital potentiometers AD5241 and DS1803, both with 256 positions and 10 kΩ nominal resistances are compared. The figure shows a relatively large difference between the wiper resistances of these two digital potentiometers. Therefore it is possible to assume that the digital potentiometer AD5241 [8] uses a multistage architecture with any of the switches on-resistance minimization techniques in [2], [9]. Typically, the minimization of the switches on-resistance is achieved by increasing the size of the pass devices and by properly choosing the substrate bias scheme. For example in [9], the preferred positions for the medium range stages are adjacent to the reference terminals, in order to minimize the switch resistance variation due to the substrate bias effect while switching throughout various stages. Moreover, dummy

structures can be introduced on various branches of the network in order to match the existing bypass switches, as shown in [2]. However, for stable operation of digital potentiometers at frequencies above 1 MHz, it is important a small wiper switch resistance swing which can be seen in digital potentiometer AD5241, see Fig. 3.

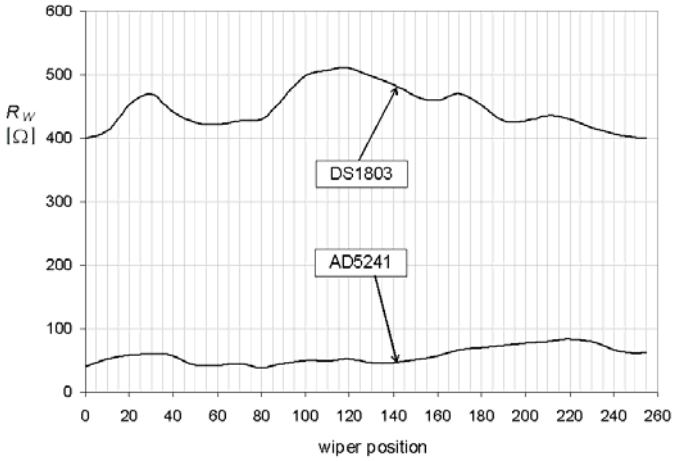

Fig. 3. Wiper switch resistance for two types of digital potentiometers

A parasitic capacitance is inherent to all digital potentiometers and is a limited factor of the circuit frequency bandwidth. Actual wiper capacitance can vary from 3 pF to over 120 pF and is function of wiper resistance, the number of steps the IC process used and the pot architecture used. In Fig. 2 above there are shown three parasitic capacitances. The modeling and practical testing shows that the largest impact on changes in circuit parameters has the growing wiper parasitic capacitance C_W. In Fig. 4 it is shown how the value of wiper parasitic capacitance affects the maximum achievable frequency bandwidth (BW_{3dB}).

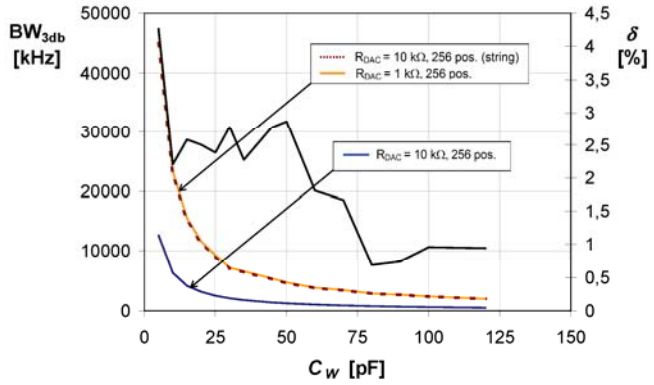

Fig. 4. Wiper parasitic capacitance of two types of digital potentiometers

Analysis of the parasitic capacitances was performed by using the AC method. The AC method is a frequency domain measurement. A 10-MHz AC voltage signal of known DC offset with small amplitude (for example 100 mV) is applied to the pin under test. The imaginary component of the complex current is measured and used in the equation

$$C = \frac{I_{IM}}{2\pi f \cdot V_{IN}} , \tag{3}$$

where I_{IM} is the imaginary component of an input current, V_{IN} is the magnitude of an input voltage, and f is the frequency.

The value of this parasitic capacitance increases with the increasing number of positions in use and its overall size depends also on the other design parameters such as total number of positions and the total potentiometer resistance value. Indispensable effect on the total maximum frequency band has also integration of digital potentiometer to the circuit [10] - [12]. One method is the using a parallel resistor string to lower the circuit impedance and is described in Fig. 5. Another alternative method to increase the BW_{3dB}. is the use of high-speed buffer BUF634 to adjust potentiometer outputs. This method was used for the frequency performance analysis in Fig. 16.

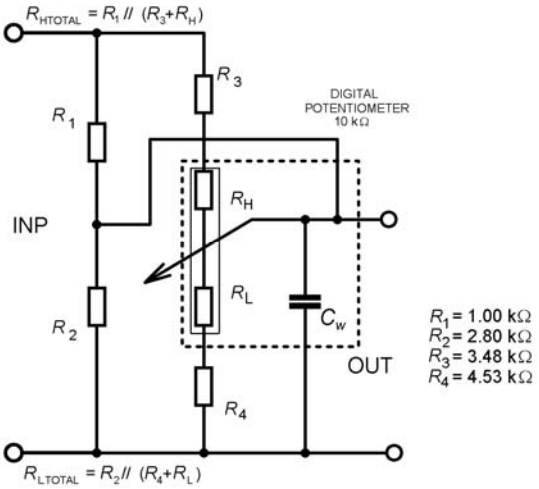

Fig. 5. Parallel resistor string used

This method in connection with 10 kΩ digital potentiometer allows to achieve almost the same performance as in the digital potentiometer with 10 times lower nominal resistance 1 kΩ, see Fig. 4. In this case the term δ expresses the relative difference between the maximum achievable BW_{3dB} fo digital potentiometer with a nominal resistance of 1 kΩ and nominal resistance of 10 kΩ using the parallel resistor string. Given the findings above there can be added to the macromodel the following equations (4) and (5) for the effect of parasitic capacitances included, see Fig. 2. These equations correspond to the type of a digital potentiometer AD8400 [13] (10 kΩ, 256 pos.) with the declared values of parasitic capacitances C_W = 120 pF and $C_H = C_L$ = 75 pF, measured at mid-range position of wiper. Similar expressions can be found in [13].

$$C_H = 90.4 \cdot 10^{-12} \cdot \left(\frac{D_W}{256} \right) + 30 \cdot 10^{-12} , \tag{4}$$

$$C_L = 90.4 \cdot 10^{-12} \cdot \left(1 - \frac{D_W}{256} \right) + 30 \cdot 10^{-12} , \tag{5}$$

where D_W is the number of wiper position in the potentiometer and its maximal range is represented by the value 256 in this case (D_W value can be used as a macromodel parameter and varies from 32 to 1024, according to the selected potentiometer), R_W is wiper resistance.

In fact, the situation is somewhat different. The equations above can be considered as an ideal variation of wipers parasitic capacitance. In Fig. 6 it is shown a dependence of the frequency bandwidth on the wiper positions. The comparison of Fig. 4 and Fig. 6 shows that the frequency stability of potentiometers at frequencies above 1 MHz requires the use of only about 10% of the range of digital potentiometer. Then it is possible to suppose the value of parasitic capacitances from 10 pF to 20 pF [10]. For different values of parasitic capacitances of digital potentiometers between the various manufacturers it is not easy to establish a general model. For macromodel in Fig. 6 the average value obtained from the multiple measurements of different potentiometers is used.

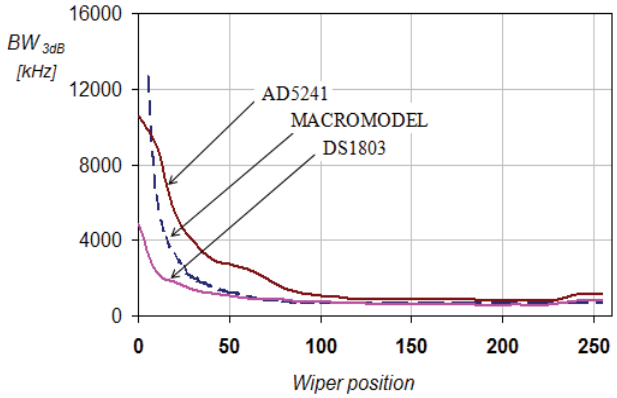

Fig. 6. Variation of BW_{3dB} in digital potentiometer

High resolution digital potentiometers are subject to a fundamental limitation: the increasing number of steps reduces the resistance of the elemental resistor to a value comparable with the on-resistance of the switches. Thus, the actual resistance value achieved on the wiper may differ from the ideal value for a given wiper position. Accuracy of digital potentiometers with a view to achieving the desired resistance is described by the integral non-linearity [2], [12] and is partially a result of the switches included in the signal path between the wiper and the reference terminal. Another important precision parameter, describing the deviation of the step variation from one tap to another is described as differential non-linearity [2], [12].

III. Macromodel Validation

A. *Universal filter*

The universal programmable filter UAF42 [14] from Texas Instruments will be used to compare the accuracy of the digital potentiometer with the macromodel. The parameters of this universal filter circuit can be easily controlled by external potentiometers. It uses a classical state-variable analog architecture with an inverting amplifier and two integrators. The circuit realized second order low-pass, high-pass, band-pass and band-reject transfer function. Test circuit including two digital potentiometers is shown in Fig. 7.

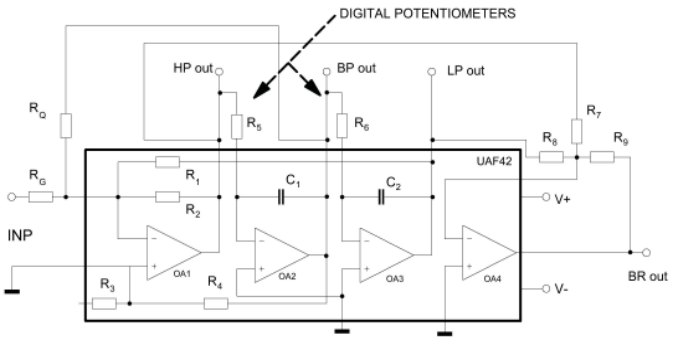

Fig. 7. Universal programmable filter

The pole (center) frequency is given as

$$f_p = \frac{1}{2\pi} \cdot \sqrt{\frac{R_1}{R_2 R_5 R_6 C_1 C_2}} \tag{6}$$

The filter is designed as a Butterworth and its quality factor $Q = 0{,}707$. The resistance R_Q can be calculated as

$$\frac{1}{Q} = \frac{R_1}{R_Q} \quad \Rightarrow \quad R_Q = Q \cdot R_1 \tag{7}$$

The values of resistors and capacitors integrated in UAF42 are $R_1 = R_2 = R_3 = R_4 = 50$ kΩ and $C_1 = C_2 = 1$ nF. The values of the external resistors are $R_G = 50$ kΩ, $R_Q = 35.4$ kΩ and $R_7 = R_8 = R_9 = 10$ kΩ.

In Fig. 8 and Fig. 9 the simulation results, experimental results and relative error for the pole (center) frequency versus tap position of the digital potentiometer are presented.

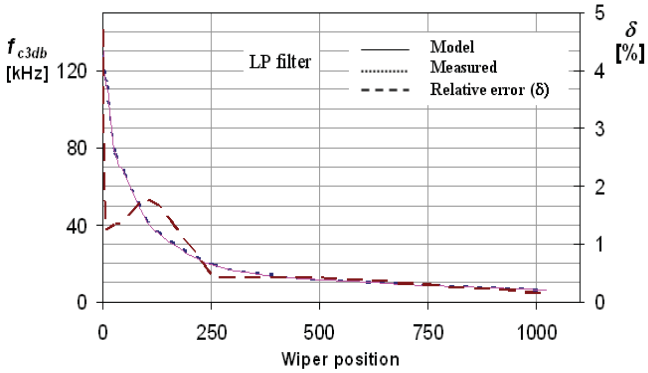

Fig. 8. Magnitude response of low-pass filter

The resistors R_5 and R_6 are represented by dual-channel, 1024-position resolution digital potentiometer AD5235 [15] with the nominal resistance $R_{DAC} = 25$ kΩ. The digital potentiometer is connected to a circuit including the series resistor $R_S = 1$ kΩ. The measurements results give a good agreement between the macromodel and the real digital potentiometer. The final error is not higher than 6 %. The larger error for band reject filter is caused by additional active and passive components.

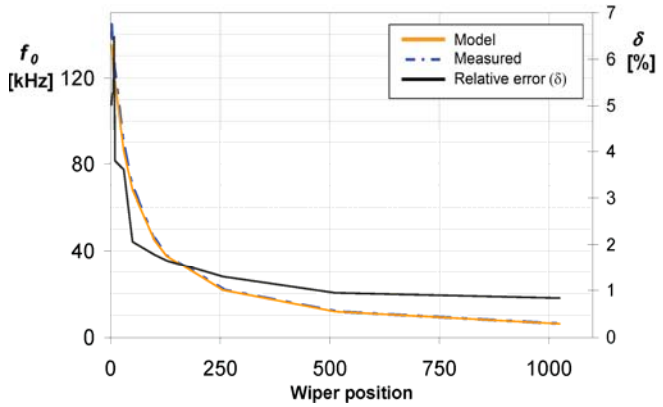

Fig. 9. Magnitude response of band-reject filter

However, the maximum value of BW_{3dB} is around 125 kHz for digital potentiometer AD5235. Generally available digital potentiometers with 1024-position resolution do not reach values of BW_{3dB} higher than 300 kHz. One way to achieve high resolution of digital potentiometer at frequencies above 1 MHz is daisy chain structure involving. This method can be applied only if SPI interface is used, see Fig. 10. For I^2C interface an addressing of more potentiometers in a single bus is included in the communication protocol.

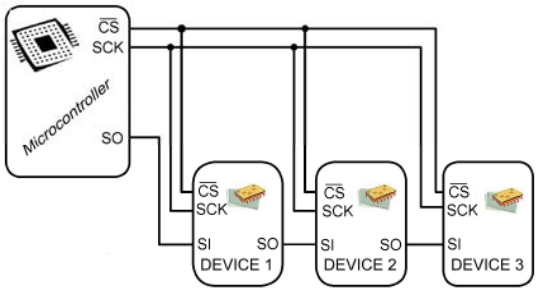

Fig. 10. Principle of daisy chain structure

In Fig. 11 and Fig. 12 simulation results, experimental results and relative error for the pole (center) frequency versus tap position of digital potentiometer at frequencies above 1 MHz are presented.

Digital potentiometer for frequencies above 1 MHz was created by combining three potentiometers with a nominal resistance $R_{DAC} = 2.5$ kΩ (AD5243 [15]) and one potentiometer with a nominal resistance $R_{DAC} = 1$ kΩ (AD5252 [16]). All four potentiometers have 256-position resolution. The digital potentiometer is connected to a circuit including the series resistor $R_S = 200$ Ω. In this case a discrete realization of the universal filter with operational amplifiers AD8042 [17] and capacitor values $C_1 = C_2 = 150$ pF is used for testing. The filter in this configuration is tunable in range of frequencies from about 121 kHz to about 4 MHz. It is also necessary to consider the parasitic effects of the filter circuit, which were not included in modeling and affect the final error. Better results can be achieved by using modern structures, which can also be controlled electronically [18], [19].

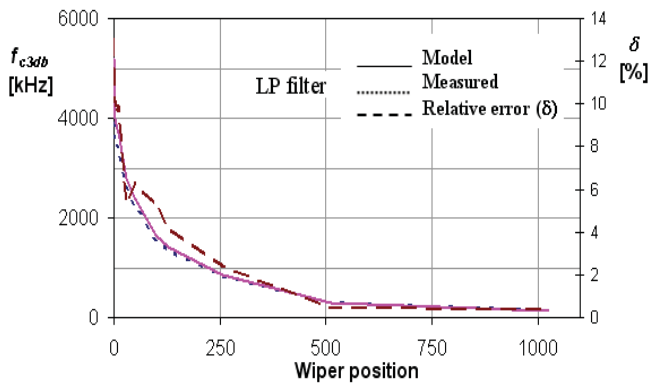

Fig. 11. Model and experimental results for the low pass filter with chain structure used

The final maximum error is higher than in the previous case and it is about 15 % for band reject filter. It should be noted that it is necessary to carefully select individual digital potentiometers with regard to the best resistive match of channels in tandem.

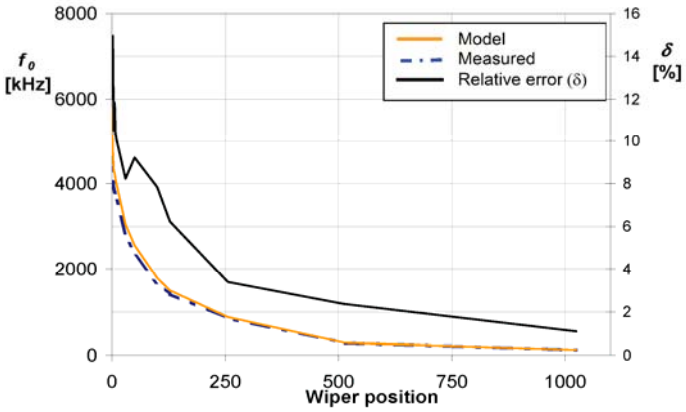

Fig. 12. Model and experimental results for the band reject filter with chain structure used

The final results of PSpice sensitivity analysis in Fig. 13 and Fig. 14 show how tolerance of each passive component affects the final value of f_{c3dB} frequency. In the first case, only tolerances of digital potentiometers were set to 10%.

Measurement	Original	Min	Max
Cutoff_Lowpass_3dB(V(lpp)) ...	1.0267meg	956.6714k	1.1040meg

Fig. 13. PSpice sensitivity analysis of the proposed filter

For the second variation the 1% resistors tolerance and 5% capacitors tolerance were chosen. It is obvious that the tolerance of individual elements have a greater impact on the overall frequency response than tolerances of digital potentiometers with somewhat higher tolerances. With regard to the use of chain structure and digital potentiometers with 256 tap positions we can generally assume a lesser differences between the original (simulated) and measured f_{c3dB}. frequency.

Measurement	Original	Min	Max
Cutoff_Lowpass_3dB(V(lpp))	1.0267meg	937.9401k	1.1339meg

Fig. 14. PSpice sensitivity analysis of the proposed filter - 2nd variation

The following Fig. 15 confirms the relatively good filter properties if we take into consideration the value of parasitic capacitances about 100 pF for each of the digital potentiometer used in filter.

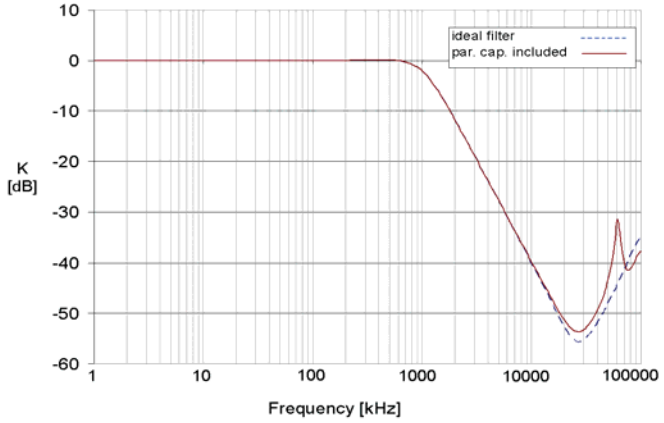

Fig. 15. Magnitude responses of proposed filter (low pass function)

The simulation in the Fig. 15 but ignored the real properties of digital potentiometers associated with effects of higher values of parasitic capacitances. This fact is graphically represented in Fig. 16 where the attenuation of the signal of a digital potentiometer TPL8002-25 [4] is analyzed. Each level of the signal for the set position of the digital potentiometer is moved to the reference level 3 dB to easy determine the value of BW_{3dB}. This fact is confirmed by further analysis below.

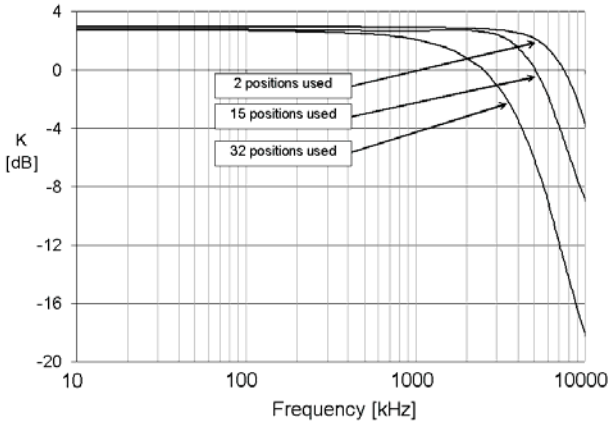

Fig. 16. Frequency response of TPL8002-25 digital potentiometer

B. Filter Building Block

For the realization of an universal filter with minimum of external components for frequencies above 1 MHz a commercially produced active-RC filter building block LT1568 [20] from Linear Technology is used. With a single resistor value, the LT1568 provides a pair of matched 2-pole Butterworth low-pass filters with unity gain suitable for example in I/Q channels. By using unequal-valued external resistors, the two 2-pole sections can create different frequency responses or gains. In addition, the two stages may be cascaded to create a single 4-pole filter with a programmable response. Capable of cut-off frequencies up to 10MHz, the LT1568 is ideal for antialiasing or channel filtering in older high speed data communication systems. The LT1568 can also be used as a band pass filter. After replacement of external resistors by digital potentiometers it is possible to create fully digitally controlled fourth order filter, see Fig. 17. The basic parameters for the filter settings are determined by (8), (9).

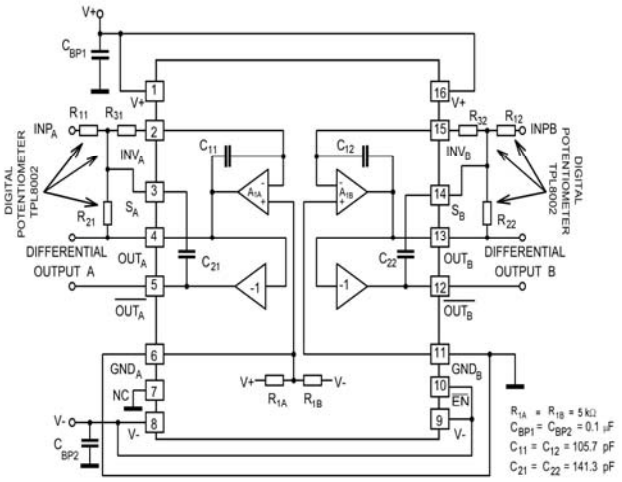

Fig. 17. Active RC-filter building block LT1568

The pole (center) frequency of each 2nd order filter is given as

$$f_p = \frac{1}{2\pi} \cdot \frac{1}{\sqrt{R_2 R_3 C_1 C_2}} \tag{8}$$

The filter can be easily designed as a Butterworth, Bessel or Chebyshev and its quality factor Q can be calculated as

$$Q = \frac{2\pi f_p \cdot C_1 C_2 R_1 R_2 R_3}{C_1\left[R_1(R_2+R_3)+R_2R_3\right]-C_2R_1R_2} \tag{9}$$

The proposed test board is able to configure both 2nd order active RC block separately or 4th order active filter with both 2nd order active RC blocks together.

In the first case the simple configuration of 2nd order Butterworth low-pass filter with digital potentiometers and f_{c3dB} = 2 MHz is analyzed. In this case, the same resistances value of digital potentiometers are set. It corresponds with 20 tap positions of digital potentiometers and resistance value is 634 Ω. It is clearly seen that parasitic capacitance discussed in section II significantly affects the actual achievable signal level in stop band. When we compare the proposed digitally controlled filter with a simply filter of the same order known as Sallen-Key (SK) with the standard resistors, it is evident a higher slope reached in the stop band. Also signal level in the stop band is at a frequency 10 MHz significantly better. For frequencies above 10 MHz the manufacturer does not

guarantee declared properties, see Fig. 18 and Fig. 19. The same type of the filter with standard resistors achieves signal level in stop band at least 15 dB better at 20 MHz. From 50 MHz to 100 MHz the filter with standard resistors copies simulated characteristics of the SK filter .

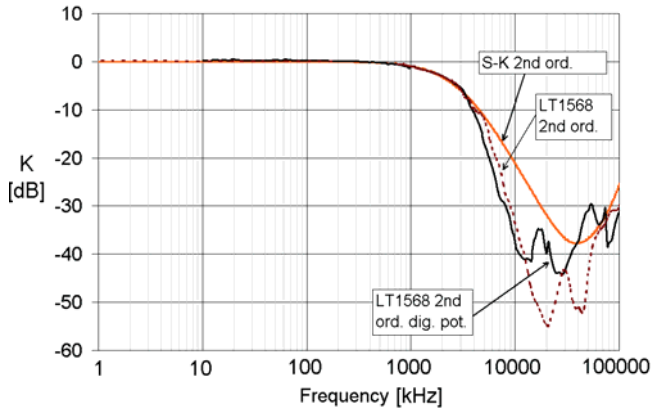

Fig. 18. Magnitude responses of LT1568 for 2nd order filter configuration

In the latter case, the 4th order low-pass filter with the Bessel approximation is analyzed. Despite the higher value of f_{c3db} = 3 MHz we have a magnitude response in the frequency range from 10 MHz to 50 MHz without significant ringing, see Fig. 19.

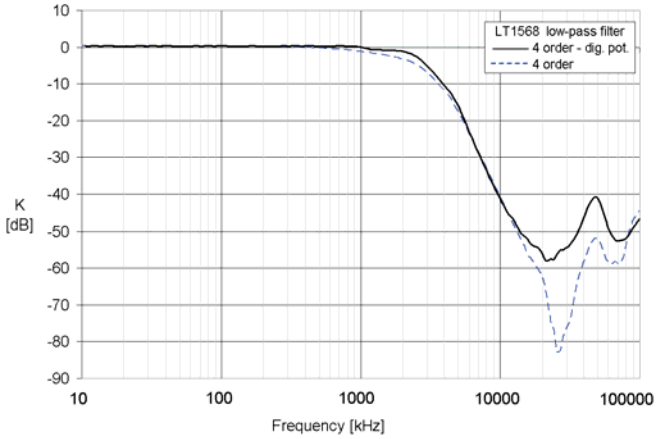

Fig. 19. Magnitude responses of LT1568 for 4th order filter configuration

This is due to the fact that we are using a smaller number of tap positions for each of the digital potentiometer. Specifically, the resistance of the first pair of digital potentiometers is 239 Ω (6 position used). The second pair of digital potentiometers have resistance 280 Ω (8 position used). This ensure more balanced frequency response at higher frequencies, see Fig. 16. More significant difference between the tuned f_{c3db} frequency is caused by tolerances of all four digital potentiometers. A simple calculation according to (8) shows difference about 212 kHz for actual measured resistance values of digital potentiometers under test. This value corresponds to the result of tolerance analysis in PSpice where the difference is 155 kHz for tolerance 10% for each digital potentiometers.

IV. Control Software

A universal application DIGIPOT for controlling digital potentiometers has been developed. The application supports three well-known types of the interfaces - I^2C, SPI and Up & Down, see Fig. 20. The user can also use built-in memory in most modern digital potentiometers and short commands to control multi-channel potentiometers. Of course, there is also support of daisy chain structure and addressing more potentiometers in a single bus. The application allows to select the number of positions and nominal resistance change. These aspects help to adapt software to the type of various potentiometers. The application communicates via USB [21] with the universal interface to control digital potentiometers. More details can be found in [11], [12]. The application is shown in Fig. 13. DLL library for communicating with the application DIGIPOT can be created based on [12], [22].

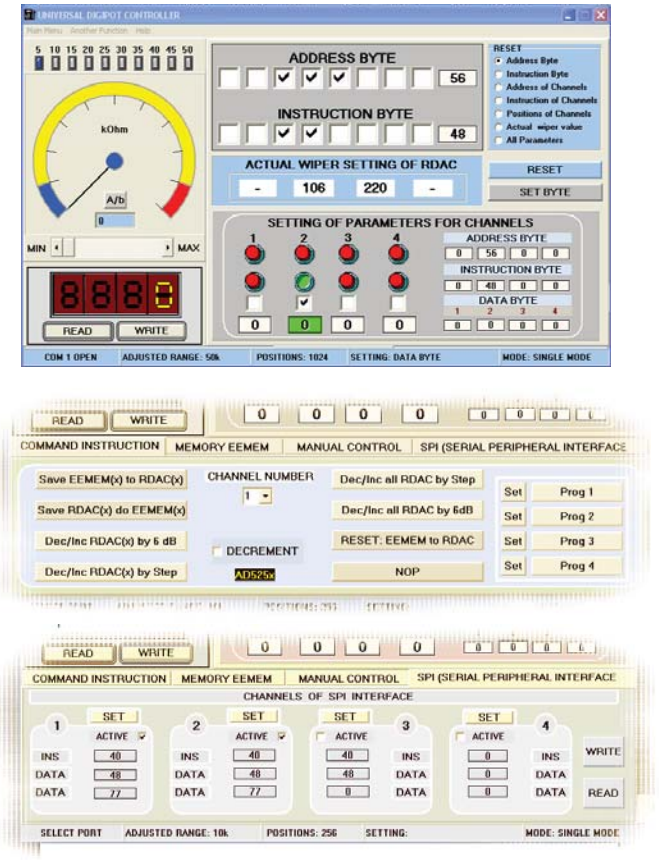

Fig. 20. Universal Control Software for digital potentiometers DIGIPOT

Two types of communication modes can be used. The first mode uses to display only the program on a computer. The second mode combines the use of computers and the communication interface to display potentiometers parameters. In this mode, the user can validate physically communication on the bus with built in LCD display. This will help to faster remove any communication problem. One of the possible measurement configuration, including the test board and vector network analyzer, is shown in Fig. 21.

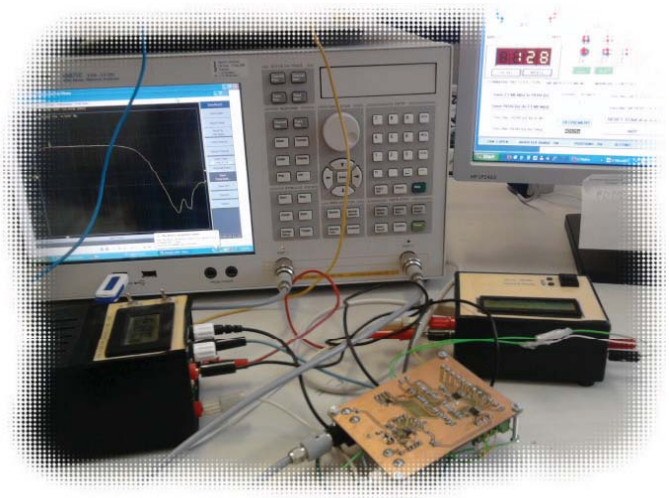

Fig. 21. Measurement configuration for digital potentiometer analysis

V. CONCLUSION

In this paper verification and validation processes of the new PSpice macro model for commercial IC Digital Potentiometers have been presented. It is obvious that it is possible with good accuracy to predict the impact of parasitic effects of the digital potentiometers in practical applications. Manufacturers of digital potentiometers generally indicate the value of parasitic capacity not only for the type of potentiometer but also separately for each nominal resistance of the same type. The model can therefore be adjusted according to actual values of parasitic capacitances and wiper resistances. Modeling the impact of parasitic capacitances on the achievable BW_{3dB} shows with good accuracy how to minimize parasitic effects. This allows the use of digital potentiometers for applications such as video. One way to achieve relatively good frequency bandwidth of digital potentiometers with high resolution is the use of multiple potentiometers with smaller nominal resistances and an easy and precise digital control. Other techniques such as minimizing impedance circuit presented in this paper help to stabilize the resistance set at frequencies above 1 MHz. This is valid for relatively straightforward implementations of digital potentiometers, but the bandwidth can be limited even more, if more complicated pot implementations are used. Practical measurements of universal programmable filter and LT1568 filter building block shows that digital potentiometers can be used for applications at frequencies above 1 MHz but with several limitations. First, it is necessary to eliminate impedance mismatches in the circuit with digital potentiometers, see the paragraph where parallel resistor string and high-speed buffer BUF634 are described. Furthermore, it si necessary to adjust the number of tap positions in use according to a current frequency response of digital potentiometer, see Fig. 16, Fig. 18 and Fig. 19. Very good frequency performance has TLP8002-25 digital potentiometer from Texas Instruments, which has stable characteristics at the frequencies to 10 MHz. Despite these drawbacks the use of digital potentiometers provides speedy and accurate multi retuning of resistance values, the possibility of easy calibration, quick configuration change to the immediate requirements for current application.

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