AMC Timing Receiver and Clock Synthesizer Module for the LLRF System

Krzysztof Czuba, Samer Bou Habib, and Dominik Sikora

***Abstract*—The new LLRF system architecture based on the ATCA platform was developed and tested at FLASH. The LLRF system require generation of highly stable clock and trigger signals for high precision data processing and synchronous system operation. This paper describes the conception, design and performance test results of the updated AMC module designed to fulfill the LLRF system timing synchronization needs. This module contains three independent clock synthesizers that are able to generate LVDS clock signals in the range of 10 MHz to 100 MHz. These signals are transmitted over the AMC connector and can be distributed over the entire ATCA crate. The clock synthesizers can be synchronized either by an internal quartz oscillator or an external phase reference signal provided to the board either via the AMC edge connector or via a front panel socket. This assures flexibility when using the board for tests and for the LLRF system operation. Besides clock synthesizers the AMC card contains also an optical receiver suited to convert and decode FLASH timing signals distributed in the FLASH accelerator system.**

***Index Terms*—Clocks; phase locked loops; timing jitter; ATCA**

I. Introduction

THE modern superconducting linear accelerator facilities such as the European XFEL use highly stable RF field for the acceleration of the electron beam. The field stabilization is performed by the LLRF system [1] including high performance RF and digital subsystems. The LLRF system must support acquisition and processing of more than 100 high frequency (1.3 GHz) measurement signals at each RF station of the accelerator. The scale of the LLRF control system, the data transfer rates, the number of implemented software applications, the required performance and finally, the required high availability and modularity lead to a decision that the xTCA standard [2] will be used as the main hardware platform for the XFEL accelerator. The "x" stands either for "μ" or for "A", respectively for μTCA and ATCA.

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The xTCA based LLRF system has been designed and the first prototype performance was evaluated at the FLASH accelerator [3]. Amongst multiple requirements fulfilled by the system architecture there are the modularity and high reliability. These requirements imply using modules of specified functionality. Minimum two modules of given type could be installed in one operating system in order to provide redundancy and thus, together with the intelligent ATCA platform management system, fulfill the high reliability requirements.

Most of the specified modules, like the ADC cards, CPU's and vector modulators require synchronization with another devices and with the measured RF signals. The overall RF stations synchronization in the entire accelerator is performed by the RF phase reference and timing distribution system [4].

In general, there are two types of synchronization signals: the phase reference (from the Master Oscillator (MO)) and the timing signals. The MO signal is an analog (harmonic) highly phase stable signal and is distributed by coaxial cables or analog optical fiber links. The phase reference signal is used for driving analog subcomponents of the LLRF system (like the vector modulator) and for generation of synchronous low jitter clock signals for the digital part of the system. The timing signal is a digital, coded signal carrying the information about triggers and various accelerator states like event codes and unique numbers for identification of e.g. pulse or electron bunch numbers.

Both the MO and the timing signals, provided to the xTCA crate should be split and distributed internally to all relevant devices. One of the most important components of the LLRF crate synchronization concept is an AMC timing receiver and clock synthesizer module (called further in this text the AMC-TM). The design and performance of the AMC-TM card is described in the remnant of this paper.

II. ATCA Based LLRF System Hardware Architecture

The ATCA based LLRF system is using a three-slot ATCA carrier board [5]. The design of the ATCA carrier (version 1) assumes, that the AMC-TM module can be installed in any of the AMC bays in the carrier board. Therefore there is a flexibility in using the AMC-TM. Furthermore, there can be two AMC-TM modules in one crate and in case of failure of one of them, the other functioning module can take over the generation of timing signals.

The conceptual hardware layout for the timing signal distribution is shown in Fig. 1. The AMC-TM localized in one of the AMC bays of the ATCA carrier generates clock and trigger signals. Those signals are distributed to the remaining AMC slots on the carrier board and over a custom Zone 3 Backplane to all other carrier boards present in the system. The hardware allows for bi-directional signal distribution, therefore the AMC-TM can be localized in any AMC slot at any carrier board in the crate.

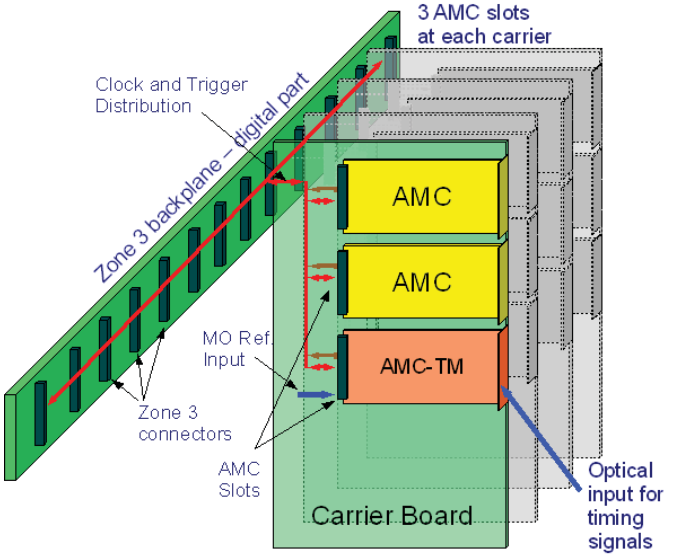

Fig. 1. The ATCA based LLRF system hardware conception with exemplary AMC-TM location and clock distribution scheme.

Due to various types of modules that can be installed in the system, the AMC-TM should generate 3 independent clock and 3 trigger signals. All these signals are distributed over the entire ATCA crate as shown in Fig. 1. The required maximum clock jitter value is 5 ps. The trigger signal jitter value is of low importance because the triggered events are of relatively low frequency and time precision of hundred of nanoseconds is sufficient for this application.

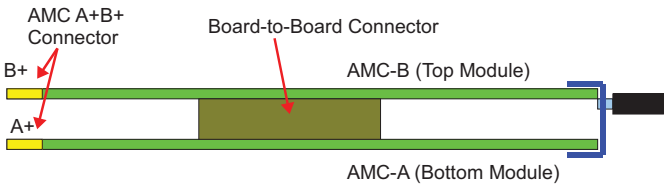

Fig. 2. The double PCB AMC module concept.

The LLRF system conception assumes installing full-size AMC modules composed of two Printed Circuit Boards (PCBs): the top module (AMC-B) [6] and the bottom module (AMC-A). General layout of such an AMC module is shown in Figure 2. The top module is an universal PCB containing all hardware components necessary for communications with the ATCA systems and specified digital I/O for controlling of the bottom module. The AMC-A can contain custom electronics (also analog) realizing given functionality for the system, e.g. a vector modulator. The top and bottom modules are connected by a universal connector used for transmission of differential signals and power supplies. One of the functional AMC-A modules is the AMC-TM board being the subject of this paper.

III. The Conceptual Design of The AMC-TM

The conceptual block diagram of the AMC-TM module is shown in Fig. 3. Schemes of both the AMC-A and the AMC-B PCBs are shown. The AMC-A construction is described in the following sections of this paper.

Two independent hardware parts can be distinguished in the AMC-TM hardware: the clock synthesizer circuits and the timing signal receiver.

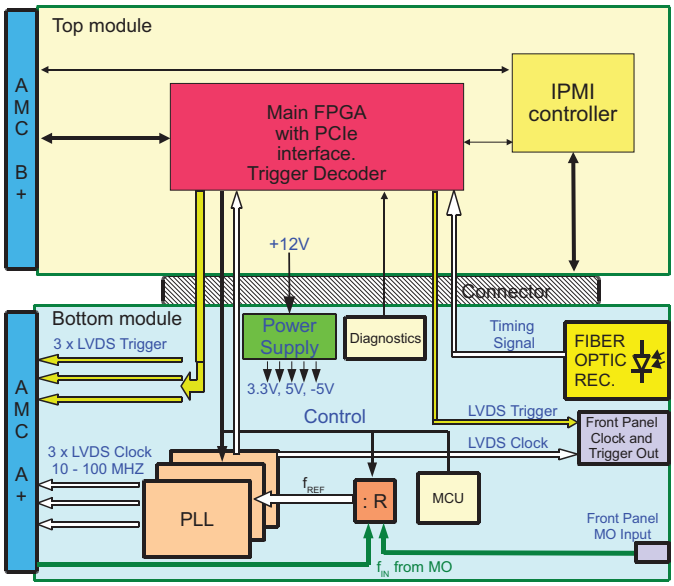

Fig. 3. The block diagram of the AMC-TM module.

The timing signal receiver uses a fiber optic receiver compatible with the FLASH accelerator timing system. The electrical signal obtained from the optical receiver is transmitted to the AMC-B card, where trigger decoding algorithms are implemented in the FPGA. Generated trigger signals are sent back to the AMC-A module and provided to the AMC edge connector and to the front panel differential output.

The clock synthesizer occupies most of the AMC-A board. The MO phase reference signal can be received either by the AMC-A+ edge connector or by a front panel connector. After passing a frequency divider circuit, the signal is provided to three independently controlled frequency synthesizers that can output LVDS clock signals in a frequency range of 10 MHz to 100 MHz. All synthesizers can be controlled either by the AMC-B module or by the on-board Microcontroller Unit (MCU).

Two modes of operation have been foreseen for the AMC-TM: a standard mode with the AMC-B and the ATCA system and a stand-alone mode, without the AMC-B and even outside of the ATCA crate. The module can easily be configured for the given mode of operation by switches and jumpers. In the

standalone mode, the MCU can configure the power supply system and the clock synthesizers. The MCU can not be used for decoding of the trigger signals but this is not required for the standalone operation of the board.

There are two benefits of the standalone mode of operation. The primary is for allowing the testing of the board and its performance in laboratory conditions, without the need for the complex top module. The other option is to allow the usage of the board as a stand-alone device for generating stable synchronized clocks to be used in other applications and experiments, e.g. synchronizing ADC evaluation boards. Moreover the evaluation of the module outside the ATCA crate can be used for comparing the performance of the crate clock distribution system with the stand-alone system, i.e. to obtain information about the clock degradation due to the AMC-B part operation and clock distribution through other parts of the noisy digital ATCA system.

The AMC-TM board incorporates also diagnostic circuits designed to monitor the temperature of the board, the availability of input signals, the board component status (like PLL locks) and the values of power supply voltage. The diagnostic information can be read out by the AMC-B card and used by the crate management software for fault detection and for switching between the redundant units during regular operation of the ATCA based LLRF system.

IV. Clock Synthesizer Circuit

The overall schematic of the frequency synthesis circuit is shown in Fig. 4. The input frequency divider and distribution chip can use signals provided either from the AMC edge connector or from the front panel of the AMC module. Additionally a highly stable on board crystal oscillator circuit can provide a reference clock in case when the MO signal is missing or when the ATCA crate is tested in the laboratory independently from the accelerator control system.

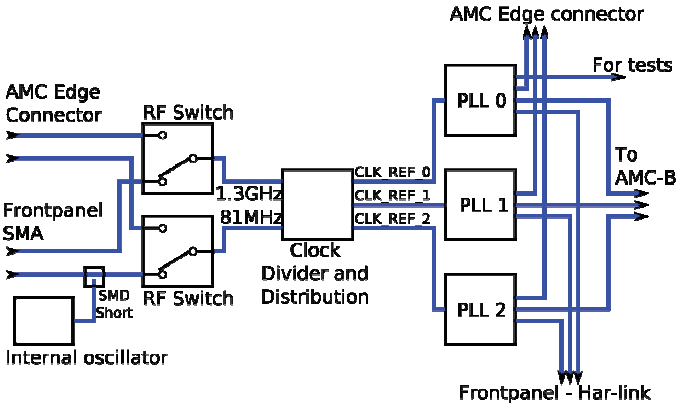

Fig. 4. Schematic of the frequency synthesis and distribution system.

Source of the input signals is selected by the RF switches or the SMD short. In the standalone mode both RF switches are set in default to transmission of the signals from the SMA connectors on the front panel. The frequency of the input signal is selected by programming the clock divider chip. This system allows to provide signals with frequencies up to 1.6 GHz. The internal oscillator signal can be connected by an SMD jumper when RF switches are in the default transmission mode.

The frequency divider chip with fanout and differential outputs was selected to be able to drive three clock synthesizer chips simultaneously. The MO signal frequency is divided to a value acceptable for the PLL synthesizer reference input (below 250MHz). Each of the clock outputs of the clock distribution chip has its own frequency divider. It is possible to divide input signal frequency by an integer value in the range of 1 to 32. The dividing ratio of 1 can be set when divider bypassing is required.

Each of the PLL chips has output clock fanout. Output signals from each PLL are provided in parallel to the front panel Har-link connector, to the AMC-B module and to the ATCA carrier by the AMC edge connector. Additionally one of the PLL0 outputs is connected to on-board SMA connectors for laboratory tests.

The clock outputs of each PLL chip can be configured either as an LVDS differential pair or as a pair of CMOS single-ended lines. In the ATCA LLRF system they are configured to the LVDS standard. The LVDS output polarity can be set as non-inverting or inverting, which allows for the adjustment of the relative polarity of outputs within an application without the need for a board layout change. The synthesizer circuit allows also for phase adjustments of the clock signals.

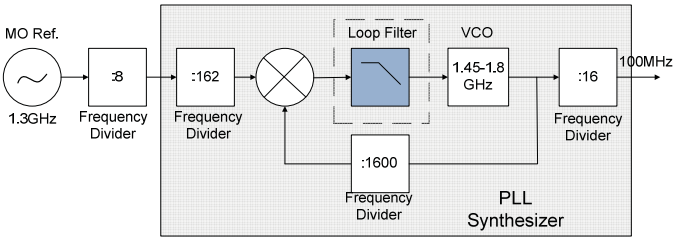

Fig. 5. Block diagram of the clock signal synthesizer (one channel).

The block diagram for signal distribution for one PLL clock synthesizer channel is shown in Fig. 5. Example divider settings for 1.3 GHz input frequency and 100 MHz output clock frequency are shown in the figure. The required clock frequency range is 10 MHz to 100 MHz with 1 MHz step but designed architecture allows for generation of signals in much broader frequency range with fine resolution and also fractional ratios to the input frequency value. The complex synthesizer chip uses an internal 1.6 GHz VCO (1.45-1.8 GHz), which allows for a very broad range of configurations and very flexible selection of the output frequency value. It is possible to divide the internal VCO signal by a factor ranging from 2 up to 6144, so signals with frequencies from 900 MHz down to 236 kHz can be obtained.

V. Timing Receiver Details

The timing signal receiver block diagram is shown in Fig. 6. The receiver was divided into an analog and digital parts. The analog part, located on the AMC-A module, contains the optical receiver which converts the optical signal received by the optical fiber to an electrical signal which is amplified and provided to a comparator circuit. The latter one forms a CMOS compatible signal which is sent to the digital part located on the AMC-B module. The CMOS standard was selected for this signal because of limited electrical performance requirements there is no need to use differential signal transmission. The 9 MHz frequency CMOS signal carries serial manchester coded telegrams with timing event information. Algorithms implemented in the FPGA on the AMC-B module are used to decode up to three various event triggers. The trigger frequency can vary from 0.1 Hz to 10 Hz. As described above, the decoded trigger signals are transmitted back to the AMC-A via the board-to-board connector and further to the ATCA carrier board and to the front panel connector.

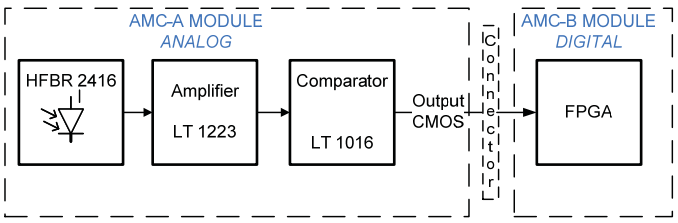

Fig. 6. Block diagram of the timing signal receiver part.

VI. The MCU

As described above, the microcontroller unit allows for the synthesizer part configuration without the use of the AMC-B module. The microcontroller uses an 8051-based single core that works on a frequency of 12.58 MHz. This device supports UART, SPI and I^2C interfaces. The UART connected to an on-board RS-232 interface chip allows programming of the AMC-TM device from a PC and then, during normal operation, to communicate with the board and change the settings of the components. The MCU can also be programmed for automatic configuration of frequency synthesizers depending on the output frequency value provided by user from the PC computer. The frequency divider and the three clock synthesizer chips are programmed through the second interface (SPI), thus allowing full control of the clock-generation system. The MCU is also a power management module that can enable and disable most of the power-supply components on the board, allowing it to turn off unused blocks.

VII. Power Supply

The power supply block diagram is shown in Fig. 7. The main voltage supply 12 V is provided from the AMC-B module via the board-to-board connector or via an on-board socket for the standalone operation mode.

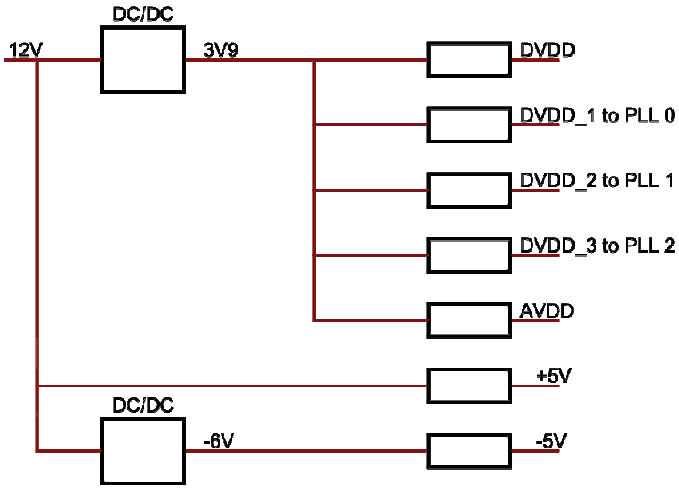

Fig. 7. Block diagram of the power supply circuit.

The 12 V voltage is converted to 3.9 V by the main DC/DC voltage regulator. Further, five linear low dropout regulators are used to obtain 3.3 V DVDD supplies for critical components of the system. Such number of voltage regulators assures good isolation between chips and better noise performance. The optical timing signal receiver parts are powered by +/-5 V voltage supplies.

The voltage regulators are controlled by the AMC-B or by the MCU in the stand-alone mode. After powering the AMC-TM on, the voltage regulators are in the power down mode. Later, the FPGA from the AMC-B or the MCU can activate them for normal operation. In the standalone mode the main DC/DC regulator (3.9 V) must be activated by an SMD jumper in order to supply the MCU for startup. The possibility of software controlling of the power supply system is required for the Intelligent Platform Management System of the ATCA crate and allows for reduction of supply power by switching off unused devices.

VIII. PCB Design

An eight-layer PCB was designed for the AMC-TM card. Signal integrity techniques were applied in order to assure the high performance of the clock signal. Low loss and improved quality substrate (comparing to the standard FR4) was selected for the circuit. Precise track routing and differential pair equalization were performed in the areas where clock signals are distributed. The RF transmission line routing, impedance matching and RF grounding techniques were used for distribution of the 1.3 GHz MO signal. Complex power supply network was used with separate low noise voltage regulators supplying each sensitive device on the board. Through this a good isolation between board sub-circuits and also interference suppression from the digital AMC-B was achieved.

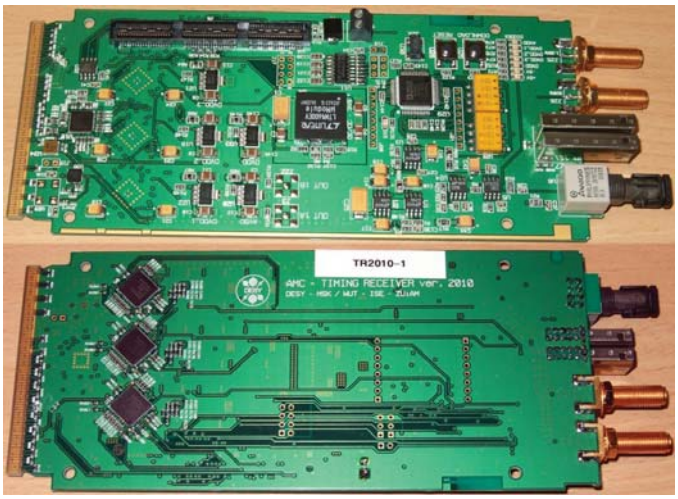

Fig. 8. The assembled AMC-TM card.

Multiple test points and configuration components were foreseen in the board in order to make possible extensive tests of the board performance in laboratory conditions. The pictures of designed device are shown in Fig. 8. More detailed description of the conception and the hardware prototype design can be found in [7].

IX. Performance Tests

Extensive laboratory tests have been performed on the clock synthesizer circuits [7]. As it was described in the section IV, there is very large flexibility in setting up of the output frequency value of the PLL synthesizer. Unfortunately, the clock jitter value strongly depends on the frequency of the signals provided to inputs of the PLL phase detector (so called comparison frequency) and also on the phase noise levels of the input signal from the Master Oscillator. In general the higher the phase detector frequency, the higher the jitter performance. Furthermore, the jitter value, at given comparison frequency depends also on the loop filter parameters and on the output frequency value. The AMC-TM architecture allows for fixing the comparison frequency value and still fulfilling the tuning range and step requirements. By this the loop filter bandwidth can be fixed and divider settings determined for the best clock signal performance. This requires significant complexity of the synthesizer control software.

Simulations were performed where various comparison frequency values were investigated along with the loop filter parameters in order to find relationships between jitter values and synthesizer settings. It was found that there is an optimum loop bandwidth for a given comparison frequency. The simulations results were confirmed by measurements performed in laboratory conditions. The Signal Source Analyzer device was used for clock jitter measurements. Jitter was measured at the on-board test output.

First clock jitter performance evaluation was performed at the comparison frequency of 1 MHz. This is the highest possible frequency value for the required 1 MHz clock frequency step when covering the required frequency range from 10 MHz to 100 MHz. The reference signal was provided from a laboratory signal generator. Measurement results are shown in Table I. The jitter values of over 7 ps were measured for the loop bandwidth of 5 kHz. For 16 kHz, there is an optimum and excellent jitter values of below 1 ps have been achieved. When increasing the loop bandwidth, the jitter values increase again.

Table I
The Measured Phase Jitter Values in ps for the Comparison Frequency of 1MHz

Loop Filer Bandwidth [kHz]	Clock Frequency		
	20 MHz	*51 MHz*	*99 MHz*
5	7,07	7,11	7,33
16	**1,32**	**0,93**	**0,97**
100	1,77	1,59	1,64

Further tests were performed during preparation for the ATCA based LLRF system evaluation. In order to find jitter performance limits, the comparison frequency was increased to 40.625 MHz. The output frequency step size was limited by this change, but the clock frequency value of 81.25 MHz used during LLRF system demonstration was generated. The extremely low phase noise 1300 MHz signal from the FLASH Master Oscillator was connected to the AMC-TM input and a new loop filter with bandwidth of 500 kHz was designed for this particular test.

Table II
The Measured Phase Jitter Values in ps for the Comparison Frequency of 40.625MHz

Loop Filer Bandwidth [kHz]	Clock Frequency			
	20 MHz	*51 MHz*	*81 MHz*	*99 MHz*
500	0.387	0.354	0.324	0.386

The output clocks were again analyzed with the signal source analyzer with a setting of 100 correlations in order to remove from the measurements the noise of the SSA itself. The measurements were performed with the module inside the ATCA crate with the ATCA power supply, but without the AMC-B control and the measured signals were derived directly from the module test output. The results of the measured phase jitter values are collected in Table II. The example measurement screen-shot is shown in Fig. 9.

The excellent measurement results of less than 324fs fulfill the requirements of the project with great reserve, but the jitter can be significantly affected by the distribution within the ATCA carrier board and over the Zone 3 Backplane. This is an issue exceeding the scope of this paper but such tests are planned.

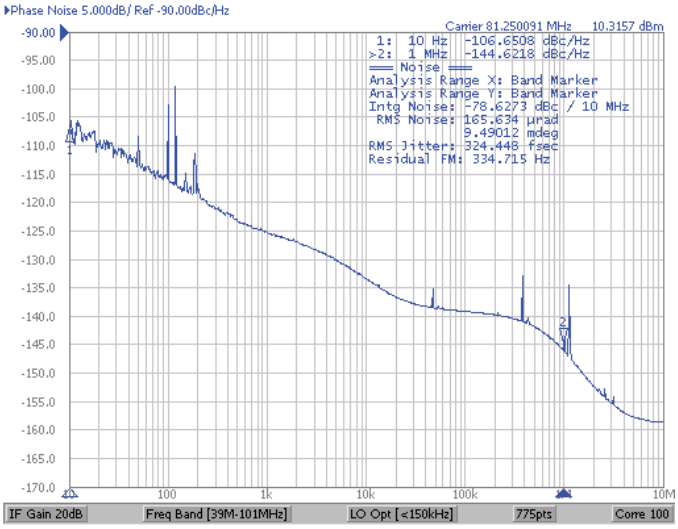

Fig. 9. Phase noise and clock jitter measurement results at 81 MHz clock signal generated with the 1.3 GHz MO input signal and optimized PLL filter parameters.

X. Summary

The conception and design of the AMC clock synthesizer and timing receiver board is described. The eight-layer PCB provides the possibility of synthesizing three low jitter independently programmable clock signals. It also allows for receiving and decoding of the optical trigger signals from the FLASH accelerator timing system. Together with the AMC-B module, the designed board allows for fulfilling the timing requirements of the ATCA based LLRF system. The system availability is supported by extended diagnostic capabilities implemented in the board where the system components state, the availability of input signals and the board temperature can be read out and sent to the ATCA management software. The measured excellent clock jitter values show that the design and board configuration was performed correctly. Further plans foresee extensive performance tests of the board installed in the operating ATCA system.

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During the summer 2001 he worked for the ZF-Luftfahrttechnik in Kassel-Calden, Germany, where he designed an on-flight strain measurement system for helicopters main rotor. He worked as a Satellite Telecommunication Network Operator for Polish Phonesat in Warsaw during 2002. In 2006 he started working for the Warsaw University of Technology in the Microwave Circuit and Instrumentation Division, where until now, he holds an Assistant Professor position. He supervised in total 8 B.S theses and 6 M.S. theses. He published about 15 conference and journal papers. Since 2002 he is a member of a scientific cooperation between the Institute of Electronic Systems and the German scientific institute DESY from Hamburg. Within this cooperation he developed multiple electronic devices for high energy particle accelerators.

Dr. Czuba received first award from the AP/AES/MTT Joint Chapter of Polish IEEE Section for the best M.S. thesis in the contest organized at the MIKON 2004 conference. He also received first class honors from the vice chancellor of the Warsaw University of Technology for his Ph.D. thesis.

Samer Bou Habib was born in Warsaw, Poland in 1985. He finished his Bachelor of Sciences degree in the field of electronics engineering at the Warsaw University of Technology in Warsaw, Poland in 2008. Then on the same university he acquired his Master of Sciences degree also in the field of electronics engineering in 2010.

Since 2010, he is now PhD. Student at Warsaw University of Technology, working in collaboration with DESY institute in Hamburg. Recently, he has published an article for the Mixdes conference in Wroclaw, Poland in 2010 under the title of "Design of Eight-channel ADC Card for GHz Signal Conversion". The paper concerns his main work on the project for direct sampling of high frequency signals for the European XFEL which is his field of study.

Dominik Sikora was born in Radom, Poland in 1983. He received his B.S. and M.S. degrees in the field of electronics engineering at the Warsaw University of Technology, Institute of Electronic Systems, Poland in 2008 and 2010 respectively.

After graduating Master's degree he is now Ph.D. student at the same university. He is collaborating with the DESY institute in Hamburg, Germany. He is co-author of article for the MIKON conference in Vilnius, Lithuania in 2010 under the title of "Phase drifts versus temperature measurements of coaxial cables".