Thermal Assisted Switching Magnetic Tunnel Junctions as FPGA Memory Elements

V. Silva*, J. R. Fernandes*, L. B. Oliveira†, H. C. Neto*, R. Ferreira‡, S. Freitas#, P. P. Freitas#
*INESC-ID / IST / UTL, Technical University of Lisbon, Portugal
Email: {victor.silva, jorge.fernandes, horacio.neto}@inesc-id.pt
†INESC-ID / FCT / UNL, New University of Lisbon, Portugal
Email: l.oliveira@fct.unl.pt
‡INESC-MN, Portugal
Email: rferreira@inesc-mn.pt
#INESC-MN / IST / UTL, Technical University of Lisbon, Portugal
Email: {sfreitas, pfreitas}@inesc-mn.pt

***Abstract*—This paper presents our research and development work on new circuits and topologies based on Magnetic RAM for use as configuration memory elements of reconfigurable arrays. MRAM provides non volatility with cell areas and with access speeds comparable to those of SRAM and with lower process complexity than FLASH memories. The new memory cells take advantage of the Thermal Assisted Switching (TAS) writing technique to solve the drawbacks of the more common Field Induced Magnetic Switching writing technique. The CMOS circuit structures to implement the main components for reading and writing the MTJ cells have been developed, characterized and evaluated. A scaled down prototype of a coarse grain reconfigurable array that employs the TAS-MRAM elements as configuration memory has been designed and electrically simulated pre- and post- layout. The results obtained for all the circuit elements, namely the storage cells and the current generators, indicate that the new configuration memory cells can provide a very promising technological solution for run-time reconfigurable hardware devices. The prototype has been manufactured using a standard process 0.35µm 4-Metal CMOS process technology and should be under test in the foreseeable future.**

***Index Terms*—MRAM, MTJ, Writing schemes, FIMS, TAS, STT**

I. INTRODUCTION

Most FPGA are static RAM (SRAM) based and thus they are volatile, in other words, each time power is off, the FPGA configuration is lost and has to be setup at each power-up. To avoid this drawback a non-volatile Programmable Read Only Memory (PROM) module is usually required [1]. This not only increases the start-up time, the total device cost and the PCB area required but can also be a security concern since it is quite easy to tamper with an external memory.

Internal FLASH memory has been used by some manufactures on some of their products [2] [3] to deal with the volatile nature of SRAM based FPGA, but FLASH memory has its own drawbacks such as slow reprogramming, limited number of writing cycles and a significant increase in manufacturing costs due to the number of extra steps and the area overhead needed to implement FLASH memory.

Magnetic RAM (MRAM) based technology allows the same non-volatility of FLASH memory, with lower writing and reading times, virtual limitless re-programmability, a much cheaper manufacturing process, due to the lower number of extra steps required to implement the Magnetic Tunnelling Junction (MTJ), and a potential higher functional density, since MTJ are laid over the CMOS and thus there is no area overhead. Table 1 compares these characteristics for the different memory technologies [4].

TABLE I. COMPARISON OF DIFFERENT MEMORY TECHNOLOGIES

Memory Technology	DRAM	FLASH	SRAM	MRAM
Cell structure	1T/Cap	1 FGT	6T	1T MTR
Cell size (130nm u^2)	0,14	0,2	0,65	0,34
Write Energy	< 200pJ	~200pJ	< 100 pJ	< 100 pJ
Endurance	∞	1,00E+06	∞	1,00E+14
Acess Time	~ 50ns	~ 50ns	5 - 10 ns	~ 30ns

This paper addresses the design of a recently proposed Thermal Assisted Switching (TAS) MRAM cell to be used as a configuration memory element in the context of reconfigurable computing. This type of MRAM solves many of the drawbacks of the first generation of MRAM cell as explained in further detail in sections 2 and 3. In section 4 a top down in-depth explanation of the implemented TAS-MRAM cell is given. The CMOS circuits have been designed and implemented in full custom using the Austria Microsystems (AMS) 4 metal 0.35µm CMOS process, and the first samples have just been received. The back end fabrication of the nanometric TAS-MRAM junctions, over the CMOS wafer, will now be carried out at INESC-MN.

Copyright © 2010 by Department of Microelectronics & Computer Science, Technical University of Lodz

II. MRAM Basic Principles

The most common MRAM cells consist of Magnetic Tunnelling Junctions (MTJ) vertically integrated with silicon CMOS transistors. MTJ are fully compatible with classical CMOS processes, and require only a few additional steps after the standard CMOS process (Fig. 1).

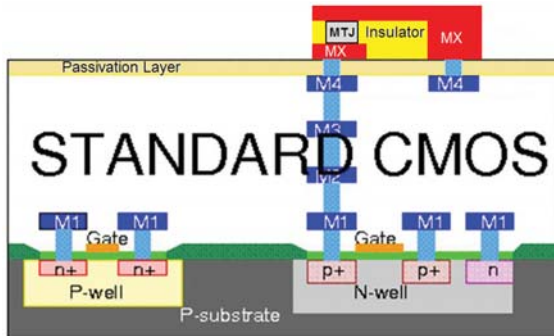


Fig.1. MTJ requires a few steps above standard CMOS

A MTJ is conceptually made of two thin ferromagnetic layers separated by an ultra thin non-magnetic oxide layer (Fig. 2). The relative magnetic orientation of these layers is employed to store information.

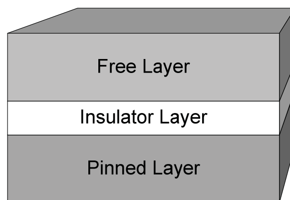


Fig.2. Magnetic Tunnel Junction Structure

One layer's magnetic orientation is pinned and used as reference while the other one is free and can be changed during the functioning of the memory. The relative magnetic orientation of the two layers exhibits two different values of resistance.

The ratio between these two resistances (R_{AP} and R_P) is characterized by the Tunnelling Magneto Resistance (TMR), which is defined as:

$$TMR = \frac{\Delta R}{R} = \frac{(R_{AP} - R_P)}{R_P}$$

Both the TMR and the resistance-area product (RxA) turn to be extremely critical for the MRAM.

Those two values of equivalent resistance can be employed to represent the logic states “0” and “1”. The magnetic remanence of the ferromagnetic elements provides for the non-volatility.

The resistance can be evaluated by sending current through the junction and measuring the voltages at the nodes of the MTJ. A structure is required to determine whether the junction is on the low resistivity configuration or in the high resistivity configuration.

The resistance of the MTJ depends on the area of the MTJ, the thickness of the oxide layer and is also dependent on the voltage applied to the junction. Thus, the current is a non-linear function of the voltage.

To write information in a MTJ the relative orientation of the ferromagnetic layers must be manipulated. Currently, there are 3 alternative writing approaches, known as Field Induced Magnetic Switching (FIMS) [4] [5], Thermally Assisted Switching (TAS) [6] [7] and Spin Transfer Torque (STT) [8].

Despite FIMS earlier success, this technique has major drawbacks, as explained below, such as its susceptibility to soft errors due to write selectivity, its lower scalability and its high current consumption.

In the FIMS approach an external field is created by the vector sum of 2 magnetic fields created by 2 currents that flow across 2 orthogonal wires. The basic principle of this technique is that the only bit that will be programmed is the one in the intersection of the orthogonal wires where there are currents flowing, while the others will be left undisturbed. Unfortunately, due to the statistical switching field distribution, a perfectly selective writing becomes a practical impossibility, leading to writing errors. Furthermore, the demagnetizing fields increase with the memory density and the current needed to write increases as well. The number of bits that can be packed with a reasonable current consumption is therefore limited.

The above mentioned shortcomings have been the driver for the development of the so called second generation writing techniques, the STT and the TAS.

The STT [9] approach does not need an external magnetic field since the same effect is accomplished by driving a current (bidirectional) polarized by magnetization in the pinned layer. The concept has been demonstrated [10] but, although it solves the selectivity problems of the FIMS-MRAM, it requires write currents below 0.1 mA to remain competitive with flash memories. This can only be achieved with deep sub-micron elements with low RxA product ($< 1\ \Omega\ \mu m^2$) and high tunnel magnetoresistance (TMR) signals (> 30%).

III. The TAS-MRAM Approach

A TAS-MRAM MTJ extends the basic MTJ structure, besides a high blocking temperature and high exchange antiferromagnetic layer pinning the reference layer there is also a low blocking temperature and low exchange antiferromagnetic layer soft-pinning the storage layer (Fig.3).

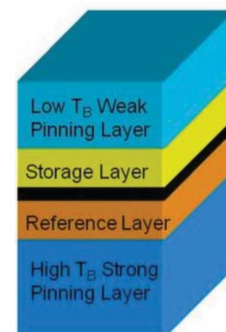


Fig. 3. TAS-MRAM MTJ structure

The TAS approach requires one bidirectional current to create a non-local magnetic field. A local current (for each junction) is then used to heat the soft-pinning anti-ferromagnetic layer exchange coupled to the storage ferromagnetic layer. If the temperature is risen above the soft-pinning layer blocking temperature, the storage layer becomes unpinned. The pinning direction will be re-defined during cool-down by the direction of the non-local magnetic field. As a result, the transfer curve centre is shifted with respect to zero field, where the MTJ can either be in a high resistance or low resistance state depending on the relative orientation of the ferromagnetic layers (Fig. 4).

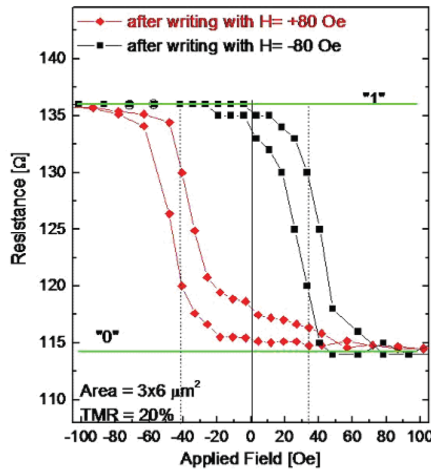


Fig. 4. Resistance versus external magnetic field of a TAS-MRAM MTJ in two possible electrode configurations

The high blocking temperature and high exchange antiferromagnetic layer strongly pins the reference ferromagnetic layer, while the low blocking temperature and low exchange antiferromagnetic layer weakly pins the ferromagnetic storage layer.

The element state can be determined by sensing the resistance level in the absence of a magnetic field, in a reading scheme similar to any other MRAM cell.

In order to switch the storage layer orientation, a two step process is used. First, a large writing current pulse is used to heat the MTJ pillar. If the current pulse has enough power to raise the temperature of the MTJ pillar above the blocking temperature of the weak pinning layer, then the storage layer will become free and can be switched using an external magnetic field. This blocking temperature varies between 110º and 150º C, depending on the junction manufacturing process. Once the current pulse reaches its end, the element starts cooling and the exchange coupling at the weak antiferromagnetic / storage ferromagnetic interface will be restored. Since an individual element can only be switched by an external magnetic field if it has been previously heated, there are no write selectivity issues in the write operation even when the field is non-local.

Using the Write Power Density (PW) obtained experimentally in micron-sized structures, together with the MTJ resistance-area product (RxA), and the junction pillar area (A) as inputs it is straightforward to calculate the write power requirements of an actual TAS-MRAM cell.

Actual measurements of the power required to switch micron-sized MTJ cells as reported at [11] show that TAS DC write power density required to switch these structures can be as low as 1mW/μm^2, therefore the initial value for the Write Power Density is set to 1 mW/μm^2. A pessimistic hypothesis where the thermal barriers would not prevent the heat from flowing away faster in sub-micron elements was also included by considering a power density increase by a factor of 10 with respect to the measurements performed in micron sized MTJs. Table 2 shows the calculations performed for 100x100nm^2 elements.

TABLE II. WRITE POWER REQUIREMENTS OF 100X100nm^2 ELEMENTS

Power Density (mW/um2)	RxA (Ohm/um2)	Resistance (Ohm)	Pulse Current (mA)	Pulse Voltage (mV)	Current Density (A/cm2)
1	1	100	0,316	32	3,16E+06
1	10	1000	0,100	100	1,00E+06
1	40	4000	0,050	200	5,00E+05
10	1	100	1,000	100	1,00E+07
10	10	1000	0,316	316	3,16E+06
10	40	4000	0,158	632	1,58E+06

Consequently the current pulse amplitude required to switch a 100x100 nm^2 MTJ cell is equivalent to a current density between 3.16x10^6 A/cm^2 (for a barrier of 1 Ω μm^2) down to 5.00x10^5 A/cm^2 (for a barrier of 40 Ω μm^2).

In any case, these values are very competitive when compared to those obtained with Spin Transfer. In most of the conditions considered, the current density across the MTJ element should stay in the 10^6 A/cm^2 range (competitive with Spin Transfer Torque switching) and in some of them, write currents of 0.1mA or below are even possible.

Furthermore, these power requirements do not depend on the tunnelling current polarization and are not affected by the demagnetizing field effect on nano-sized pillars, which is not the case in STT switching. For this reason, TAS based MTJ cells are far less demanding from a deposition point of view and therefore more appealing from the manufacturing point of view than STT.

For both FIMS and TAS, the wire(s) that carry the current(s) for the external(s) magnetic field(s) do not touch the MTJ but are placed as near as possible to the junction to minimize the losses on the magnetic field(s).

IV. TAS-MRAM BASED STORAGE CELL

A main objective of this work is to validate the potential of TAS-MRAM as a viable alternative to either SRAM based FPGA or FLASH based FPGA memory elements. Therefore, the work has focused on the development of a TAS-MRAM based storage cell that will form the basis of the programmable memory for reconfigurable arrays.

The distributed nature of the memory in reconfigurable computing applications imposes that the sensing structure has to be much simpler than in a standard MRAM memory.

Therefore, the MRAM cell employed in this work uses a pair of MTJ programmed in complementary fashion to store information, instead of the more common 1T1MTJ employed in standard MRAM [12]. The use of two complementary MTJ per bit simplifies the sensing circuitry required to read the data stored in the MTJ pair and improves the robustness of the sensing circuitry by decreasing the importance of the process variations of the magnetic junctions.

Two circuit architectures, following those proposed in [6] [7] have been evaluated as candidates for the TAS-MRAM based storage cell. These circuits are shown in Fig. 5 and Fig. 6 and consist of:

- An Unbalanced Flip Flop used as a sense amplifier.
- Two MTJ cells, MTJ1 and MTJ2.
- Two unidirectional current sources that are responsible for the Joule effect on each MTJ (active when a Write signal is applied). These are represented by the two sets of CS1/S1 and CS2/S2, in architecture 1, and by the NMOS transistors MN4 and MN5, in architecture 2.
- A write line that is employed to propagate the external magnetic field in either direction. For this prototype this line is common to all storage cells. This line is driven by a shared bidirectional current generator similar to the ones presented at [4] [5].
- Two PMOS isolation transistors (for architecture 2).

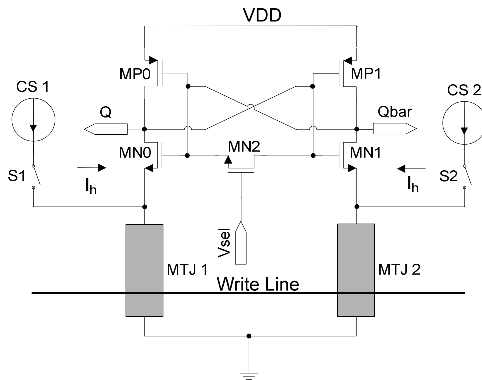


Fig. 5. TAS-MRAM based storage cell (Architecture 1)

Both architectures were implemented and simulated pre and post-layout. For that purpose the MTJ were simulated by the electrical model explained in sub-section A. All blocks were tested in 3 possible situations: write cycle, read cycle and idle cycle.

Due to the implementation of the bidirectional current generator responsible for the external magnetic field, as further detailed in sub-section D, the writing cycle is roughly divided into 2 phases. In the first phase, all cells which will be written with a logic ‘1’ turn on their respective unidirectional current generators for the time required by the junctions to reach the blocking temperature, while the external magnetic field responsible for writing a logic ‘1’ will be kept on until the junctions have cooled down. In the second phase, all cells which will be written with a logic ‘0’ will turn on their respective unidirectional current generators for the time required by the junctions to reach the blocking temperature, while the external magnetic field responsible for writing a logic ‘0’ will be kept on until the junctions have cooled down. The duration of the Joule effect pulse and of the two phases of the external magnetic field are process dependent.

In the read cycle, the CMOS latch converts the information stored in the MTJ into its equivalent electrical voltage (VDD and 0V) when triggered by a Vsel/Read signal. This new information is retained until a new read cycle is started even if one of more write cycles occur in between.

In the idle cycle both the information stored in the CMOS latch and in the MTJ are left undisturbed. Nonetheless, it is important to notice that the information stored in the couple of MTJ is non-volatile while the information stored in the CMOS latch is still volatile. The effect of the isolation transistors in architecture 2 (MP2 and MP3) is to avoid any parasitic current in the CMOS latch during the write cycle.

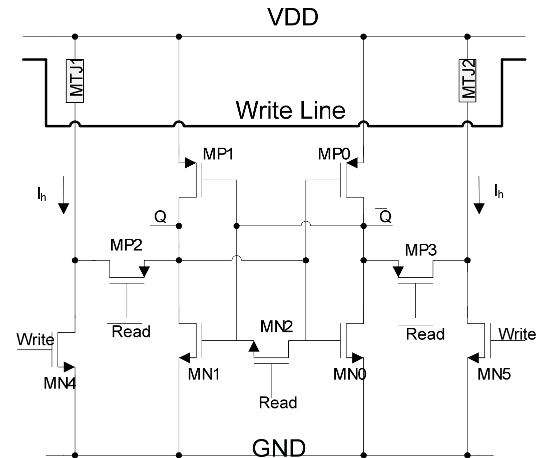


Fig. 6. TAS-MRAM based storage cell (Architecture 2).

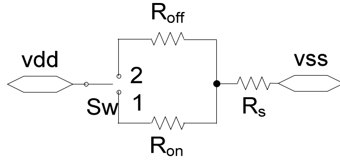
Architecture 1 has been preferred over architecture 2 because it requires a lower TMR. According to post-layout simulation results for the target CMOS 0.35 micron technology, architecture 2 requires a TMR of at least 40%, while architecture 1 requires a TMR of 30%. On both cases the value of Rp has been set to 1KΩ. Hence, the following discussion will be focused at architecture 1.

A. MTJ electrical model

The functioning of the storage cell depends on the electrical behaviour of its MTJ elements. For that purpose a SPICE compatible electrical model for the MTJ was developed. Since our application relies only on the TMR it is necessary to model the static resistive response of the MTJ.

This electrical model consists of a non ideal voltage controlled switch (SW) in series with a resistance (Rs) as depicted on Fig. 7. The switch on resistance (Ron) is set with the value of 1Ω, while the switch off resistance (Roff) is given by (TMR × Rp) + 1 Ω. The Rs resistance is Rp - 1 Ω. This

scheme is necessary to overcome the inherent limitation of most SPICE alike simulators when dealing with a voltage controlled switch that has its Ron parameter set to null.



Fig, 7. MTJ equivalent electrical model

B. Unbalanced Flip Flop

The Unbalanced Flip Flop (UFF) is a small and stable structure that is being used as a sense amplifier or CMOS latch. This structure (architecture 1) consists of two cross-coupled inverters (transistors MP0, MP1, MN0 and MN1) and one switch (transistor MN2).

The UFF depends for it functioning on the existence of the two MTJ polarized in complementary fashion. During the read phase, the MN2 NMOS transistor acts as a short circuit, thus, the two cross-coupled inverters are pulled to a meta-stable operating state. The resistance value of each of the MTJ will move away the meta-stable operating point from one of the stable states and bring it closer to the other. So, when the Vsel/Read signal is released, the structure will move to the closest stable state. Afterwards, new information can be stored into the MTJ without altering the value stored in the UFF.

The circuit behaviour was simulated with a large set of Monte Carlo runs in order to check its reliability and make the necessary adjustments. As a result of this analysis, the width and the length of the UFF transistors have been increased to 4.0µm and 3.5µm, in order to reduce the mismatches between the transistors [13]:

$$\sigma(P) \propto \frac{1}{\sqrt{W \times L}}$$

Finally, the layout was improved by adding 4 NMOS dummy transistors and 2 PMOS dummy transistors. This procedure ensures that the transistors at the UFF see the same surroundings.

C. Unidirectional current generator

As discussed in section 3, the value of the unidirectional current generator depends on several process related parameters. The current process allows choosing one set among the several options in table 3, where I_w corresponds to the Joule current, R corresponds to the parallel equivalent magnetoresistence, V_{break} is the junction breakdown voltage, V_w is the voltage at the MTJ due to I_w and a fixed TMR of 30% is considered.

TABLE III. MTJ ‘Writing Currents Specs

R	I_w	V_w	V_{break}
100Ω	316µA-1mA	31mV-100mV	250mV
1kΩ	100µA-316µA	100mV-316mV	400mV
5kΩ	44µA-140µA	220mv-700mv	900mV

These values are set by the Write Power Density (PW) obtained experimentally in micron-sized structures and by the MTJ resistance-area product.

A unidirectional current generator capable of delivering at least 1mA was developed.

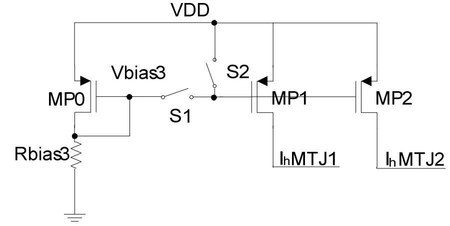


Fig. 8. TAS Current generator

The unidirectional current generator (Fig. 8) is split into a front- end and a back-end. The Front-end is made of a resistance (Rbias3) and a PMOS transistor (MP0) while the back-end is made of switches (S1 and S2) and two identical PMOS transistors (MP1 and MP2). The switches are implemented with PMOS/NMOS pass transistors.

The front-end is shared among the whole set of unidirectional current generators while there is one back-end module associated with each memory cell pair of MTJ.

Rbias3 is an external resistance that is employed to bias the back-end's driver transistors (MP1 and MP2). The switches S1 and S2 operate in complementary fashion. Their purpose is to turn on and off the PMOS driver transistors (MP1 and MP2). They are opened and closed depending on the value of an internal generated digital control signal (WriteCtl). When WriteCtl is set to logic '1' then switch S1 is closed while S2 is opened, hence both PMOS transistors MP1 and MP2 will form a current mirror with the external resistor Rbias3 and the PMOS transistor MP0. When WriteCtl is set to '0' switch S1 is opened while switch S2 is closed, so both PMOS transistors MP1 and MP2 will be cut off. The WriteCtl signal is a function of the current writing phase, as defined in section 3, and the input data.

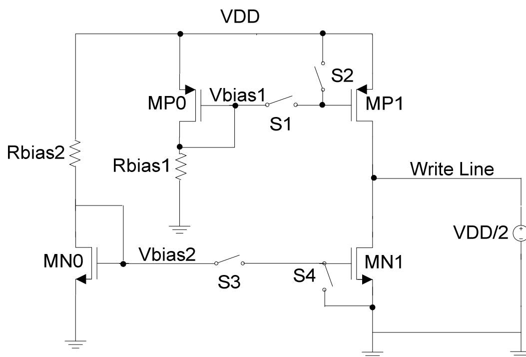
D. Bidirectional current generator

As aforementioned, the TAS writing approach uses a bidirectional current to create the external magnetic field that is necessary to change the magnetic orientation of the MTJ free layer. For that purpose a bidirectional current generator capable of delivering a current in the order of |20| mA was developed.

The bidirectional current is shared among all TAS-MRAM storage cells, and therefore only one generator is required for the whole set of MTJ. The writing operation requires 2 steps. In the first step the current flows in a direction that will allow writing a logical '1' on the given memory cells, and in the second step, the current will reverse its direction in order to allow writing a '0' in other memory cells.

The generator circuit (Fig. 9) is a slight variation of the circuit that was proposed in [4] and [5]. The major difference is that this implementation provides the capability to fully characterize the MTJ. For this purpose, both the current source

and the current sink have been implemented in a current mirror topology. Therefore, the intensity of the current that flows through the current source is a function of the external resistor Rbias1, while the intensity of the current that flows through the current sink is a function of the external resistor Rbias2.



Fig, 9. Bidirectional current generator

The switches S1 and S2 operate in complementary fashion. Their purpose is to turn on and off the current source. The switches S3 and S4 operate in complementary fashion and are responsible for turning off or on the current sink. This circuit works in one of 3 states:

- Current source on and current sink off - a current will flow through the write line from the MP1's VDD to the dc voltage source VDD/2.
- Current source off and current sink on - a current will flow through the write line from the dc voltage source VDD/2 to MN1's GND.
- Both current source and current sink off - no current will flow through the write line.

V. Conclusions

Thermal assisted switching provides an alternative MTJ writing mechanism in MRAM memories to both the Field Induced Magnetic Switching and the Spin Transfer Torque approaches. The TAS writing approach solves the drawbacks associated with the FIMS writing scheme. At the same time it is capable of providing write current densities at least as small as those achieved by with Spin Transfer Torque in state of the art junctions, with the advantage that the switching currents do not depend as strongly on the tunnel barrier, therefore resulting in weaker demands from the material point of view.

A scaled down prototype of a coarse grain reconfigurable array [14] that employs these TAS-MRAM elements as configuration memory was designed using a standard 0.35µ 4-Metal CMOS process technology. The reconfigurable array and each of its individual components, namely the storage cells and the current generators, were electrically simulated post-layout under an extensive set of stimuli. The results obtained give us a good degree of confidence that the new TAS-MRAM configuration memory cells can provide a very interesting technological solution for run-time reconfigurable hardware devices. The CMOS frontend design has been sent for external fabrication. The back end fabrication of the MTJ cells over the CMOS wafer, at INESC-MN, will then follow. Samples have already been received from the CMOS foundry and a PCB board is under design for further evaluation and analysis of this prototype.

Acknowledgment

This work was partially supported by the Portuguese Foundation for Science and Technology (FCT) through Project MRAM (PTDC/EEA-ELC/72933/2006).

References

[1] Third Generation Non-Volatile FPGAs Enable System on Chip Functionality. White Paper, Lattice Semiconductor Corporation, 2007.

[2] ProASIC3 Handbook, Actel Corporation, 2009.

[3] LatticeXP2 Family Handbook, Handbook, Lattice Semiconductor Corporation, 2008.

[4] Nicholas Bruchon, Lionel Torres, Gilles Sassatelli, Gaston Cambon, "Magnetic Tunneling Junction based FPGA", Proceedings of the 2006 ACM/SIGDA 14th International Symposium on Field Programmable Gate Arrays, pp. 123-130, ACM, New York, 2006.

[5] Nicholas Bruchon, Lionel Torres, Gilles Sassatelli, Gaston Cambon, "New non-volatile FPGA concept using Magnetic Tunneling Junction", Proceedings of the 2006 IEEE Computer Society Annual Symposium on Emerging VLSI Technologies and Architectures (ISVLSI'06), pp. 269-276, IEEE, 2006.

[6] Weisheng ZHAO, Eric Belhaire, Bernard Dieny, Guillaume Prenat, Claude Chappert, "TAS-MRAM based Non-volatile FPGA logic circuit", International Conference on Field-Programmable Technology (ICFPT 2007), pp. 153-160, IEEE, 2007.

[7] Yoann Guillemenet, Lionel Torres, Gilles Sassatelli, Nicholas Bruchon, Ilham Hassoune, "A Non-volatile Run-Time FPGA using Thermally Assisted Switching MRAMS", International Conference on Field-Programmable Logic and Applications (FPL 2008), pp. 421-426, IEEE, 2008.

[8] W. Zhao, E. Belhaire, Q. Mistral, E. Nicolle, T. Devolder, C. Chappert, "Integration of Spin-RAM technology in FPGA circuits", 8th International Conference on Solid-State and Integrated Circuit Technology (ICSICT '06), pp. 799-802, IEEE, 2006.

[9] J. Grollier et al., "Spin-polarized current induced switching in Co/Cu/Co pillars", Appl. Phys. Lett. 78, 3663, 2001.

[10] M. Hosomi, et al., "A Novel nonvolatile memory with Spin Torque Transfer Magnetization Switching: Spin-Ram", IEDM Technical Digest. IEEE International, pp. 459- 462, 2005.

[11] S. Cardoso, R. Ferreira, F. Silva, L. V. Melo, P. P. Freitas, R. C. Sousa, O. Redon, "Double barrier magnetic tunnel junctions with GeSbTe thermal barriers for improved thermally assisted magnetoresistive random access memory cells", J. Appl. Phys. 99, pp. 08N901, April 2006.

[12] S. Tehrani, J. M. Slaughter, M. DeHerrera, B. N. Engel, N. D. Rizzo, J. Salter, M. Durlam, R. W. Dave, J. Janesky, B. Butcher, K. Smith and G. Grynkewich, "Magnetoresistive random access memory using magnetic tunnel junctions," Proc. IEEE, vol. 91, no. 5, pp. 703-714, May 2003.

[13] Marcel J.M. Pelgrom, Aad C. J. Duinmaijer, Anton P. G. Welbers, "Matching Properties of MOS Transistors", IEEE Journal of Solid-State Circuits, vol. 24, no 5, pp. 1433-1439, October 1989.

[14] Victor Silva, Luís B. Oliveira, Jorge R. Fernandes, Mário P. Véstias and Horácio C. Neto, "Run-Time Reconfigurable Array using Magnetic RAM", IEEE - 12th Euromicro Conference On Digital System Design Architectures, Methods and Tools, pp. 74-81, August 2009.