Low-Power Open Loop Multiply-by-two Amplifier with Gain-accuracy Improved by Local-Feedback

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***Abstract*—This paper proposes the complete electrical design of a new multiply-by-two amplifier to be readily used in ultra high-speed medium resolution pipeline ADC stages. It is based in a switched-capacitor open-loop structure but with the novelty of having the gain accuracy improved by using an active amplifier with local feedback. Simulation results demonstrate that, with a very low-power dissipation and without employing any digital self-calibration or gain-control techniques, the circuit exhibits, over PVT corner and device mismatches, a dynamic performance and a gain-accuracy compatible with 6-bit level.**

***Index Terms*—ADC; multiply-by-two; low-power; time-interleaved; gain-accuracy**

I. Introduction

Wireless short range connectivity with high data rate capabilities, is and will be one of major driven technology for the consumer electronics mass market. Wireless (USB) and Ultra Wideband (UWB) Bluetooth are examples of such technologies since they start from an installed base in the billions of ports. Software radio UWB receiver implementation has numerous potential benefits ranging from low-cost and ease-of-design to flexibility. However such approach implies analogue-to-digital converters (ADCs) capable of sampling rates in order of GS/s, which constitutes a technical challenge when using a low-cost pure digital CMOS technology.

Parallel pipeline ADCs have been used to achieve medium resolutions at very high sampling rates [1, 2]. Also sharing some common blocks between two or more parallel ADCs, in a time-interleaved fashion can reduce the total power. The closed-loop multiply-by-two residue amplifiers (MBTA) usually integrated in the pipeline ADCs can be replaced by open-loop amplifiers [3, 4], reducing global size and power. However, it becomes mandatory to employ either digital gain-calibration [3] or employ replica circuits for implementing global-gain control techniques [4].

This work presents the complete design, in a 1.2 V 130 nm 1P-8M CMOS technology, of a time-interleaved MBTA building block targeting high-speed, medium/low resolution pipeline ADCs. Although open-loop residue amplification is performed, the proposed amplifier employs local-feedback in order to achieve constant closed-loop gain against Process-Supply-Temperature (PVT) variations and thus, avoiding the need of any digital self-calibration or gain-control techniques.

Simulated results demonstrate that, with a power dissipation as low as 2.0 mW, the dynamic performance of the circuit operating at 200 MS/s is compatible with more than 6 bits and very robust against PVT variations and device mismatches.

In Section II a description of the complete open-loop switched-capacitor (SC) time-interleaved MBTA circuit is presented and, in Section III, the transistor-level implementation of the closed-loop active amplifier is described in detail. Simulated results of dynamic performance of proposed MBTA circuit are provided in Section IV, and the main achieved results are finally summarized in Section V where the main conclusions are drawn.

II. Circuit Architecture

Figure 1 shows the circuit schematic of a SC open-loop MBTA. The circuit is an important building block in a time interleaved pipeline ADC. As illustrated in Figure 1 the amplifier is shared between two channels.

The circuit operates as follows. During phase Φ_1, channel 1 samples the input voltage v_{ip} into sampling capacitors C_{Si}. For a direct application in a 6-bit pipeline ADC (targeting 5.5-bit ENOB), the capacitance value of the four unit capacitors C_{Si} is set to 300 fF in order to set the thermal noise one bit below the quantization noise and also to deal with a 6 ps clock jitter (assuming that the clock is provided by a feasible PLL). In phase Φ_2, the sampled signal is amplified by a gain of 2 and the output signal is produced according to

$$v_{od} = v_{op} - v_{on} = -2 \cdot v_{id} \quad (1)$$

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where $v_{id} = v_{ip} - v_{in}$. Channel 2 operates in opposite phases. The negative reference V_{REFN} is set to 0.3 V and the common-mode voltage, V_{CM}, to 0.55 V. Switches connected to the amplifier input signals are implemented with asymmetrical transmission-gates (ATG) employing bulk-switching, switches connected to the reference voltage V_{REFN} are simply NMOS transistors and all remaining switches are implemented using symmetrical transmission gates (STG).

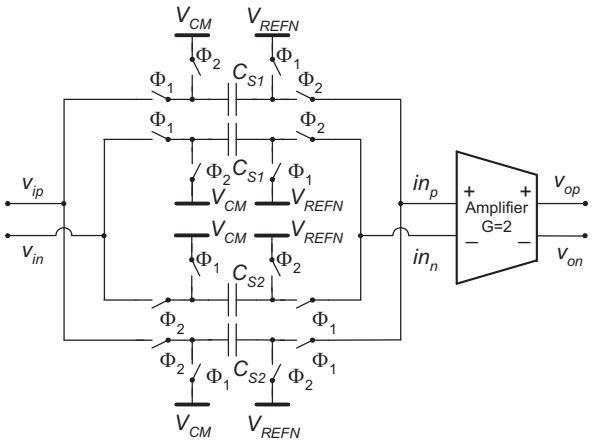

Figure 1. Schematic of the proposed open-loop time-interleaved multiply-by-two amplifier using a closed-loop active amplifier.

Note that to be readily used in pipeline ADCs, the proposed MBTA has to be slightly modified (adding 8 additional switches) into a multiplying digital-to-analogue converter (MDAC). However, this modification is relatively straightforward for implementing a 1.5-bit MDAC since the only difference is that the bottom plates of the sampling capacitors have to be connected during phase Φ_2, in the positive signal paths either to $V_{REFN}/2$, $V_{REFP}/2$ or to V_{CM} depending on the X, Y, Z digital code provided by the local 1.5-bit flash quantizer (see 0Figure 2). Likewise, the bottom plates of the sampling capacitors have to be connected during phase Φ_2, in the negative signal paths either to $V_{REFP}/2$, $V_{REFN}/2$ or to V_{CM} depending on the same X, Y, Z digital code. As a consequence of this circuit modification, at the end of phase Φ_2 the differential output signal will be given by

$$v_{od} = v_{op} - v_{on} = -2 \cdot \left(v_{id} - \frac{X \cdot V_{REFD}}{2} + \frac{Y \cdot V_{REFD}}{2} \right) \quad (2)$$

where $V_{REFD} = V_{REFP} - V_{REFN}$. For a full-scale differential signal swing of 1 Vp-p, a V_{REFP} equal to 0.8 V should be employed setting $V_{REFP}/2$ and $V_{REFN}/2$ respectively to 0.675 V and 0.425 V.

As a practical example of using an MDAC circuit, the basic block of one 1.5-bit stage of a pipelined A/D converter is shown in Figure 3. The local ADC samples the input voltage, and quantizes it in a two bit code. The MDAC reconstructs that code into a voltage, which is subtracted from the sampled input voltage. The residue obtained is then amplified and delivered to the next stage as $v_{od} = v_{op} - v_{on}$.

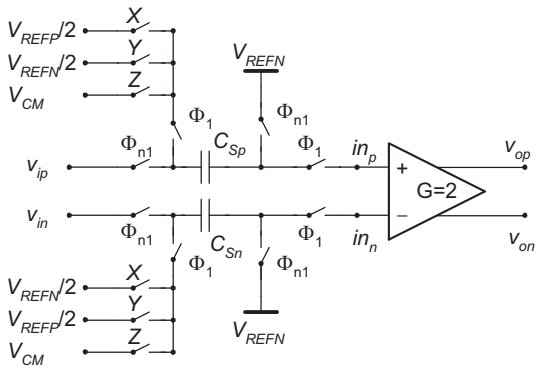

Figure 2. Modified 1.5-bit MDAC circuit.

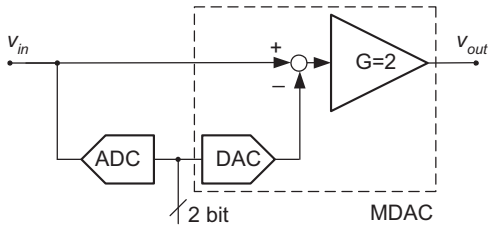

Figure 3. Generic 1.5 (or 2) bit pipelined converter stage.

Open-loop structures in pipelined A/D converters have widely been used and their main advantages are pointed out in [5]-[8]. One possible implementation when an open-loop structure is used is shown in Figure 4. Notice that, in this case, there is no feedback capacitor. Then, the amplifier gain is settled internally to 2.

The quantizer code D_i controls the reference level to be selected. Since that reference level is also amplified, the reference voltages need to be previously divided by 2. Capacitor C_S stays charged during amplification, not being the charge redistributed onto any feedback capacitor as in the closed-loop schemes, and imposes to the amplifier input an inverted signal. This is corrected inverting also the amplifier gain, to −2. During phase Φ_2, the input signal, v_{in}, is applied to the local sub ADC input, with threshold values at $+V_{REF}/4$ and $-V_{REF}/4$, and C_S is charged. During the next phase Φ_1, C_S is switched to the adequate reference voltage, according to previously stored quantizer outputs, D_i, and the amplifier processes the signal presented at its input, delivering to the next stage the produced residue.

The high gain requirement is avoided and a light and simple amplifier topology can be used, improving power efficiency, stability and allowed sampling rate. Another main advantage relies on the fact that a single sampling capacitor is required to implement both, sampling and DAC functions. As a consequence, the *kT/C* noise of this circuit is smaller when compared with the closed-loop approach.

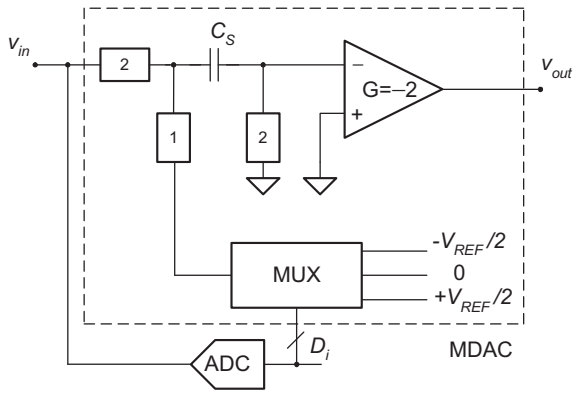

Figure 4. Open-Loop structured stage.

In other words, for the same amount of noise generated by a given stage, the capacitance value adopted can be smaller for the open-loop approach, resulting in significant power savings. However, some challenging effects are introduced in open-loop solutions. Moreover, either self-calibration or servo-loop techniques have to be used to linearize the gain.

III. Amplifier Implementation

A standard topology for a differential programmable gain or variable gain amplifier is shown in Figure 5. It is a circuit with a degenerated differential pair with a resistor as load. The differential input voltage, $v_{id} = v_{inp} - v_{inn}$, causes a current flow in the degeneration resistors, $R_{Dp} = R_{Dn}$, a function of the sum of these and of the two transistors transconductance, g_m.

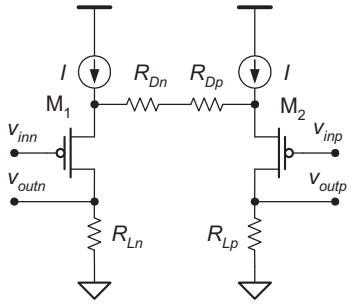

Figure 5. Degenerated differential pair amplifier (no local feedback).

The output voltage, $v_{od} = v_{outp} - v_{outn}$, is a function of the difference of the current flowing in load resistors, $R_{Lp} = R_{Ln}$, and then it can be expressed by function (3), where $R_D = R_{Dp} = R_{Dn}$ and $R_L = R_{Lp} = R_{Ln}$.

$$v_{od} = -v_{id} \frac{R_L}{R_L + 1/g_m} \tag{3}$$

The major advantage of this open-loop architecture relies on the fact that it is easy to change the overall gain, by changing the ratios of the load and degeneration resistors, making this circuit suitable for use as variable or programmable gain amplifier. Due to noise requirements, the resistance values have to be small, and to maintain the distortion levels low, the bias current needs to be large enough. An improvement [9] is the circuit shown in Figure 6 allowing a larger output swing and reduced bias current of the input transistor. The output currents are mirrored and the output currents can be higher, or the output levels easily changed.

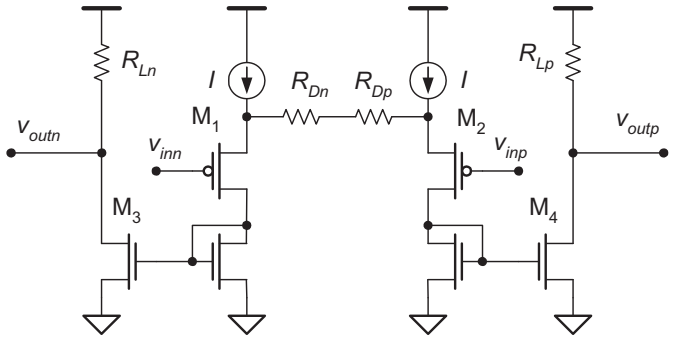

Figure 6. Amplifier with mirrored current.

The input transistors, M_1 and M_2, are still driving the current flowing in the degeneration resistors. The introduction of two current sources and two other transistors, M_5 and M_6, acting together with the input transistors, M_1 and M_2, as two super (enhanced) source followers [70][71], can be seen in Figure 7. The input transistors, M_1 and M_2, are forced to conduct a static current defined by the current sources shown hereunder. The transistors M_5 and M_6 conduct the difference of the currents defined by the upper and lower current sources. Also they take care of the current flowing through the degeneration resistors, a function of the differential input voltage. That current can be mirrored to M_3 and M_4, and to the load resistors. The performance of this amplifier circuit is suitable, for example, for multiply-by-two stages in 10-bit A/D converters [10][11].

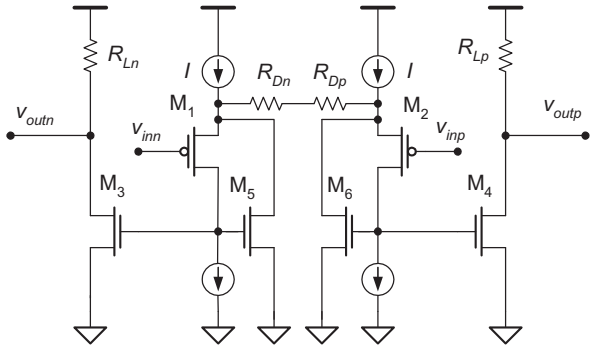

Figure 7. Amplifier with super-source followers.

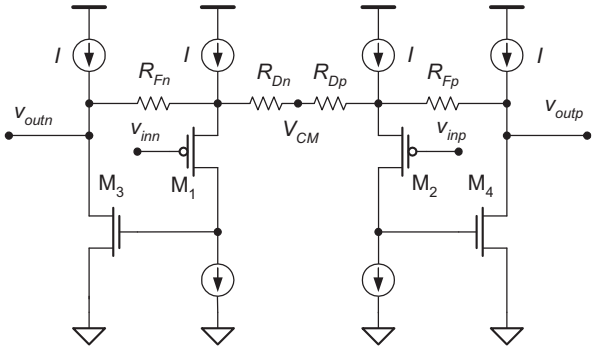

Figure 8. Amplifier with internal (local) feedback.

The circuit can be improved with the introduction of local feedback [9][10]. A closed-loop circuit, without the need of transistors M_5 and M_6, is displayed in Figure 8. The load resistor is replaced by a current source, obtaining a larger gain-bandwidth product (GBW). A negative feedback from the

output to the low impedance input transistor source is added. Input transistors, M_1 and M_2, forced to drive a fixed current, are acting as source followers, placing over degeneration resistors the differential input voltage. The subsequent degeneration resistors current is compensated by current flowing through feedback resistors, from outputs. Transistors M_3 and M_4 are acting as a class-A second stage amplifier, providing the necessary output current. Its nonlinearity is highly reduced by the first stage gain. The input transistor linearity is mandatory to achieve an appropriate overall performance. However, that requirement can be limited to small signals.

A detailed example of an amplifier with local feedback fixing the gain is displayed in Figure 9. The input transistor, M_1, is forced to drive a constant current defined by current sources, $I_1 = I_2$. It acts as a source follower, replicating at its source the input voltage swing.

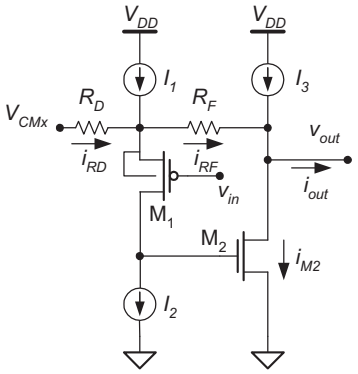

Figure 9. Amplifier with local feedback.

The level shift is the gate-to-source voltage, a function of aspect ratio and current (4).

$$V_{GS} = V_{TO} + \sqrt{\frac{2i_{DS}}{KP_pW/L}} \tag{4}$$

With the bulk connected to the source, the threshold voltage is constant, V_{TO}. The factor KP_p is technology defined. The current i_{RD} is a function of the source voltage and the V_{CMx} value. That current is summed with the current from source I_3, resulting in current i_{M2} in the M_2 transistor. The output level can be adjusted by the V_{CMx} value. The input capacitance is going to attenuate the input voltage. The gate capacitance is the gate-to-source, the low impedance node, and the less significant gate-to-drain capacitance, if no external compensation capacitor is used. The feedback corrects that attenuation, nevertheless it should be contained. The second amplifier stage delivers the output voltage to the next block.

The output voltage swing and common-mode level requirements define the drain-to-source saturation voltage of transistor M_2, V_{DSsat}, which must be guaranteed. Increasing the current and the size of M_2, transconductance will be increased. But the parasitic capacitance will increase too, and the bandwidth decreased. Being the M_1 transistor conductance moderate, the gate capacitance of M_2 is relevant. The current i_{M2} is a function of the difference between the recommended output level and the voltage at the input transistor source. The latter is shifted from the input level, which needs to be large enough to assure the operation of M_1. The current delivered by the control voltage, V_{CMx}, is going to be added to the current delivered by I_3, which can be decreased.

The gain is approximately equal to $1+R_F/R_D$, but the capacitive attenuation due to parasitic capacitor at the input (gate of M_1) reduces it. Instead of varying R_F, by linearity and stability reasons [9], the overall voltage gain can be tuned by adjusting R_D, in order to compensate for the errors, *i.e.* input parasitic capacitance, open-loop gain and output impedance. Adjusting R_D does not interfere with bias, while V_{CMx} can be also adjusted in a small range, being the offset corrected in a differential scheme. It is a non-inverting amplifier configuration, suitable to be used in 10-bit A/D converters [9] .

Figure 10 shows the final architecture of the proposed amplifier based on local feedback. It is based on a two-stage amplifier (transistors M_2 and M_5) with no inverting feedback. Transistor M_2 acts as a source follower, copying the input signal in_p to the resistor node. Transistor M_5 delivers the output voltage v_{op}, and current. The input transistor M_2 has its bulk shorted to its source to reduce the body effect. Transistors M_1, M_3 and M_4 operate as current sources. The compensation capacitor C_C is used for stability purposes and it is made equal to a unit sampling capacitance of 300 fF in order to be laid out in the same capacitor-array. The gain of the amplifier is approximately equal to $1+R_2/R_1$ but the input parasitic capacitances reduce it. The gain can be adjusted varying the value of R_1. The values of 315 Ω and 330 Ω are chosen for R_1 and R_2. The bias circuit delivers the reference voltages V_{BP} and V_{BNo}. The bias current of the input and output stages are respectively 100 μA and 500 μA.

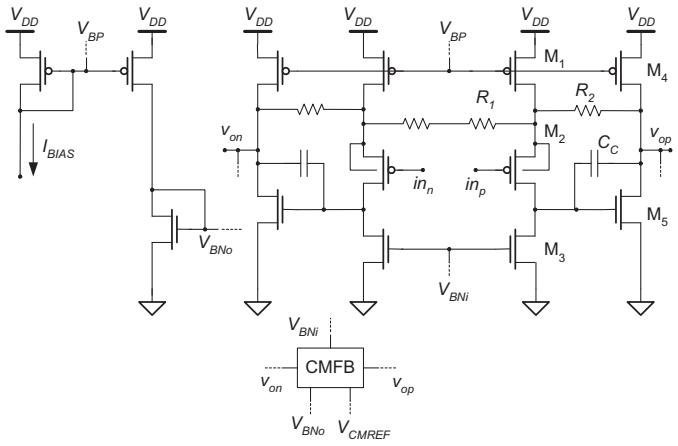

Figure 10. Fully-differential closed-loop (local feedback) active amplifier with biasing circuitry.

Figure 11 shows a traditional SC common-mode feedback circuit to be employed, in order to avoid accumulation in the common-mode errors by cascading several pipeline stages. It senses the output voltages, compares their level with a given reference level (V_{CMREF}) and adjusts the biasing voltage of the NMOS current-sources, V_{BNi}. Due to stability purposes, the values of 250 fF and 50 fF are adopted for C_{F1} and C_{F2} respectively.

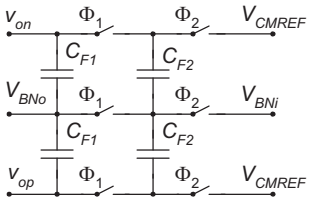

Figure 11. SC common-mode feedback circuit used in the circuit of Figure 10.

IV. Simulation Results

As stated before, the proposed open-loop MBTA circuit was designed and simulated at transistor level in a standard 130 nm CMOS technology. Figure 12 displays an input signal with differential amplitude equal to 200 mV (top graph), with a common-mode voltage of 550 mV and the output signal of the amplifier. A gain of 2 is obtained, and the output common-mode voltage is approximately adjusted to 550 mV (bottom graph).

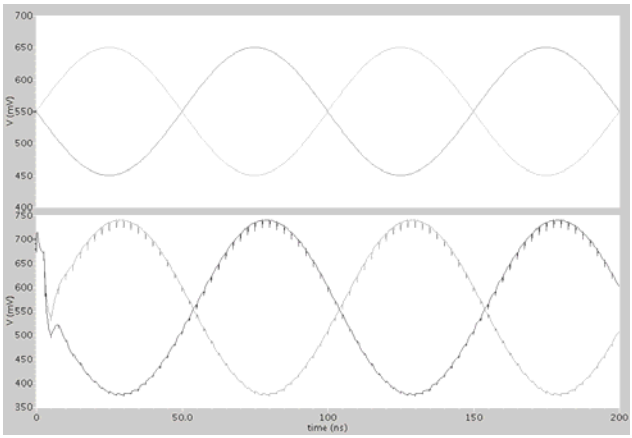

Figure 12. Input and output signals of the amplifier.

Figure 13 displays a simulated 512-bin FFT (coherent sampling) of the amplifier differential output when a sampling frequency of 200 MHz is used and an input differential signal of 200 mV and 79 MHz is applied to the amplifier (and driving a fixed 500 fF load). Simulations results exhibit a THD better than -40.4 dB mainly dominated by the third harmonic.

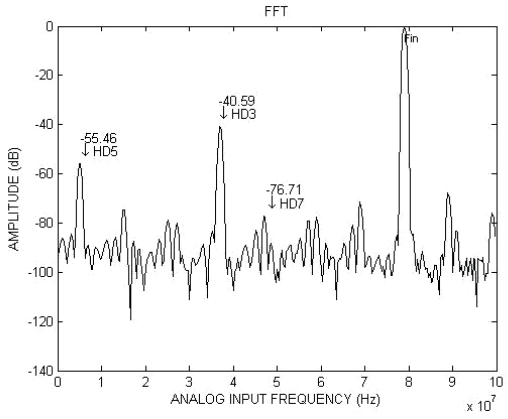

Figure 13. Simulated FFT spectrum of the output signal of the proposed MBTA circuit operating at 200 MHz when a 79 MHz input signal is applied.

In order to evaluate the gain accuracy without the need of any calibration scheme and the output common-mode errors of the amplifier, PVT corners were simulated. Table I. shows a summary of the gain and common-mode errors in the different corners considered. The circuit was simulated in fast, slow and typical parameters for the given process and for variations in the power supply of ± 5%. Temperature variations ranging from -40 ºC to 85 ºC were also considered. The amplifier has highest gain errors due to temperature effects and the worst case occurs in slow processes and 85 ºC of temperature with a gain error of -3.68 %. We should note that, for a gain accuracy compatible with the 6-bit level (when referred the output of the MBTA), a gain variation of ±3.1% is tolerable after amplification by two. The circuit exhibits low deviation from the ideal behavior due to voltage power supply variations. Maximum common-mode error is 12.06 % (~66 mV) which is acceptable since the proposed MBTA circuit has an AC-coupled sampling structure. Hence, cascading several MBTA circuit easily overcome variations up to 100 mV (the maximum input ranges are still bounded to 200 mV and 900 mV). Our main concern was to minimize the error in typical conditions and accept some degradation in worst-case corners. A second approach could be to set the boundaries of the error to ±3 % and adjust R_2 to get the required gain accuracy in all PVT corners.

TABLE I. Simulated PVT Variations.

Process	*Temp. (ºC)*	*Voltage (V)*	*Gain error (%)*	*Common-mode error (%)*
Fast	85	1.14	-1.48	-7.06
		1.2	-1.45	-7.03
		1.26	-1.45	-6.96
	25	1.14	0.20	-4.01
		1.2	0.23	-3.97
		1.26	0.33	-3.91
	-40	1.14	1.45	-0.01
		1.2	1.5	0.05
		1.26	1.6	0.07
Typical	85	1.14	-1.75	-1.90
		1.2	-1.70	-1.85
		1.26	-1.73	-1.81
	25	1.14	0.10	1.22
		1.2	0.18	1.24
		1.26	0.23	1.28
	-40	1.14	1.20	5.38
		1.2	1.28	5.41
		1.26	1.33	5.52
Slow	85	1.14	-3.68	4.72
		1.2	-3.55	4.82
		1.26	-3.50	4.85
	25	1.14	-1.33	7.86
		1.2	-1.15	7.89
		1.26	-1.05	7.94
	-40	1.14	-0.10	12.04
		1.2	0.23	12.05
		1.26	0.38	12.06

Figure 14 and Figure 15 display, respectively, in graphic mode, the simulation results of the gain error and of the output common-mode voltage.

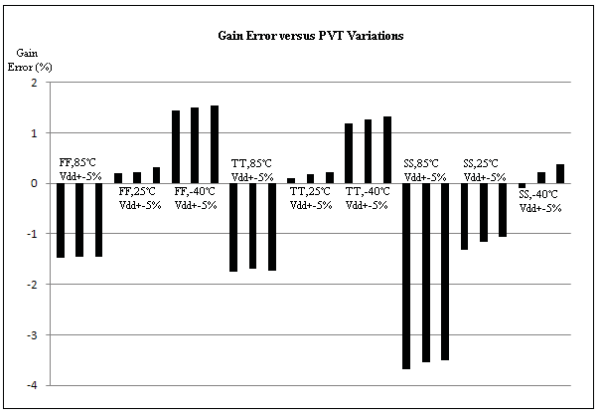

Figure 14. Gain error versus PVT variations.

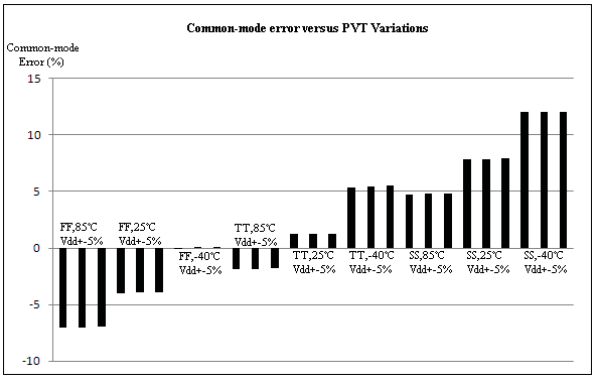

Figure 15. Output common-mode error versus PVT variations

Since the gain of the amplifier is mainly set by the resistance values (of resistors R_1 and R_2), gain and output common-mode errors due to resistor mismatch have also been considered in simulations. In these tests, the nominal supply voltage was used (1.2 V), since this parameter exhibits a small influence at the output. Results are displayed in Table II. Absolute variations of ± 15% were considered in the resistance values. Again, the temperature is the main parameter that affects the behavior of the gain error which is bounded to -4.5 %.

The complete circuit dissipates only 2.0 mW (RMS) in typical conditions which clearly demonstrates the power efficiency of the proposed MBTA block. Furthermore, the circuit does not need any digital self-calibration or gain-control techniques for achieving gain-errors compatible with 6 bits of accuracy.

V. CONCLUSIONS

The work described in this paper shown the complete electrical design of a new multiply-by-two amplifier to be readily used in high-speed medium/low resolution pipeline ADC stages. It is based in a existing switched-capacitor open-loop structure but with the novelty of having the gain accuracy improved by using an active amplifier with local feedback. Simulation results demonstrated dynamic performance and a gain-accuracy compatible with the 6-bit level.

TABLE II. MISMATCH VARIATIONS IN RESISTORS AND TRANSISTORS

Process	*Resistor mismatch (%)*	*Temp. (ºC)*	*Gain error (%)*	*Common-mode error (%)*
Fast	+15 %	85	-1.38	-7.30
		25	0.23	-4.41
		-40	1.43	-0.43
	-15 %	85	-2.13	-6.68
		25	-0.25	-3.56
		-40	1.08	0.55
Typical	+15 %	85	-1.58	-2.26
		25	0.10	0.76
		-40	1.20	4.90
	-15 %	85	-2.43	-1.46
		25	-0.43	1.68
		-40	0.85	5.91
Slow	+15 %	85	-3.25	4.38
		25	-1.05	7.42
		-40	-0.30	11.47
	-15 %	85	-4.50	5.24
		25	-0.83	8.77
		-40	-0.25	12.56

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