A CTS Pump with a Crossed-Coupled Output for Higher Conversion Efficiency

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***Abstract*—In this paper, a novel switching-capacitor DC-DC voltage converter with higher efficiency will be presented. This circuit was designed by modifying the output stage of the conventional static charge-transfer-switch (CTS) charge pump in a cross-coupled configuration. In this design, a control scheme to overcome both the reverse charge sharing and the threshold drops in the CTS pump was also employed. In this study, the capacitances for all the pumping capacitors were selected the same as 0.1 μF. With this design, our circuit can operate with a clock rate up to 1 MHz. The performance of this circuit was first evaluated by simulation by HSPICE with the 0.35-μm technology of TSMC. The results showed that this circuit can pump the low input of 1.5V nearly 5 times at the output. The conversion gain can be around 95%. The performance of the real chip manufactured by TSMC was measured and will be compared with the simulation results.**

***Index Terms*—DC-DC Converter; CTS Charge Pump; Cross-Coupled Charge Pump**

I. Introduction

The rapid advancement in fabrication technologies for complex integrated circuits over the past decade has created the trend to include all kinds of digital and analog submodules into a system chip. How to transform the low voltage of external batteries to supply various voltage levels with stable DC powers for all the on-chip modules becomes a critical challenge. There are several kinds of DC-DC converters that can be found in textbooks.[1] Among them, with the target of higher conversion efficiency, the switching type converters may be rather suitable for the design for smaller area and low power. The concept used in our design was based on the Dickson pump [2] and will be described briefly at below.

For the conventional charge-transfer-switch (CTS) pump, two problems will deteriorate the conversion efficiency. The first is the threshold drop at each stage of the switching diode. Wu and Chang proposed a static scheme to promote the conversion efficiency.[3] However, this scheme also created a problem of reverse charge sharing problem in the auxiliary pumping path. For this problem, Wu proposed a dynamic scheme to block the reverse path from sharing the charges between two neighboring stages.[3] In our previous study, we also proposed a static control scheme with a level shifter to overcome this problem.[4,5] In this study, for higher conversion efficiency, the output of this converter was modified by a cross-coupled configuration. From the simulation and measurement results, excellent performance was obtained with our circuit. The related characteristics will be demonstrated in this paper.

II. Problems of Static CTS Charge Pumps

The concept of our design was based on the Dickson charge pump. The detailed principles of operation are introduced at below.

A. Dickson Charge Pump

The Dickson charge pump is a switched-capacitor (SC) circuit that can be controlled by MOS diodes and is suitable for modern CMOS on-chip fabrication.[2] But in this design, the threshold-voltage, V_{TH}, drop in each diode would deteriorate the pumping efficiency of the promoted voltage. The resulted output voltage can be expressed as the following equation.

$$V_{out} = V_{in} + n\times(V_{\Phi H} - V_{TH}) - V_{TH} \quad (1)$$

where V_{TH} is the threshold voltage of the MOSFET, $V_{\Phi H}$ is the high-level voltage of the clocks, and n is the number of the MOS diodes in the pumping chain.

To overcome the problem of the voltage drop, the CTS pump was proposed by an additional auxiliary diode chain to control the main diodes by the higher voltage from the later stages.[3] The detailed operation is described at below.

B. Static CTS Charge Pump

The circuit of the static CTS converter is shown in Fig. 1 with a control scheme by two non-overlapped clocks, $V_{\Phi 1}$ and $V_{\Phi 2}$. The auxiliary switch chain containing M_{S1}~M_{S5} is arranged in parallel to the main switching diode chain, M_1~M_5. In this auxiliary chain, each diode is driven by the higher voltage from the next node to eliminate the voltage difference between the gate and the source electrodes which is limited by V_{TH} of the counter part in the main diode chain. With this design, the voltage drop due to V_{TH} in eq. (1) can be eliminated.

It looks like the concept of the traditional CTS for solving the V_{TH} drop works very well. However, in practical operation, this structure will fail in pumping due to the reverse charge sharing problem. This problem will be explained in the next subsection.

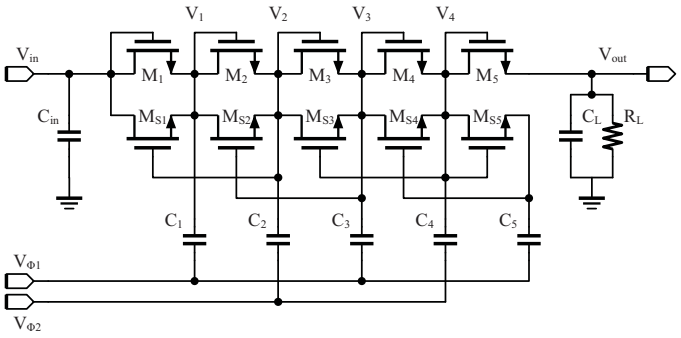

Figure 1. A four-stage static CTS charge pump. M_1~M_5 form the main diode chain from the Dickson pump to pump up the voltages from V_1 to V_4 stored in the capacitors C_1~C_4. M_{S1}~M_{S5} are the auxiliary diodes to reduce the voltage difference during the pumping at each stage in the main diode chain.

C. Reverse Charge Sharing in the Static CTS Pump

Consider the circuit shown in Fig.1. For the diodes in the stage i, the conventional CTS pump employs the higher voltage, V_{i+1}, from the node i+1, to promote the gate voltage of M_{Si}. Therefore, the voltage of the capacitor, C_i, can be pumped up without the loss by the V_{TH} in M_i. Nevertheless, M_{Si} should be off after V_i has reached its ideal value such that no shorted path exists during the pumping phase for the next stage.

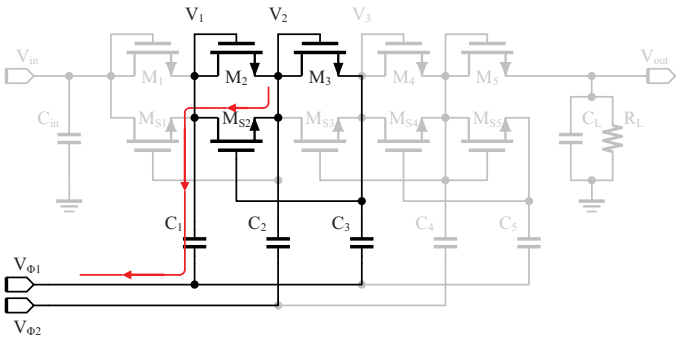

Figure 2. The reverse charge sharing path at stage 2. Diode M_{S2} is ON due to its gate voltage controlled by C_3.

Unfortunately, the gate voltage for M_{Si} would not be reduced owing to the fact that the voltage stored in C_{i+1} is kept high for pumping the next stage. As a consequence, the voltage in the pumped capacitor C_i, i.e. V_i, will be reduced due to the conduction in the reverse path through M_{Si} by sharing its charges with the lower voltage in the preceding capacitor C_{i-1}. Figure 2 illustrates the situation for stage 2 as an example. The leaking path is also indicated in this figure. Thus, the final voltage at each node would be significantly degraded.

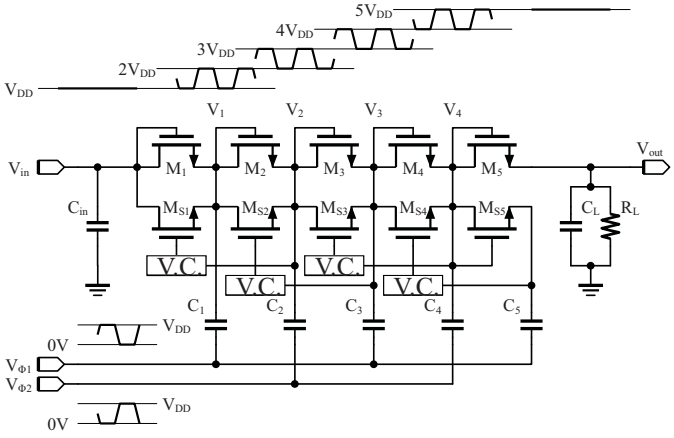

Figure 3. The CTS Pump with voltage controllers. With suitable gate control for the auxiliary diodes, M_{S1}~M_{S4}, the voltage at node i can be pumped up from iV_{DD} to $(i+1)V_{DD}$. The waveforms for the node voltages, V_1~V_4, are shown above the circuit. For example, V_1 can be pumped from V_{DD} to $2V_{DD}$ and at last V_4 can be pumped from $4V_{DD}$ to $5V_{DD}$. In this design, V_{in} was kept at V_{DD} and the high level of clocks $V_{\Phi1}$ and $V_{\Phi2}$ was also V_{DD}.

Some smart control schemes for the gate voltages of the auxiliary diodes have been proposed to block the reverse conduction paths appropriately.[3-5] In general, they can be expressed as the schematic structure shown in Fig. 3. In this figure, the voltage control (V.C.) block was designed to turn off the corresponding auxiliary diode appropriately. With this scheme, the voltage at each stage can be effectively pumped up higher than that in the previous node. For example, for the node voltage at the i-th stage, V_i is $i \times V_{DD}$ when $V_{\Phi1}$ is logic high, and V_i is $(i+1)V_{DD}$ in the next phase when $V_{\Phi2}$ is high. In Fig. 3, all the waveforms of the node voltages are shown above the circuit.

In our previous design, we proposed a static voltage shifter to control the operation of the auxiliary MOS diodes.[4,5] Since the V.C. blocks do not need to conduct large current, the layout did not consume too much area as compared to those of the pumping chain or the auxiliary chain. As a consequence, it was expected that the output voltage can be ideally pumped up with a high efficiency.

III. The CTS Pump with a Modified Output Stage

Let's consider the circuit shown in Fig. 3. The conversion efficiency may be improved by the V.C. blocks. However, the output performance may exhibit poorer regularity simply by an output diode M_5. In this design, a cross-couple structure for the output driver was employed.[6,7]

In Fig. 3, with the similarity as discussed in the conventional CTS pumps, there is also a voltage drop of V_{TH} in M_5 for providing current to the load. In addition, it can be foreseen that the performance of the load regularity would be poor due to the weak conduction by M_5. To improve this characteristic, the output was modified by the cross-coupled structure to compensate the V_{TH} drop at the load. Figure 4 illustrates the structure of cross-coupled output stage used for our DC-DC converter. In this circuit, V_{in} comes from the voltage of V_4 as in Fig. 3 with the omission of M_5. With the complementary clocks, $V_{\Phi1}$ and $V_{\Phi2}$ in Fig. 4, the load, R_L and

C_L, can be supplied with rather stable voltage and current. The detailed operation for this output stage is described at below.

In this design, two PMOS switches were used in the cross-coupled pair to isolate the output node from the internal pumping stage. Two charging phases will be controlled by the complementary clocks. Figure 5 illustrates the charging process at each phase. In this condition, $V_{in} = V_4$ and changes form 6 V to 7.5 V during the two phases of pumping. Assume $V_{\Phi H} = V_{DD} = 1.5$ V and $V_{\Phi L} = 0$ V, which are the two logic levels for the clocks.

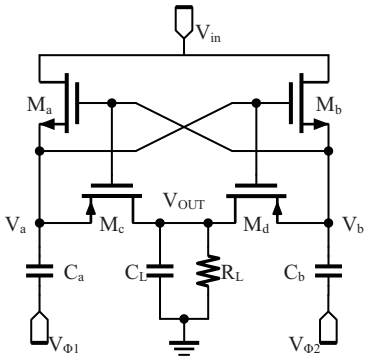

Figure 4. The cross-coupled output stage employed in our design.

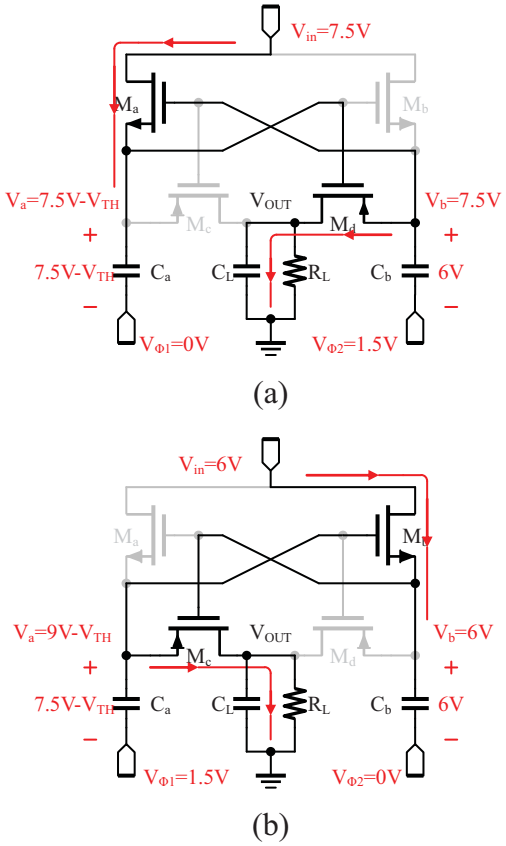

Figure 5. Operation of the cross-coupled charge pump.

Assume the voltages in C_a and C_b can follow the change of V_{in} while being pumped up by the previous stages as shown in Fig. 4. In the steady state, when $V_{\Phi 1}$ is high, C_b would be charged to V_{in}, i.e. $4V_{DD}$=6 V and C_a would be charged to $5V_{DD}$=7.5 V in the period when $V_{\Phi 2}$ is high. As seen in Fig. 5(a), i.e. in the period of $V_{\Phi 2}$=1, since V_b controls the gates of NMOS M_a and PMOS M_c, it is high enough to turn M_c off and turn M_a on at the same time. Then the load capacitor C_L can be charged by V_b through M_d. Therefore, the output voltage, V_{out}, can be charged up to $5V_{DD}$, i.e. 7.5 V.

When the clocks change to another phase, i.e. $V_{\Phi 1}$ is logic high and $V_{\Phi 2}$ is logic low as shown in Fig. 5(b), the complementary counter parts would take over the task of charging the load capacitor but with additional voltage of 1.5 V-V_{TH}. Therefore, the effective power can be supplied by C_a and C_b in this cross-coupled output. With this output configuration, the burden of the pumping stages would be reduced.

Fig. 6 shows the complete circuit of our circuit. In this design, M_5 and M_{S5} were unwanted and were replaced by the cross-coupled output pump. According to the voltage multiplication, this circuit was effective a 5-stage pump for the voltage conversion.

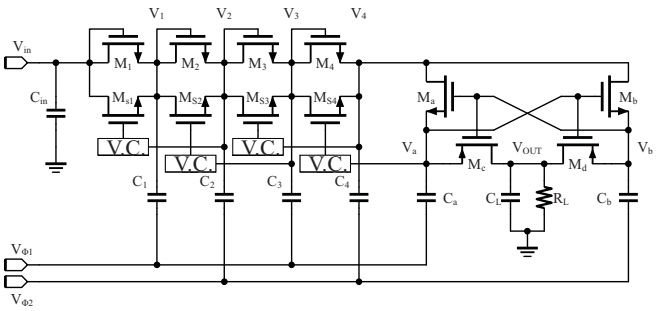

Figure 6. The whole cicuit combining the CTS and the cross-coupled charge pump.

As mentioned in the discussion for Fig. 5, the problem aroused in Fig. 6 may be the ripple at the load voltage due to the pumped voltages by the clocks. Some modification was performed on the cross-coupled module as shown in Fig. 7.

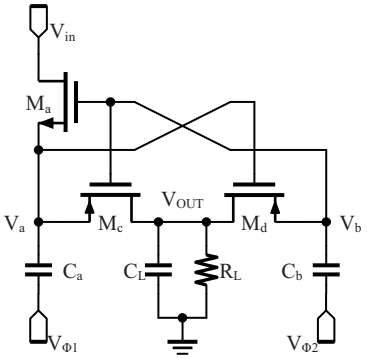

Figure 7. The modified cross-coupled charge pump.

In Fig. 7, the charging switch M_b for C_b is removed. And C_b was only taken as a buffer for the load capacitor. As discussed for Fig. 5, V_a can be pumped up to $6V_{DD}$-V_{TH} and provides charges to C_L when $V_{\Phi 1}$=1. In the next phase, C_L and C_b can share the same charge by turning M_d on by the lower V_a when $V_{\Phi 1}$=0 and $V_{\Phi 2}$=1. By this scheme, the difference between the voltages in C_a and C_b would be smaller than that

in Figs. 5 and 6 and thus the ripple in the output voltage would be reduced. Fig. 8 shows the whole circuit with the modified output pump. It was expected that this circuit would exhibit rather ideal conversion efficiency.

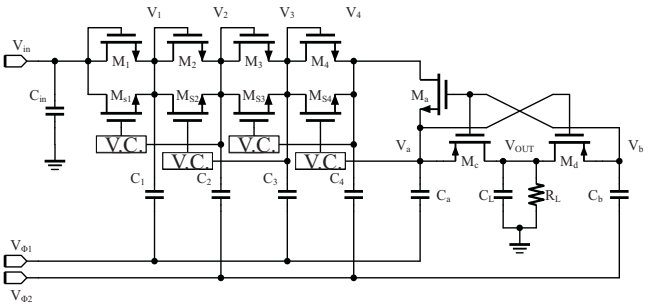

Figure 8. The charge pump with the modified cross-couple output.

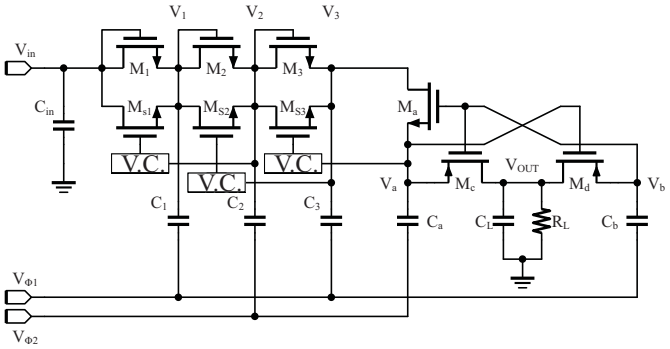

Figure 9. The 4-stage charge pump with the modified cross-coupled output.

IV. Simulation and Measurement Results

In estimating the performance of our circuit in Fig. 8, it can be seen that this is effective a 5-stage charge pump and its output would be about $6V_{DD}$. For comparison with the conventional circuit with the 4-stage pump, the circuit in Fig. 9 was used by removing one stage in the CTS pump.

In our simulation, the circuit was simulated by HSPICE with the TSMC 0.35μm technology. Fig. 10 demonstrates the voltage waveforms for the nodes of the static CTS pump in Fig. 1 and with voltage controller shown in Fig. 9. In this case, the load resistance was set as 2 kΩ. As seen in this figure, the circuits of Fig. 9 still exhibit very good waveforms. The estimated average output voltages were 6.51 V and 4.63 V for the circuits in Fig. 9 and 1, respectively. The ripples were only 7.4 mV and 5.2 mV for Fig. 9 and 1, respectively. For the case of RL= 10 kΩ, the average V_{out} was 7.20 V with a ripple of 0.7 mV for our pump in Fig. 9. With this result, it can be found that the circuit in Fig. 9 has higher conversion efficiency. Though the ripple voltage for Fig. 9 is a little higher than that for Fig. 1, the degradation is tolerable for pursuing higher efficiency.

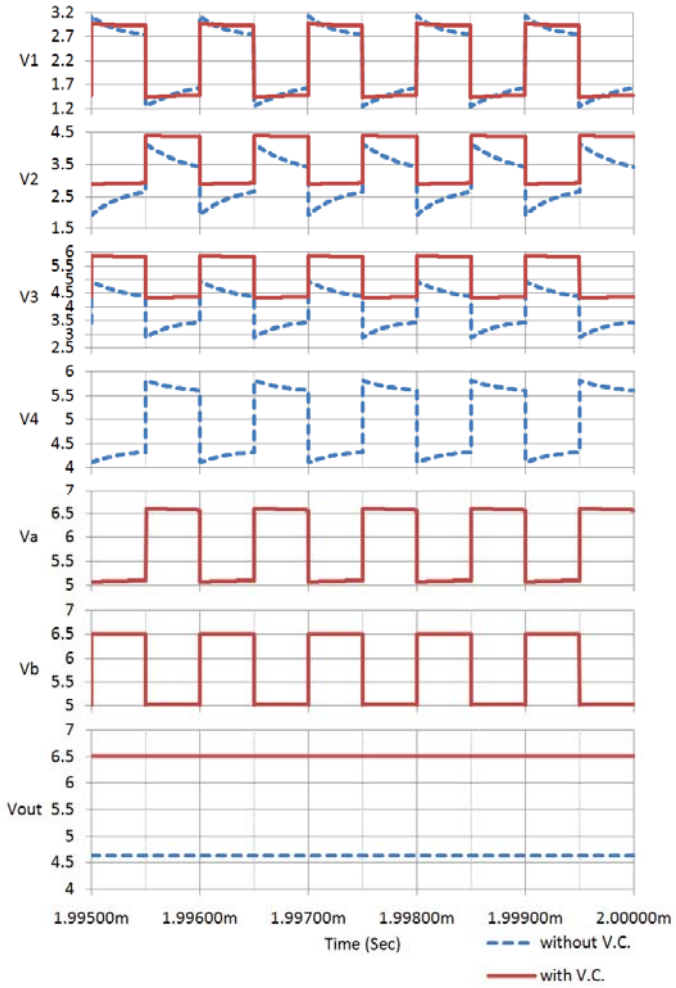

Figure 10. Simulated waveforms for the node voltages in Fig. 1 and Fig. 9 with the same load resistance that R_L=2 KΩ. The solid lines indicate the waveforms for the nodes in Fig. 9.

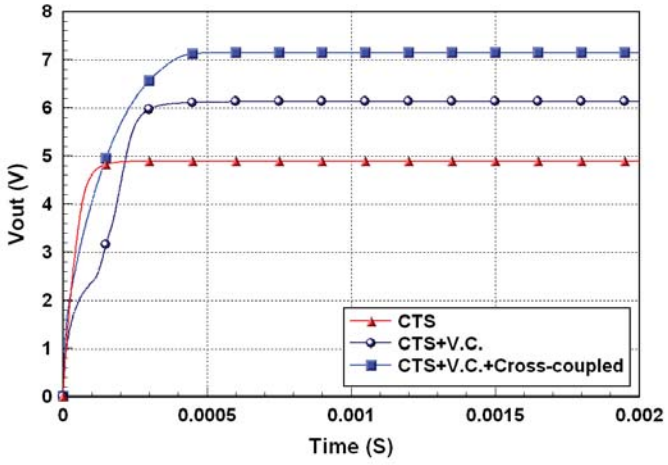

Figure 11. Simulation for different structures with the same pump stages for comparison. The curve with triangular marks is the output waveform for the circuit in Fig. 1; the curve with circle marks is for the circuit in Fig. 3; and the curve with square marks is for Fig. 9.

Figure 11 shows the simulation results of the power-up transients for the CTS pumps in Figs. 1, 3, and 9, respectively. In this case, the clock frequency was set at 1 MHz. All the pumping capacitors were 0.1μF and the load R_L was 10 KΩ. As seen in Fig. 11, it can be seen that the CTS pumps controlled by V.C. only may exhibit a slower rising curve. This delay can be eliminated when the output is replaced by the cross-couple structure.

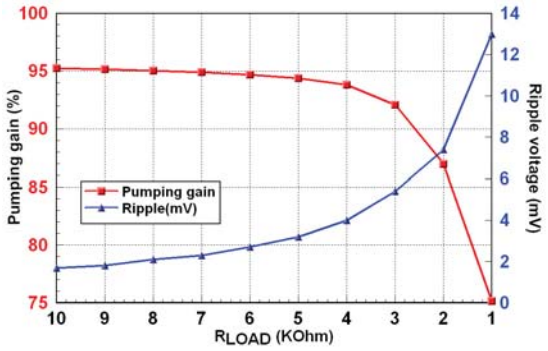

Figure 12. The conversion efficiency and the ripple voltage of the circuit in Fig. 9 with different R_L.

TABLE I. SIMULATION RESULTS FOR DIFFERENT TYPES OF CTS PUMPS.

Performance item	*Fig. 1* [3]	*Fig. 3* [4]	*Fig. 9 This work*
Input voltage	1.5 V		
Value of pumping capacitor	0.1 μF		
Clock frequency	1 MHz		
Output voltage @R_L=10 KΩ	4.89 V	6.13 V	7.17 V
Pumping gain	65.2 %	81.73 %	95.6 %
Number of Power MOS	10	10	8
Number of Pumping-Capacitor	5	5	5

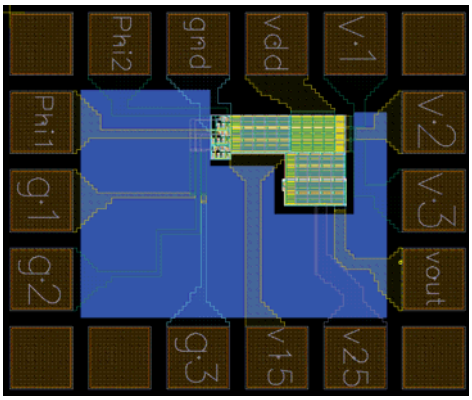

Figure 13. Physical layout of our CTS pump.

The further performance of regularity of our pump in Fig. 9 is shown in Fig. 12. From this figure, the conversion efficiency can be kept above 85 % for the load above 2 KΩ. For this case, the ripple can be controlled below 7 mV which is good enough for practical uses. Table I lists the performance parameters for comparison with other circuits. In this table, it can be seen that our circuit needs fewer power MOS devices and has a higher pumping efficiency.

In this study, our circuit was fabricated by TSMC with the 0.35-μm technology. Fig. 13 and 14 illustrate the physical layout and the micrograph of our chip. The total area of this chip was 116x172.2 μm^2. In this design, the extra area occupied by the voltage controllers was only about 26.2x57.1 μm^2, which was only about 7% of the whole chip. The additional cost of V.C. can be neglected.

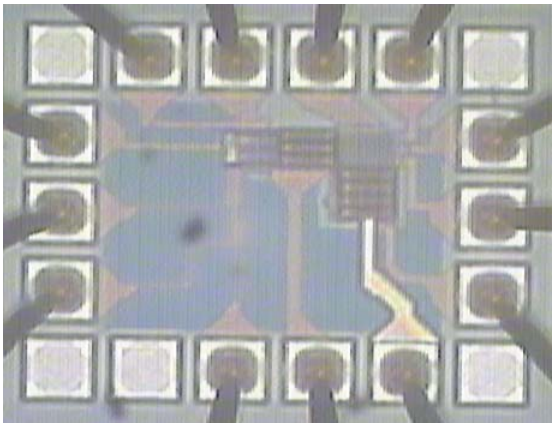

Figure 14. The die photo of the physical chip under measurement.

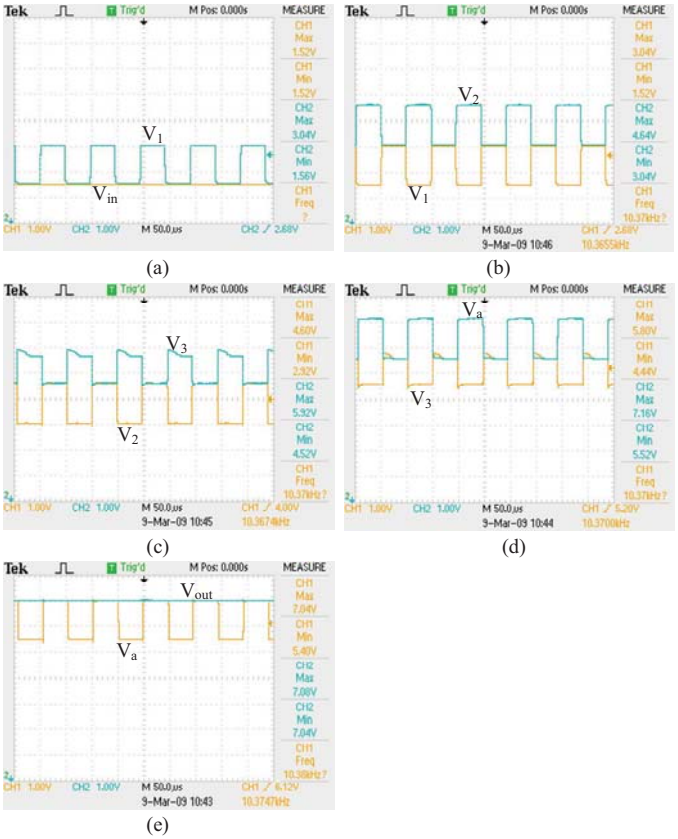

Figure 15. Measured waveforms for the nodes of the circuit in Fig. 9 with the load resistance that R_L=10KΩ.

Figure 15 is the measured waveforms of the return chip with R_L= 10 KΩ. The obtained V_{out} was 7.06 V with a ripple of 4mV which are very close to the simulation results.

V. Conclusion

A novel high-efficiency switching-capacitor DC-DC voltage converter by combining the traditional CTS pump and a cross-coupled pump has been designed and investigated. This charge pump operated at the input voltage of 1.5V with the switching frequency of 1 MHz. The output voltage can be promoted up to 7.17 V at the load of 2 kΩ. The pumping efficiency was improved to be 95.6%. This performance is suitable for on-chip voltage conversion for low power VLSI circuits. Both the simulation and measurement results confirmed us that excellent performance and efficiency can be achieved by our charge pump.

Acknowledgment

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