Analysis and Optimization of LUDMOS Transistors on a 0.18um SOI CMOS Technology

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***Abstract*—This paper is focused on the design and optimization of power LDMOS transistors (V_{BR} > 120 Volts) with the purpose of being integrated in a new generation of Smart Power technology based upon a 0.18 μm SOI-CMOS technology. The benefits of applying the shallow trench isolation (STI) concept along with the 3D RESURF concept in the LDMOS drift region is analyzed in terms of the main static (R_{on-sp}/V_{BR} trade-off) and dynamic (Miller capacitance and $Q_g \times R_{on}$ FOM) characteristics. The influence of some design parameters such as the polysilicon gate electrode length and the STI length are exhaustively analyzed.**

***Index Terms*—Power MOSFET, LDMOS, RESURF, STI, Superjunction, Silicon-On-Insulator.**

I. Introduction

Deep Sub-Micron Smart-Power Technologies are needed to enable future consumer products such as display drivers for LCD and plasma displays, power management for high efficiency power conversion and Ethernet applications. The lateral double-diffused MOS (LDMOS) transistor is the best suited power device for Smart-Power applications thanks to its ease of integration and isolation with CMOS technology [1]. The Smart-Power lithography, which is actually 0.35 μm resolution for production technologies, starts at 0.18 μm for new developments. The shrinking benefit in CMOS and BiCMOS performance circuits is difficult to be obtained in the case of power LDMOS due to its reliability dependence with the drift region length (L_{LDD}). Then the LDMOS size is mainly defined by the output stage characteristics and not by the design rules [1]. LDMOS transistors performance as switches in power ICs is basically limited by its gate charge (Q_g) and capacitance (C_g), and its specific on-state resistance (R_{on-sp}) for a given breakdown voltage (V_{BR}). Several techniques have been proposed so far to improve the R_{on-sp}/V_{BR} trade-off without leaving the gate parasitic capacitance generation aside. The superjunction (SJ) concept [2], which applies the 3D RESURF technique in the drift region (LDD), allows a further reduction of R_{on-sp} at a given V_{BR}, thus improving the R_{on-sp}/V_{BR} trade-off obtained in conventional RESURF LDMOS structures. However, this technique requires deep and narrow high doped P/N pillars, which are prone to degradation effects such as charge imbalance, P/N pillars doping inter-diffusion and current crowding at the gate/drift region [3, 4]. A second approach is placing a STI (Shallow Trench Isolation) divot in the gate/drift region of an LDMOS in order to improve the V_{BR} characteristics and to move further away the harmful electric field from the gate surface edge. The device R_{on-sp}/V_{BR} trade-off strongly depends on the dimensions, length (L_{STI}) and thickness (T_{STI}), and position of the STI block along the LDD region [5].

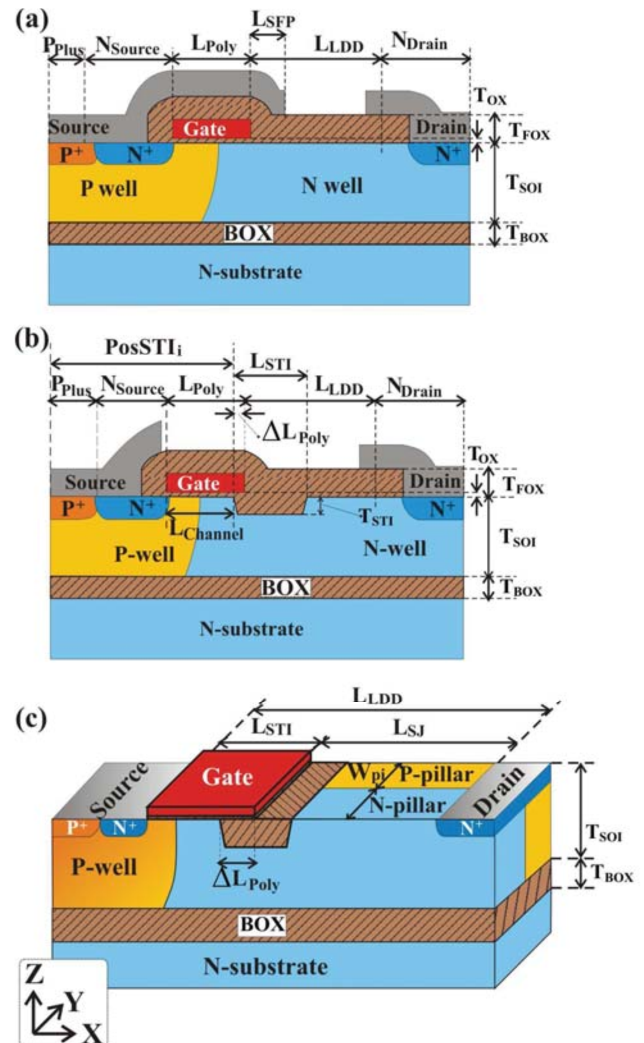

Figure 1. Schematic cross sections of the analyzed structures: (a) RESURF-LDMOS (b) RESURF-LUDMOS and (c) SJ-LUDMOS.

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In this sense, this work is addressed to analyze several LDMOS designs structures in terms of $R_{on\text{-}sp}/V_{BR}$ trade-off, $R_{on}\times Q_g$ Figure-of-Merit (FOM), and Miller charge (Q_{gd}) and capacitance (C_{gd}) by means of 2D and 3D TCAD simulations [6].

II. Structures Definition

Fig. 1 shows the schematic cross section of the LDMOS designs studied in this work: a conventional RESURF-LDMOS structure (a), a RESURF-LDMOS structure with an STI in the LDD (b) – called RESURF-LUDMOS [1] – and a 3D RESURF LDMOS structure (c), also with an STI in the LDD – called SJ-LUDMOS. A SEM image detail of a RESURF-LUDMOS transistor is shown in Fig. 2.

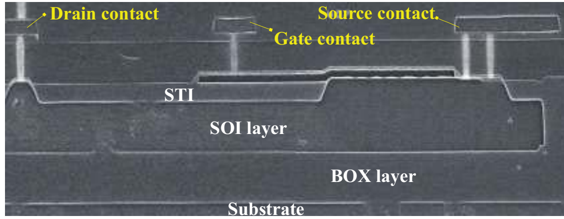


Figure 2. SEM image cross section of a fabricated RESURF-LUDMOS transistor.

All the analyzed LDMOS structures have the same Thin-SOI substrate with a SOI layer (T_{SOI}) and buried oxide (T_{BOX}) thickness of 1.6 µm and 1 µm, respectively. The same L_{LDD} of 7 µm for a total cell length (L_{cell}) of 11.5 µm is also considered. The STI depth (T_{STI}) is of 0.4µm, corresponding to the measured value on the SEM image. Boron (P-well) and Phosphorous (N-well) high-energy multiple-ion implantation sequences are needed to define an almost constant doping profile of Boron (P-well) and Phosphorous (N-well) across the SOI Silicon layer. A source field plate (SFP) is added in the RESURF-LDMOS structure (Fig. 1 (a)) to smooth the electric field peak at the Poly-gate edge. This harmful electric field can be also alleviated by means of including an STI in the LDD region. Hence, both LUDMOS structures (Fig. 1 (b) and (c)) require a previously formed STI block in the drift region before the P-well and N-well definition. On the other hand, higher P and N-type implantation doses are needed to define the optimal P and N-pillars doping concentration in SJ-LUDMOS structures (Fig. 1 (c)), which depends on the defined pillar width (W_{pi}) [2].

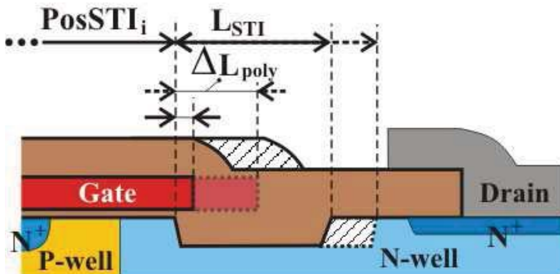


Figure 3. Schematic cross section detail of the STI length (L_{STI}) and Poly-gate/STI overlap length (ΔL_{Poly}).

Moreover, the Poly-gate length (L_{Poly}) in LUDMOS structures can be described as the addition of the Poly length ($L_{Channel}$) not-covered by the STI, or region length where the channel is defined, and the Poly length (ΔL_{Poly}) above the STI. As seen in the schematic cross section from Fig. 3, different STI lengths (L_{STI}) and ΔL_{Poly} with a fixed STI initial position ($PosSTI_i$), which leads to a constant $L_{Channel}$ of 2 µm, have been considered in these structures. Finally, all TCAD simulations throughout this work have been performed using an almost ideal constant doping profile in the drift region with a small lateral factor (LF) diffusion of 0.2, which is close to the reality.

III. LDMOS vs LUDMOS-RESURF Structures

A. Static results

Fig. 4 shows the impact of the L_{STI} and the N-well drift doping concentration value on the $R_{on\text{-}sp}/V_{BR}$ trade-off in the RESURF-LUDMOS. The RESURF-LDMOS structure with the same L_{Poly} of 2.5 µm is also included with the aim of comparing both structures.

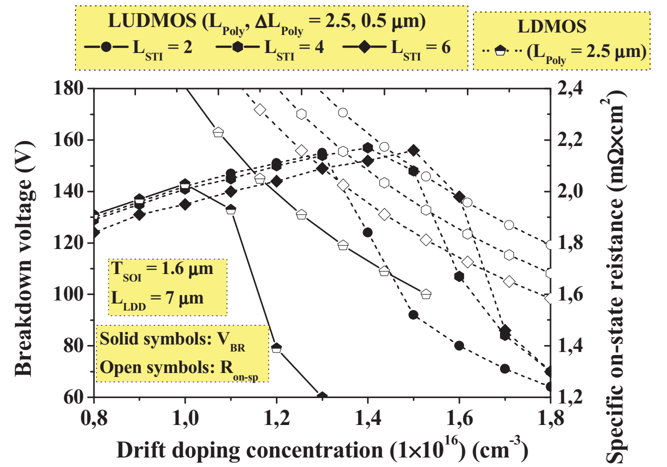


Figure 4. $R_{on\text{-}sp}/V_{BR}$ trade-off as a function of N-well doping concentration in RESURF-LDMOS and LUDMOS structures considering different L_{STI} values.

In contrast to the typical U-shaped electric field distribution in conventional LDMOS, which basically depends on the N-well and L_{LDD} values, the inclusion of the STI block leads to better electric field distribution along the LDD region at breakdown in LUDMOS structures [5]. That brings to higher V_{BR} value at higher N-well drift doping concentration, especially as L_{STI} increases. Besides, the performance of the RESURF-LUDMOS structure can be also changed by enlarging the ΔL_{Poly}, as seen in Fig. 5, where the same $R_{on\text{-}sp}/V_{BR}$ trade-offs are represented as a function of N-well doping concentration at different L_{STI} and ΔL_{Poly} values. According to the results from Fig. 5, the longer the ΔL_{Poly} the less sensitive V_{BR} value as a function of N-well doping concentration. Nevertheless, an excessive ΔL_{Poly} increment leads to lower optimal V_{BR} values since the gate moves closer to the drain, thus tightening the voltage drop between both terminals which highly stresses the structure at the Poly-gate edge region. On the other hand, the ΔL_{Poly} enlargement brings to a reduction of $R_{on\text{-}sp}$ thanks to the higher electron concentration induced by the Poly-gate at the Silicon surface.

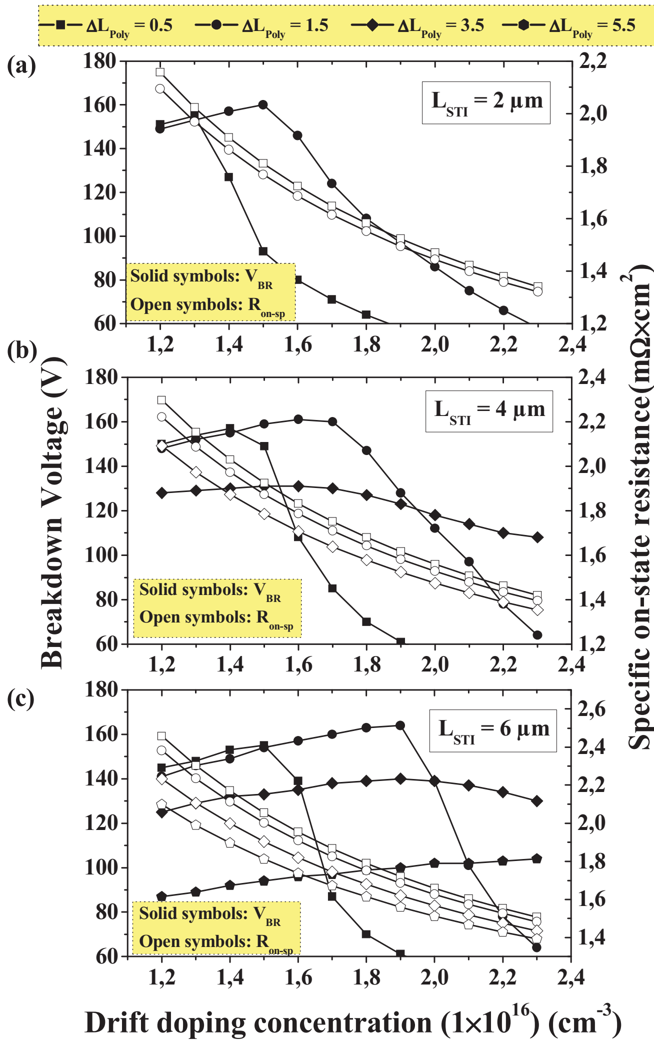


Figure 5. R_{on-sp}/V_{BR} trade-off as a function of N-well doping concentration in RESURF-LUDMOS for different ΔL_{Poly} values at L_{STI} of (a) 2 µm, (b) 4 µm and (c) 4 µm.

B. Dynamic results

The gate charge characteristics of different RESURF-LDMOS and LUDMOS structures have been simulated using the equivalent circuit from Fig. 6 where V_{dd} is fixed at 15V.

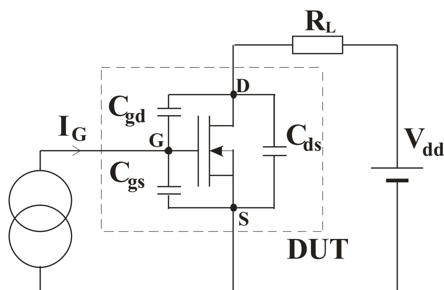


Figure 6. Equivalent circuit for gate charge characteristics simulations.

The gate charge characteristics simulation results of optimal RESURF-LDMOS and LUDMOS (with L_{STI} = 4 µm) structures in terms of R_{on-sp}/V_{BR} trade-off have been compared in Fig. 7 for different L_{Poly} values.

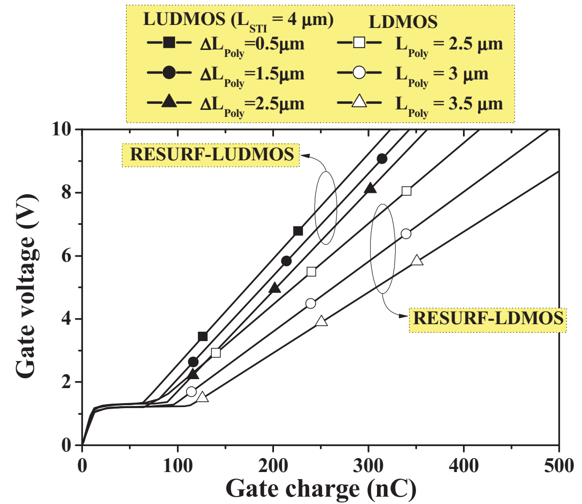


Figure 7. Gate voltage versus gate charge characteristics for RESURF-LDMOS and LUDMOS optimal structures for different L_{Poly} values.

The STI in the drift region allows to lower Poly-gate/Silicon interaction which results in a reduction of the switching losses as illustrated on Fig. 7. Moreover, L_{Poly} enlargement highly modifies the RESURF-LDMOS switching performance in contrast to LUDMOS structures. On the other hand, the Miller charge (Q_{gd}), which is approximated by the plateau region of the gate charge chart, is also highly reduced in LUDMOS structures, especially at short L_{Poly} values.

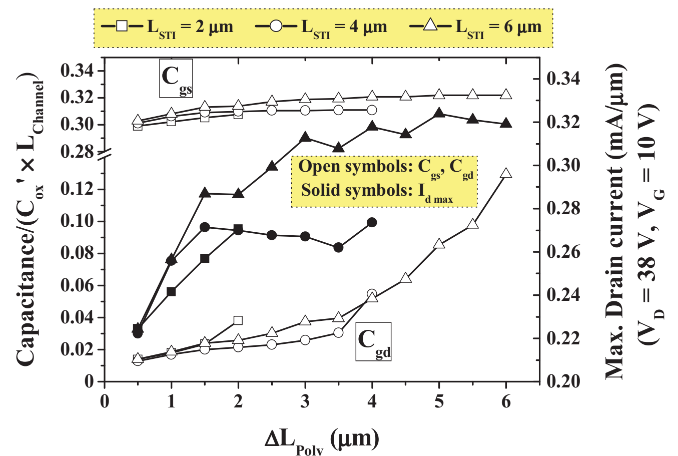


Figure 8. Capacitance and maximum drain current as a function of ΔL_{Poly}.

The gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitances as a function of ΔL_{Poly} for optimal RESURF-LUDMOS structures, in terms of R_{on-sp}/V_{BR} trade-off, are represented on Fig. 8, where the maximum current density has been simulated at an operation voltage of V_G = 10 V and V_D = 38 V. According to the small-signal simulation results from Fig. 8, the C_{gd} dramatically increases when the ΔL_{Poly} length becomes close to the L_{STI} value, that is, when the

Poly-gate block overlaps almost the whole STI region. As for C_{gs} evolution, results show almost no dependence of C_{gs} as a function of ΔL_{Poly}. On the other hand, the maximum current density increases with the L_{Poly} and L_{STI} increments due to the reduction of the R_{on-sp} as seen in previous section.

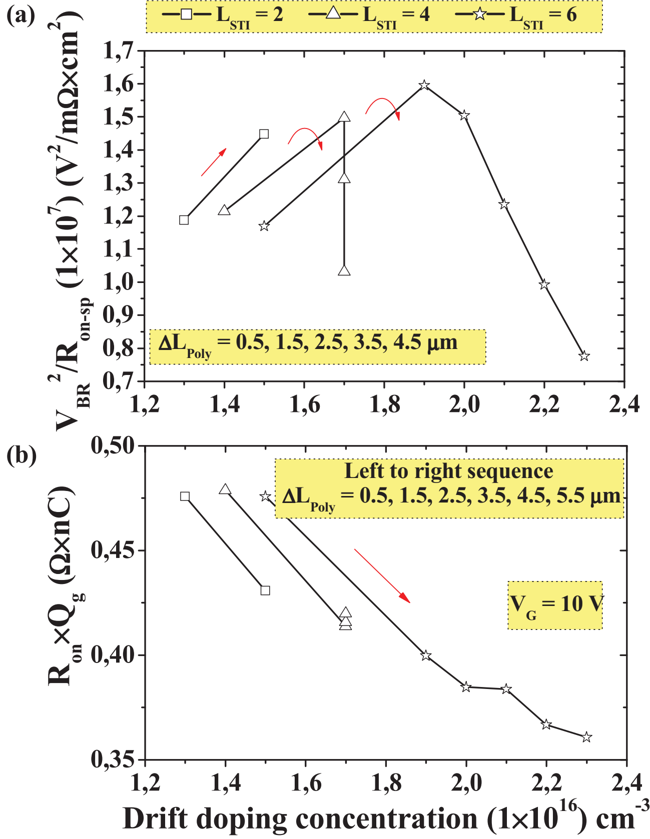


Figure 9. (a) V_{BR}^2/R_{on-sp} and (b) $R_{on}\times Q_g$ FOMs as a function of N-well drift doping concentration for different ΔL_{Poly} and L_{STI} values.

Finally, Fig. 9 shows the evolution of two different FOMs ((a) V_{BR}^2/R_{on-sp} and (b) $R_{on}\times Q_g$) vs ΔL_{Poly} and L_{STI} parameters where the optimal drift doping concentration (X axis) is considered in each case. All graph points which represent different ΔL_{Poly} values from 0.5 µm to 5.5 µm are sorted out and represented in a clock-wise sequence (Fig. 9 (a)) and from left to right sequence (Fig. 9 (b)). On the other hand, only ΔL_{Poly} values lower to L_{STI} are represented in every case. Hence, the simulation results of L_{STI} = 2 µm are sequentially represented with ΔL_{Poly} of 0.5 and 1.5 µm, and so on. Simulation results from Fig. 9 (a) clearly show maximum V_{BR}^2/R_{on-sp} factor when ΔL_{Poly} = 1.5 µm for every L_{STI} value. On the other hand, the $R_{on}\times Q_g$ factor is clearly reduced as N-well concentration increases. However, if we look at the optimal V_{BR}^2/R_{on-sp} values at ΔL_{Poly} of 1.5 µm, the $R_{on}\times Q_g$ slightly reduces as L_{STI} increases. As a conclusion from Fig. 7 to Fig. 9 an optimal RESURF-LUDMOS could be designed by using long STI blocks, almost covering the whole LDD region, and finding the appropriate ΔL_{Poly} value in terms of V_{BR}^2/R_{on-sp} FOM.

IV. Superjunction LUDMOS Optimisation

The R_{on-sp}/V_{BR} trade-off obtained in the previous RESURF-LUDMOS structure can be further improved by applying the SJ concept in the LDD region. In this section, 3D TCAD simulations are provided in the SJ-LUDMOS structure (Fig. 1(c)) in order to compare its performance with previous structures. To achieve the best R_{on-sp}/V_{BR} trade-off in SJ structures, charge balanced P and N pillars without almost P/N pillars inter-diffusion must be provided [4]. Besides, applying this technique in LDMOS structures with breakdown voltage around 150 V, that is, with a drift region length (L_{LDD}) in the range of 7 µm, pillars width (W_{pi}) of 1 µm or less are required in order to further decrease the R_{on-sp} value obtained in conventional single-RESURF LDMOS [3]. However, the narrower the pillar width, the higher the net doping reduction due to P/N pillars inter-diffusion which not allows maintaining the R_{on-sp} - V_{BR} linear relationship when the device and pillar width are scaled down [7]. If we only consider the SJ drift region, its drift resistance (R_{LDD-SJ}) theoretical values can be obtained from Eq. (1-3) in Table 1, where the W_{pi} values for each N-pillar (N_{pi}) doping concentration are obtained through Eq. (1) considering $N_{pi} = P_{pi}$ in order to accomplish optimal V_{BR} or charge balance conditions [2]. The depletion width between P/N pillars is represented by W_{dep} in Eq. (3).

TABLE I. SJ structure analytical equations

$$W_{pi}\cdot N_{pi} = \frac{2\cdot\varepsilon_{si}\cdot\alpha\cdot E_{cr}}{q} \approx 4\cdot 10^{12}\ \text{cm}^{-2} \quad (1)$$

$$R_{LDD\text{-}SJ} = \frac{1}{q\cdot N_{pi}\cdot\mu_{nd}}\cdot\left(\overbrace{\frac{L_{STI}}{(h_{pi}-T_{STI})\cdot(W_{pi}-W_{dep})}}^{R_{STI}} + \overbrace{\frac{L_{SJ}}{h_{pi}\cdot(W_{pi}-W_{dep})}}^{R_{SJ}}\right)\cdot\frac{2\cdot W_{pi}}{W} \quad (2)$$

$$W_{dep} = 2\cdot\sqrt{\frac{\varepsilon_{si}\cdot V_{bi}}{q\cdot N_{pi}}} \quad (3)$$

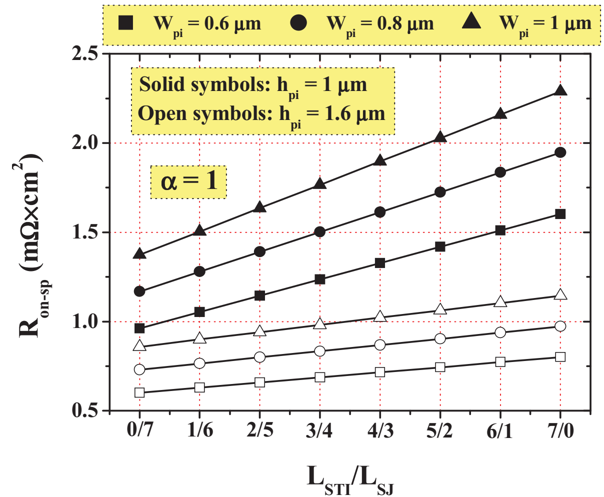
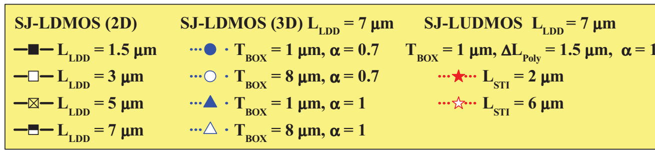


Figure 10. Theoretical R_{LDD-SJ} as a function of L_{STI}/L_{SJ} in a SJ-LUDMOS structure of L_{LDD} of 7 µm for different pillar width (W_{pi}) and heights (h_{pi}).

The resulting R_{LDD-SJ} theoretical dependence with some important parameters such as the pillar width (W_{pi}) and height (h_{pi}) and the ratio between L_{STI} and L_{SJ} in a SJ-LUDMOS structure is shown in Fig. 10. Reduction of R_{LDD-SJ} values could

be theoretically accomplished by using the deepest and narrowest possible pillars, and also by using a small L_{STI} in comparison with L_{SJ} (see Fig. 1 (c)). As seen in Eq. (1) the N_{pi} value depends on the α parameter, which is considered equal to 1. This parameter value, which can be delimited between 0 and 1 [1] should be carefully chosen as a function of the device application. That is, in applications where R_{on} drives the device optimization, high α=1 can be considered. On the contrary, V_{BR} can be favored in detriment of R_{on} by reducing α value.

Different superjunction 2D and 3D LDMOS with and without STI are compared in terms of $R_{on\text{-}sp}/V_{BR}$ trade-off taking into account W_{pi} of 1 μm in all cases. The trade-off results, illustrated in Fig. 11, are represented as a function of the percentage increment of N-pillar doping concentration with respect to P-pillar. On the other hand, 2D and 3D simulations have been done with LF of 0 and 0.2, respectively. Results from Fig.11 (a) shows the most important degradation effect in SJ lateral structures: the substrate assisted depletion. To totally eliminate this degradation effect, Silicon-on-Sapphire substrates [9] must be used. Otherwise, other alternative designs are N-type surface implantation steps [10], and the inclusion of an N-type buffer layer [11], this case is only for Bulk technology. All cases suppose high additional expenses.



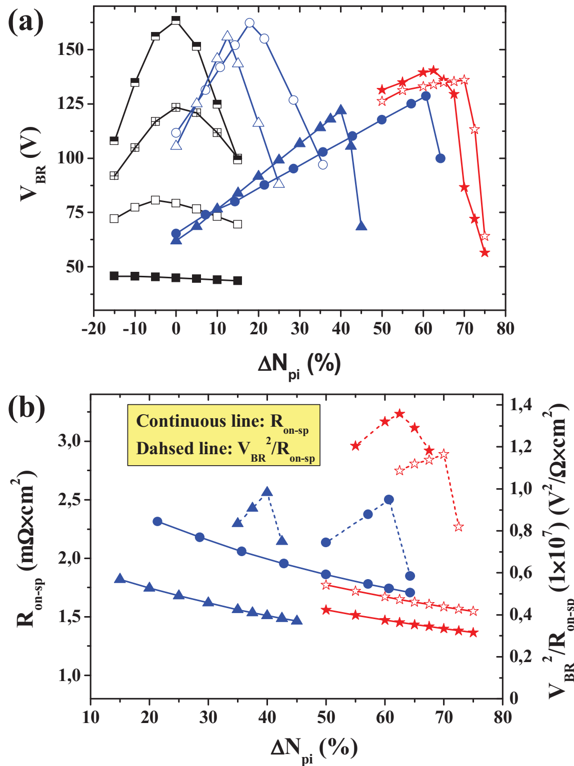


Figure 11. $R_{on\text{-}sp}/V_{BR}$ trade-off as a function of N-pillar concentration percentage variation with respect to P-pillar concentration in SJ-LUDMOS structures with W_{pi} of 1 μm.

In SJ-LDMOS (2D) simulations, where no substrate action is generated, the balanced charge conditions is assured when $N_{pi} = P_{pi}$, although a slight negative ΔN_{pi} is required, especially in small L_{LDD} values, since the N-type charge contribution coming from the N^+ drain is higher than the P-type charge from the P-well. Optimal V_{BR} are shifted to positive ΔN_{pi} values in SJ-LDMOS (3D) since the substrate effect is taken into account. These structures are simulated with different α (0.7 and 1) and T_{BOX} (1 and 8 μm) values. Although high T_{BOX} of 8 μm should almost completely attenuate the field effect action, as it happens with SOS substrates, the simulation results shows a positive ΔN_{pi} in the range of 10-20 %. However, almost no degradation of V_{BR} is observed when comparing with (2D) results with the same L_{LDD}, especially in the case of α = 0.7. Much higher positive N-type doping must be added to N-pillars when T_{BOX} is 1 μm as clearly seen in Fig. 11(a), in particular at low α = 0.7 since the higher net-doping inter-diffusion between P/N pillars [5] demands higher ΔN_{pi} variation. Besides, lower α values yields to lower N_{pi} and P_{pi} concentration, thus reducing the sensitivity to charge imbalance, as seen in SJ-LDMOS results with α of 0.7 and 1. As for SJ-LUDMOS structures, simulations are made with TBOX of 1 μm, ΔL_{Poly} of 1.5 μm and α = 1 for different L_{STI} of 2 and 6 μm. The inclusion of the STI introduces an additional field-effect action coming from the Poly-gate extension over the STI and changes the electric field distribution at the SOI layer surface, in the same way as seen before with RESURF structures. Hence, a positive shift to higher ΔN_{pi} percentage values is required, leading to lower $R_{on\text{-}sp}$ as compared with SJ-LDMOS counterpart in Fig. 11(b). The sum of the commented $R_{on\text{-}sp}$ with the slightly better V_{BR} results brings to much higher $V_{BR}^2/R_{on\text{-}sp}$ values in SJ-LUDMOS.

Table II compares the main simulation results from the most optimal LDMOS structures analyzed in this work. SJ-LUDMOS structures could improve the switching performance of RESURF-LUDMOS although some additional work has to be done in terms of reliability.

TABLE II. OPTIMAL LDMOS STRUCTURES COMPARISON

	$R_{on\text{-}sp}$ (mΩ×cm²)	$V_{BR}^2/R_{on\text{-}sp}$ (V²/Ω×cm²)	R_{on}×Q_g (Ω×nC)
RESURF-LDMOS (L_{Poly} = 2.5 μm)	2.23	9.17×10⁶	0.69
RESURF-LUDMOS (L_{STI}, ΔL_{Poly} = 6, 1.5 μm)	1.65	1.6×10⁷	0.4
SJ-LUDMOS (L_{STI}, ΔL_{Poly} = 2, 1.5 μm)	1.45	1.37×10⁷	0.31

Finally, the LDMOS structures results from Table II are compared in Fig. 12 with experimental and simulated power LDMOS devices extracted from the literature. As seen from this chart, results below theoretical VDMOS Silicon limit are reached with optimized RESURF-LUDMOS structures, which could be an excellent alternative to classical power RESURF-LDMOS transistors.

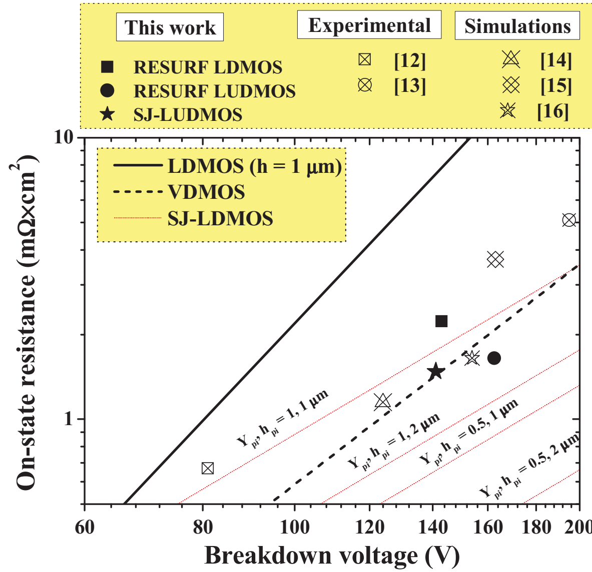


Figure 12. Comparison between the theoretical SJ and Silicon limits with the $R_{on\text{-}sp}/V_{BR}$ trade-off results obtained in this work. State-of-the-art experimental and simulated results are also added in this plot. (h is the height of the LDMOS Silicon active area).

V. Conclusions

Optimization and comparison of different power LDMOS structures on Thin-SOI substrates for Smart Power applications are presented in this work by means of TCAD numerical simulations. Appropriate STI and Poly-gate configuration design leads to excellent $R_{on\text{-}sp}/V_{BR}$ trade-off and $R_{on}\times Q_g$ FOM in RESURF-LUDMOS structures. Switching performance can be further improved in the case of SJ-LUDMOS structures. However, the inclusion of the STI block and the Poly-gate field plate in the LDD region slightly reduces the 3D RESURF effectiveness, which deteriorates the SJ-LUDMOS reliability in comparison with RESURF-LUDMOS structure.

Acknowledgment

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References

[1] M. Zitouni et al. “A new lateral power MOSFET for smart power ICs: the LUDMOS concept” Microelect Journal. 1998;30(6): 551 – 61.

[2] T. Fujuhira. “Theory of semiconductor superjunction devices” Jpn. J. Appl. Phys. 1997;36(10):6254 – 62.

[3] H. Zhong et al. “Practical superjunction MOSFET device performance under given process thermal cycles. Semicond. Sci. Technol. 2004;19(8):897 – 96.

[4] I. Cortés et al. “Analysis of low voltage super-junction LDMOS structures on Thin-SOI substrates” Semicond. Sci Technol. 2007;23(1):1 – 8.

[5] I. Cortés et al. “Static and dynamic electrical performances of STI thin-SOI power LDMOS transistors” Semicond. Sci. Technol, 2008;23(9):1 - 7.

[6] Sentaurus TCAD Tools Suite. Synopsys 2007.

[7] DN. Pattanayak et al. “Low Voltage Super Junction Technology” IET Circuit Device Syst. 2007;1(5):347 – 56.

[8] W. Chen et al. “Optimization of super-junction SOI-LDMOS with a step doping surface-implanted layer” Semicond. Sci. Technol. 2007;22:464 - 70.

[9] Nassif-Khalil S.G.: Super-junction LDMOST on Silicon-on-Saphire substrate, IEEE Trans. Electron Dev. 2003;50(5):1385 – 91.

[10] Chen W.: Optimization of super-junction SOI-LDMOS with step doping surface-implanted layer, Semicond. Sci. Technol, 2007;22(5):464 – 70.

[11] Park Il-Y.: New superjunction LDMOST with N-buffer layer, IEEE Trans. Electron Dev. 2006;53(8):1909 – 13.

[12] M. Kanechika et al. “A concept of SOI RESURF lateral devices with striped trench electrodes”. IEEE Trans. Electron Dev. 2005; 52(26): 1205 – 20.

[13] AW. Ludikhuize et al. “Extended (180V) voltage in 0.6 um thin-layer-SOI A-BCD3 technology on 1 mm BOX for display automotive and consumer applications”. In Proc. ISPSD 2002, pp. 77 – 80.

[14] S. Xu et al. “120 V interdigitated – drain LDMOS on SOI substrate breaking power LDMOS limit”. IEEE Trans. Electron Dev. 2000; 47(10): 1980 – 85.

[15] HP. Xu et al. “Superjunction LDMOS with drift region charge – balanced by distributed hexagon P – islands”. In Proc. IEEE Conference on Electron Devices and Solid–State Circuits 2003, pp. 313 – 16.

[16] MA. Amberetu et al. 150-V Class Superjunction Power LDMOS Transistor Switch on SOI. In Proc. Power Semicond. Dev. and ICs 2002, pp. 101 – 04.