HARDWARE IMPLEMENTATION OF PARAMETRIC ALGORITHM FOR ASYNCHRONOUSLY GATHERED MEASUREMENT DATA BASED ON THE FPGA TECHNOLOGY

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The hydroacoustic system based on DOA estimation utilizes passive antenna composed of many hydrophones. The samples of the arriving acoustic signal must be gathered synchronously from each hydrophone. This enables to take advantage of parametric processing signals methods. These methods make possible determination of the amplitude and the phase relationship among particular hydrophones. The newest complex systems made up of many sub modules uses network solutions. In the case of Ethernet network some standards (e.g. Precision Time Protocol) are defined to enable synchronization of the data (samples) gathered from many hydrophones by the clock synchronization. When the antenna consists of few hydrophones then the special concentrator connected point-to-point to hydrophones can be utilized. This article discusses the issue related to PTP as well as concentrator based on FPGA technology, which uses simple UDP protocol. In the case of concentrator the synchronous method of the I/Q detection which not requires synchronous samples acquisition is also presented.

INTRODUCTION

The OBR CTM S.A. develops sonar systems based on cylindrical array of hydrophones. These systems utilize DOA estimation to detect targets (threats) in protected sea area. The basic algorithm, relates to direction estimation, enables to determine statistics of time shifts among the signals generated by particular hydrophones. The parametric methods (e.g. Multisource Signal Classification) make possible to simplify this extraction to statistic methods based on the complex vectors within the selected sound band. The DOA estimation theory does not concern with the method which transforms the received signal into complex vectors, but other technical solutions perform it.

The Nyquist's theorem defines the minimum sampling frequency to correctly interpolate continuous time signal into digital samples. The available hydrophones generate analog or

digital output signal. The analog signal is not resistant to interferences. Furthermore the multi-channel ADC (Analog-to-Digital Converter) device with common timing must be utilized. The digital signal is robust to interferences. But the digital samples from hydrophones are not gathered synchronously. In this case the special method must be used to synchronize samples generated by each hydrophone.

1. THE PARAMETRIC METHODS OF THE SIGNAL PROCESSING.

The parametric methods of the signals processing deal with band signals. The methods like Discrete Fourier Transform or I/Q detection transforms series of time samples gathered from many hydrophones into complex vector. In the case of passive antenna the series of complex vectors are converted into covariance matrix. The linear algebra methods transform this matrix into DOA estimation.

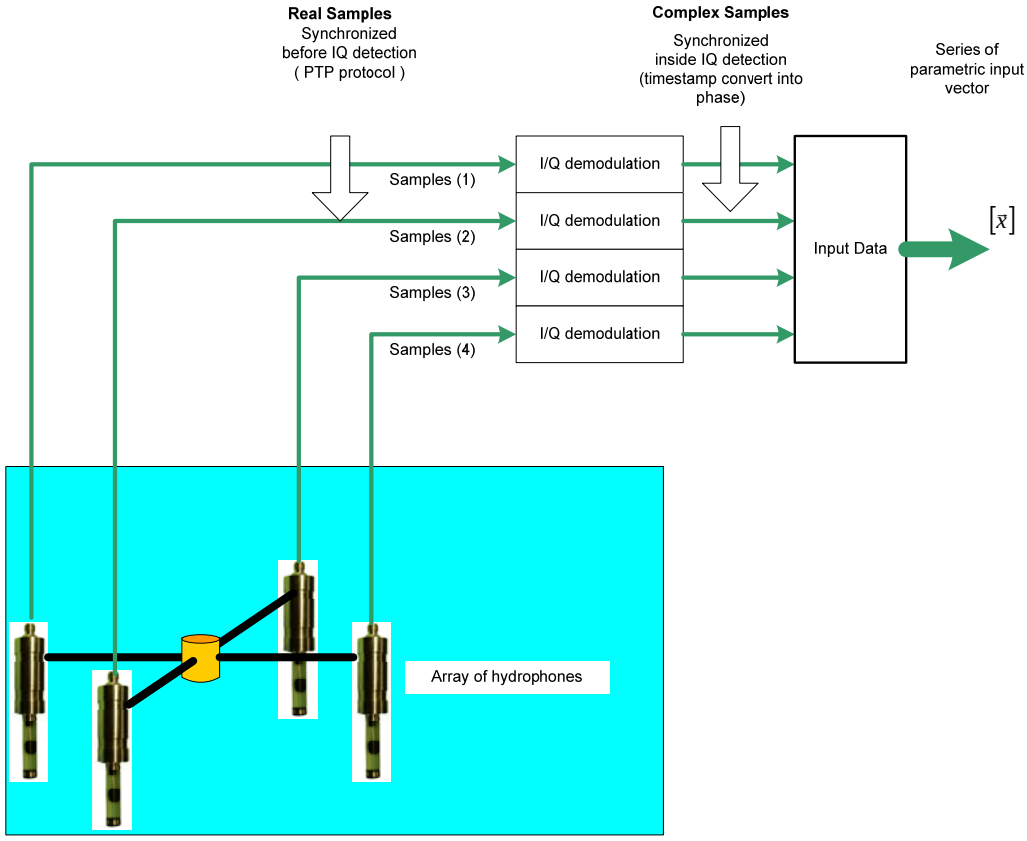

Fig.1. Transformation scheme real samples into complex vector

The equation 1 describes the sampling time for each hydrophone, when the timing is not common.

$$t_s = \frac{n_k}{fs_k} + t0_k \qquad (1)$$

In this equation k means hydrophone number, n_k is the number of time sample, fs_k is the sampling frequency and $t0_k$ means the start time of samples gathering. When hydrophone generate analog signal, then the host system utilize the analog to digital converter based on sample & hold method. In this case the sampling time does not depend on hydrophone

number. So the gathered samples are synchronized. When the hydrophone generates digital signals two methods can be used to synchronize samples:

- time base synchronization of hydrophones array based on the IEEE-1588 standard,
- measurement of sampling time based on analyzing the time-stamps.

The first standard offers the sub-microsecond synchronization of real time clocks in components of a networked distributed measurement and control system. This method requires implementation of the IEEE-1588 standard in each hydrophone (CPU). The second method can be utilized, when the hydrophone generates UDP frames. The host system must synchronize each sample via time-stamp according to common timing. This is possible on condition that the delay between processes of samples gathering and sending of Ethernet frames is strictly fixed.

2. THE TIME BASE SYNCHRONIZATION OF HYDROPHONES ARRAY BASED ON IEEE-1588 STANDARD.

The IEEE-1588 standard provides sub-microsecond synchronization over long distances with standard cabling by synchronizing multiple clocks over networks such as Ethernet. There are two steps for synchronizing devices using IEEE 1588: The first one determines which device serves as the master clock. Whereas, the second one measures and corrects the time skew caused by clock offset and network. The time difference between master clock and slave clock is a combination of the clock offset and message transmission delay. Correcting the clock skew is done in two phases: offset correction and delay correction. Because the master and slave clocks drift independently, periodically repeating offset correction and delay correction keeps the clocks synchronized. At the beginning of synchronization process master sends so called Sync-Message, with its current time to the slave where a time-stamp is generated exactly when the message is received. Then the master sends a follow-up message to the slave with the exact time when the original sync-message had been sent. Next the slave corrects its local real-time clock to the clock of the master. In order to eliminate the real-time clock delay of the slave due to travel time of packet over the network, the slave sends a so called Delay-request message to the master and notes the exact sending time. The master then replies with the time-stamp when the Delay-request message was received. The slave can then compute the exact time of the master clock and finalize the synchronization. Further statistical methods are used to constantly adjust the real-time clock to correct for any residual fluctuations from the physical layer, network, repeaters and switches.

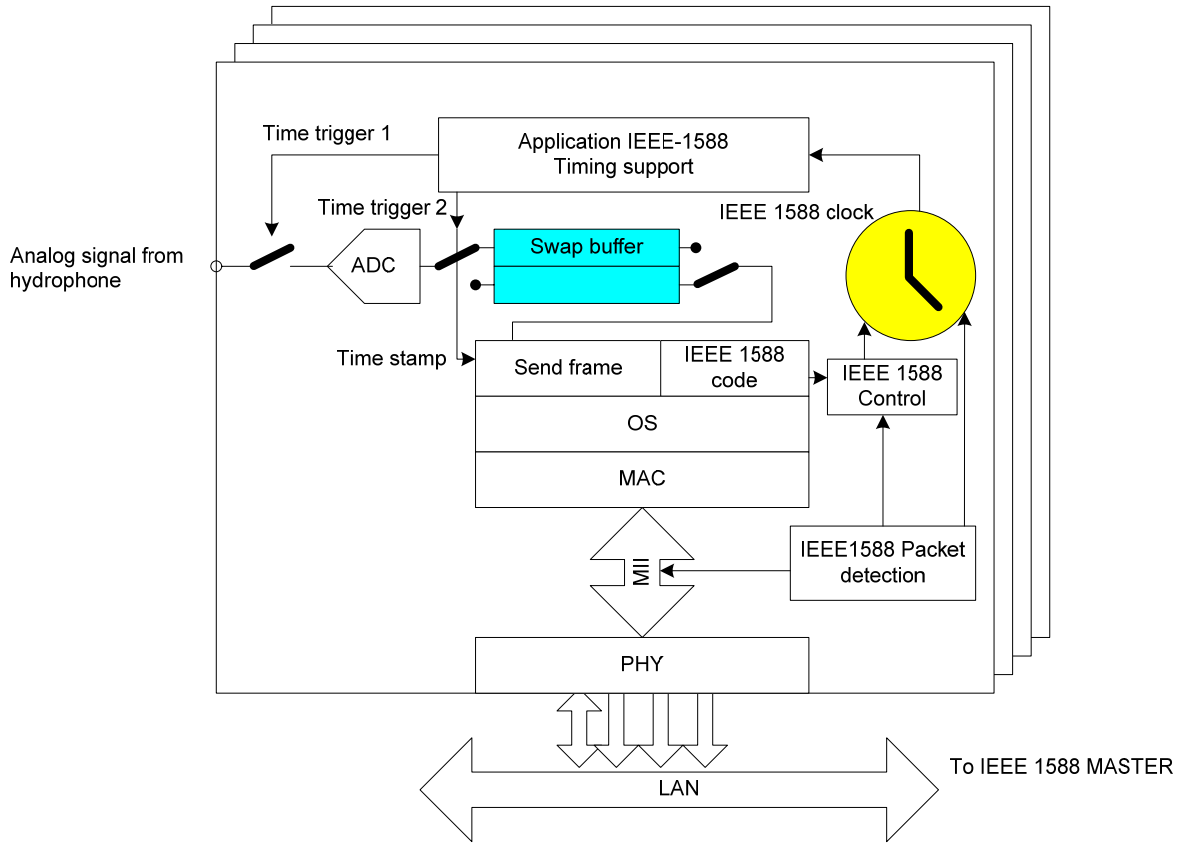

Fig.2. Application scheme, which utilizes the IEEE-1588 standard

The figure 2 presents the application, which utilizes the IEEE-1588 standard. It makes possible to synchronously capture data by many distributed devices. The common timing enables synchronous gathering of the samples. The analog signals, from each hydrophone, are sampled at the same time (Time trigger 1). The data are gathered into swap buffers. The time base is divided into two identical phases (Time trigger 2):

- during the even phase the current samples are gathered into buffer no. 1, while the data from buffer no. 2, captured in previous phase, are sent via LAN.
- during the odd phase the samples are gathered into buffer no. 2, while the data from buffer no. 1 are sent via LAN.

The synchronization process based on the IEEE-1588 standard enables Master to determine sampling time:

$$t_s = \frac{n}{fs_k} + t0 + (\mu\sec ond\_delay)_k \qquad (2)$$

where:

k means the hydrophone number;
n is the sample number in UDP frame, not depended upon hydrophone number;
$t0_k$ means the start time of data gathering.
fs_k represents instability of local oscillator.

Further calculation of signal processing algorithms (I/Q demodulation, estimation of covariance matrix, Multisource Signal Classification) is implemented in the software application.

3. THE TIME-STAMP FOR INDEPENDENT SERIES OF TIME SAMPLES.

The system composed of few independent hydrophones asynchronously gathers the samples. The capture time of each series must be reconstructed according to the host time base as presented on the picture beneath.

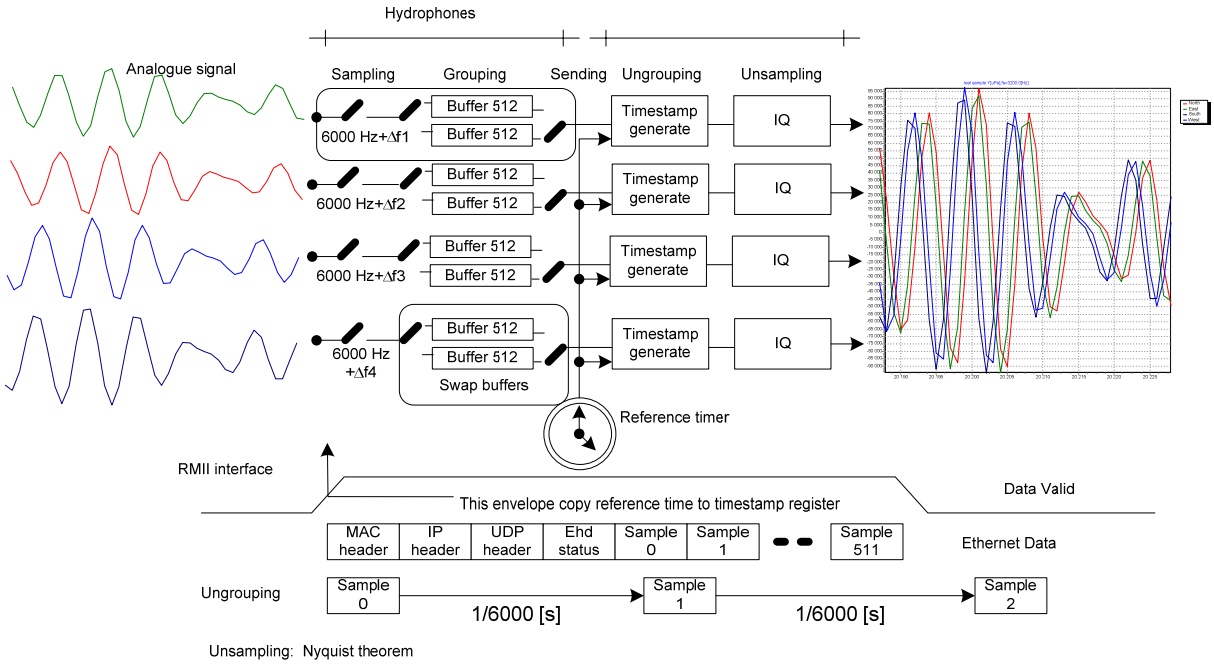

Fig.3. Application scheme, which utilizes special concentrator with reference timer

Presented on figure 3 system consists of 4 independent hydrophones, which generate digital output signal. The hydrophones convert the analog signal into digital samples with sampling rate of 6000 Hz (100ppm stability of quartz is guaranteed). The Ethernet frames containing 512 time samples are sent via UDP protocol. The connection point-to-point between host and hydrophones guarantees fixed delay of receiving frames. The Media Independent Interface (MII) makes possible to establish precise time of receiving frame, so time-stamp according to the reference clock can be determined. This enables the host system to synchronize the asynchronous Ethernet streams generated by four hydrophones. Each sample of the frame can be synchronized based on the frame time-stamp and sampling frequency. The synchronization error resulting from instability of samples capturing is negligible.

The synchronized samples generated by particular hydrophones can differ about some time shift. This time shift can be eliminated by the reconstruction of analog signal obtained from each hydrophone according to Nyquist's theorem. Then the analog signals can be synchronously converted into digital samples. The close approximation of analog signal is significantly oversampled digital signal. The simplest solution of this method is Cascaded Integrator Comb (CIC) Interpolator or Hogenauer's filter.

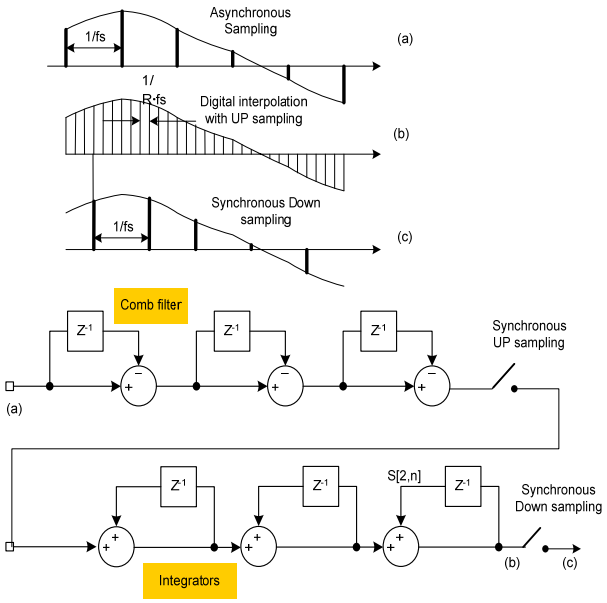

Fig.1. CIC Interpolator

Figure 4 presents different points of Hogenauer's filter wave against the background of analog signal. This method is simple on condition that the samples are captured in real time. In the case of UDP frames only the first sample is real time. Luckily the essential result of parametric methods is to generate of narrowband complex signal. Therefore the first incoming sample takes down the phase relating to reference generator. The time-stamps for other samples are also calculated. Then the I/Q detection, with time resolution results from oversampling (T/Rup) is performed, as presented on figure 5. This operation transforms time sample into complex ones. Next the samples are filtered by low-pass filter. The information about the time shift is slow-running so can be sampled at lower frequency.

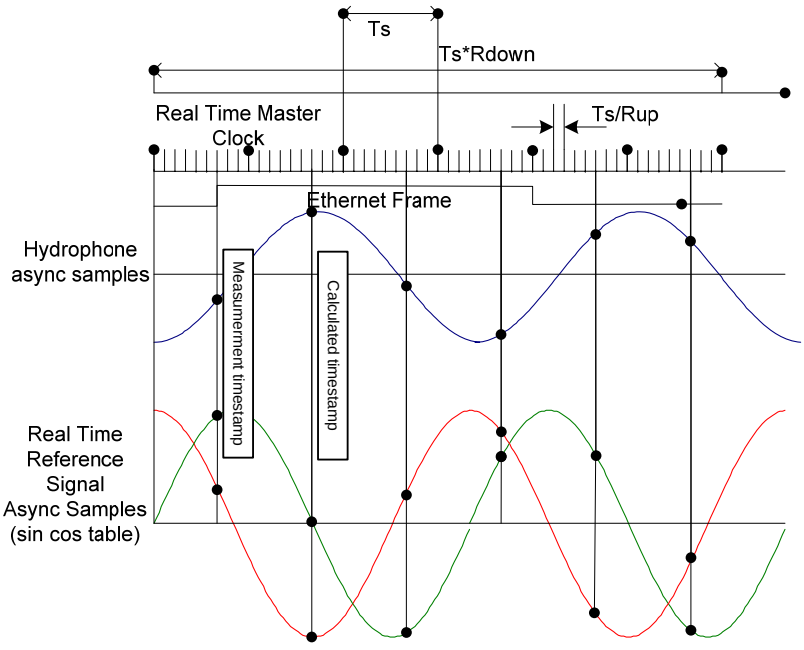

Fig.2. Synchronization process based on real-time reference signal

The synchronous sampling process of slow-running signal with sampling period Ts*Rdown is correct on condition that the pass of low-pass filters meets inequality:

$$B<0.5/(Ts*RDown) \quad (3)$$

The digital filter implementing this function is also the Hogenauer's filter.

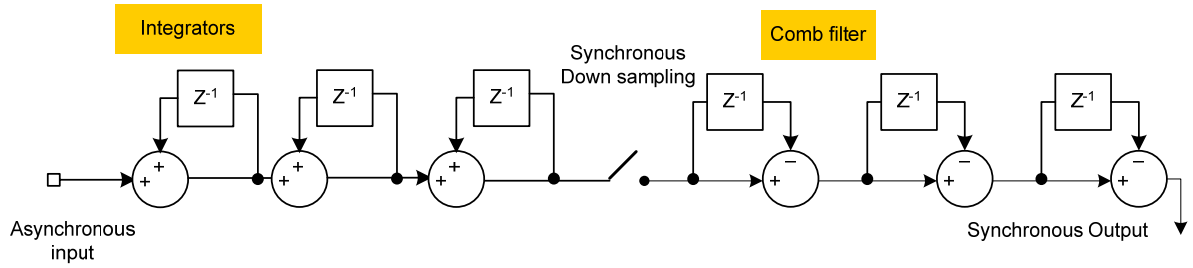

Fig.3. CIC Decimator

The signal „synchronous output" is saved into cyclical buffer at appropriate address. The address is calculated according to the resolution of real time (Ts*Rdown). So data gathered from each cycle buffer at the same address generates the complex vector.

4. THE IMPLEMENTATION OF SYNCHRONIZATION ALGORITHM BASED ON FPGA.

Fig. 7 presents the synchronization block based on Virtex-5 FPGA (Field Programmable Gate Array). The FPGA is composed of reconfigurable blocks connected according to user requirements.

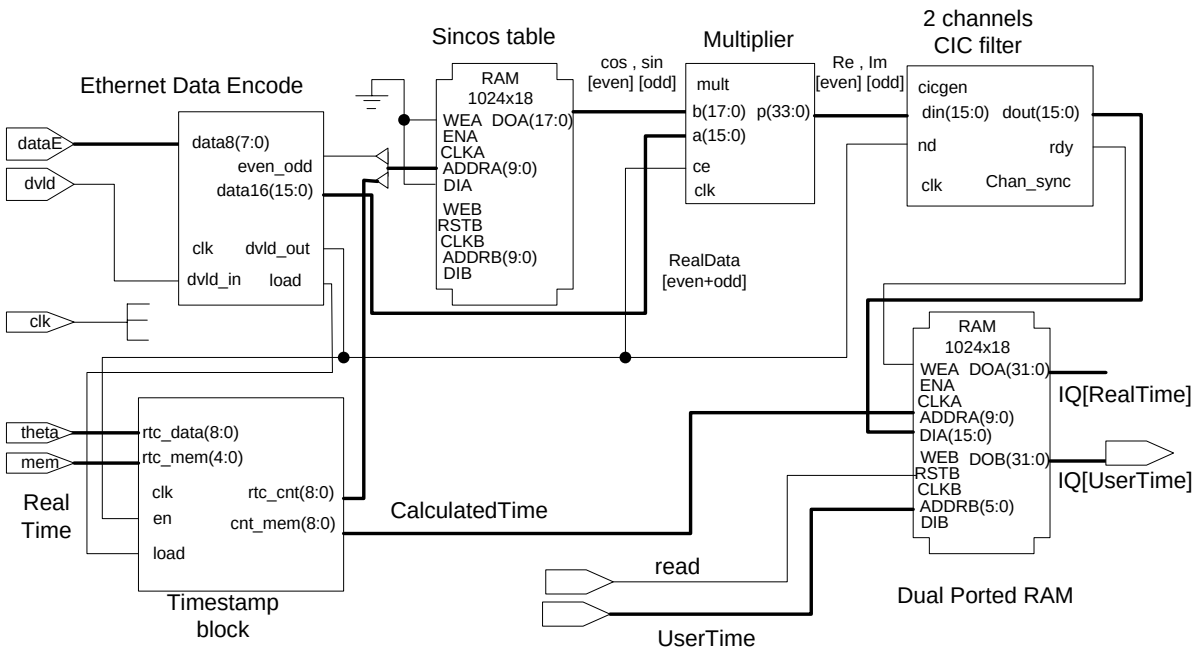

Fig.4. FPGA implementation scheme of synchronization process

The „Ethernet Data Encode" block is clocked by "clk" signal. The 8-bit input data (data8) income on every rising edge of the clock. This block combines two input data (data8) into one 16-bit digital sample (data16). So the output sample changes on every second rising edge of the clock. The "even_odd" signal also change state on every second rising edge of the clock to distinguish even and odd clock cycles. The SINCOS table generates cosine component during even clock cycle and sinus component during odd clock cycle. The appropriate table addresses (rtc_cnt) for each sample is created by TIMESTAMP block. The rtc_cnt signal depends on time-stamp of frame and sample number. It is equal to time-stamp for the first sample in the frame. Whereas for each following sample this signal increases by the sampling period. Two channel Hogenauer's filter was generated base on CIC_compiler v1.2. This block calculates I/Q demodulator components during the even and odd cycle of the clock respectively. The output data are saved into local memory (Dual Ported RAM) at appropriate addresses. The addresses are calculated exactly as SINCOS table addresses. The user can read complex sample captured at any real-time.

5. CONCLUSION

The distributed measurement system should combine the advantages of presented methods. The hydrophone's microcontroller should sample analog signal with timing synchronized by IEEE1588 standard. Then the time sample ought to be converted via IQ detection into complex ones. These samples can be sent using UDP protocol. The common cable between the host and hydrophones can be utilized when hydrophones send data only in appropriate time window. This data streams from hydrophones form a measurement vector adjusted to parametric calculation.

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