ACOUSTIC PROCESSOR OF THE MINE COUNTERMEASURE SONAR

MARIUSZ RUDNICKI, JAN SCHMIDT, ALEKSANDER SCHMIDT, WOJCIECH LEŚNIAK

Gdansk University of Technology
Faculty of Electronics, Telecommunication and Information
Department of Marine Electronics Systems
Gabriela Narutowicza 11/12, 80-233 Gdansk
mariusz.rudnicki@eti.pg.gda.pl

This paper presents the concept of an acoustic processor of the mine countermeasure sonar. Developed at the Department of Marine Electronics Systems, Gdansk University of Technology, the acoustic processor is an element of the MG-89, an underwater acoustic station. The focus of the article is on the modules of the processor. They are responsible for sampling analogue signals and implementing the algorithms controlling the measurement cycle and digital signal processing. As it performs the above functions, the device should be highly reliable and resistant to mechanical and weather conditions and ensure a user friendly operation. The functions of the processor software should help with object detection and classification. The results of measurements should be displayed with the shortest possible delay in relation to sounding signals to allow the operator to take decisions quickly and establish if the object poses a risk. The article demonstrates that the acoustic processor designed for and used by the Navy meets these requirements.

INTRODUCTION

The design of mine countermeasure sonars is quite complex. In the classic architecture they consist of: operator console, acoustic processor, receiver block, transmitter block and array and array stabilisation system. From the perspective of sonar control and acoustic sounding signal processing, the acoustic processor is every sonar's most important element. This is because the device controls a number of commands which start emitting sounding pulses, change levels of gain, change array position, start the collection of measurement data and data processing.

This concept divides the processor block into two collaborating parts. The first one comprises two industrial computers with a VMEbus interface. This part is responsible for controlling the measurement process and communications with the other elements of the sonar system such as the receiver, transmitter and array position stabiliser. It also handles the presentation of measurement results following signal digital processing using a variety of displays. The software used here provides the operator with tools for target detection and classification. The tools are based on a number of visualisations and image processing algorithms. Designed and built by the Department of Marine Electronics Systems, the second part of the processor comprises a multichannel analogue-to-digital converter module and DSP processor board, both working together. The A/D converter module samples analogue signals and makes sure that the right data series are selected for further digital processing. The DSP module gives commands to start sampling and runs algorithms of digital signal processing. The block diagram of the acoustic processor is illustrated below.

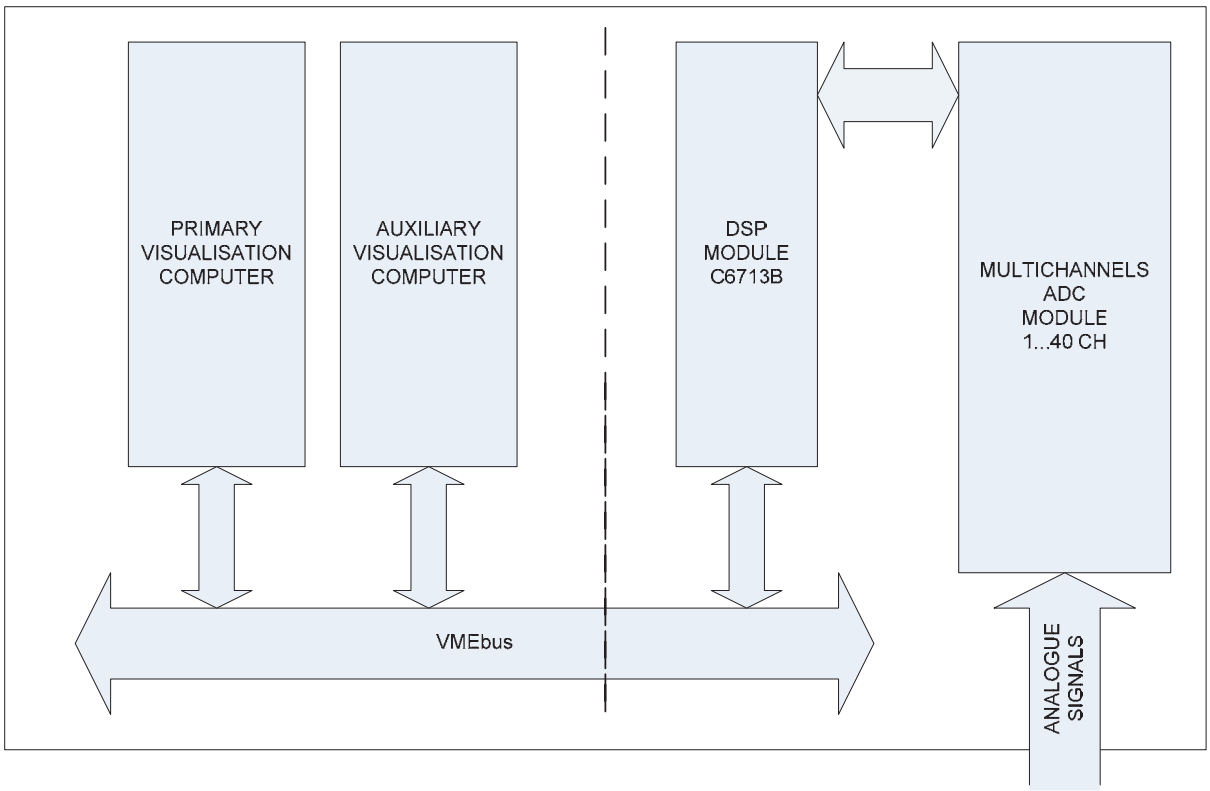

Fig.1. Block diagram of the acoustic processor.

1. MULTICHANNEL ANALOGUE-TO-DIGITAL CONVERTER MODULE

Once received by the array, analogue acoustic signals are fed to receiver inputs, amplified and transferred to the multichannel analogue-to-digital converter module. Fig. 2 shows its block diagram. The card comprises 40 identical channels of analogue-to-digital conversion. Each channel has a sample & hold unit at the start. An analogue sample from the unit's output is fed to the A/D converter input where it is converted into a 14–bit digital sample. Next, digital data are sent via a Serial Peripheral Interface Bus using an optic coupler to the FPGA matrix which has an implemented MADC card controller.

The card is able to sample up to 40 analogue channels simultaneously. All of the 40 conversion channels use the same CLK clock signal which controls A/D converters. The

"STC – Start conversion" signal is similar in that it determines the start of sampling for all channels. The signals are generated by the MADC card controller. Because the system uses phase relations between the signals from individual channels, this solution is particularly important for its operation.

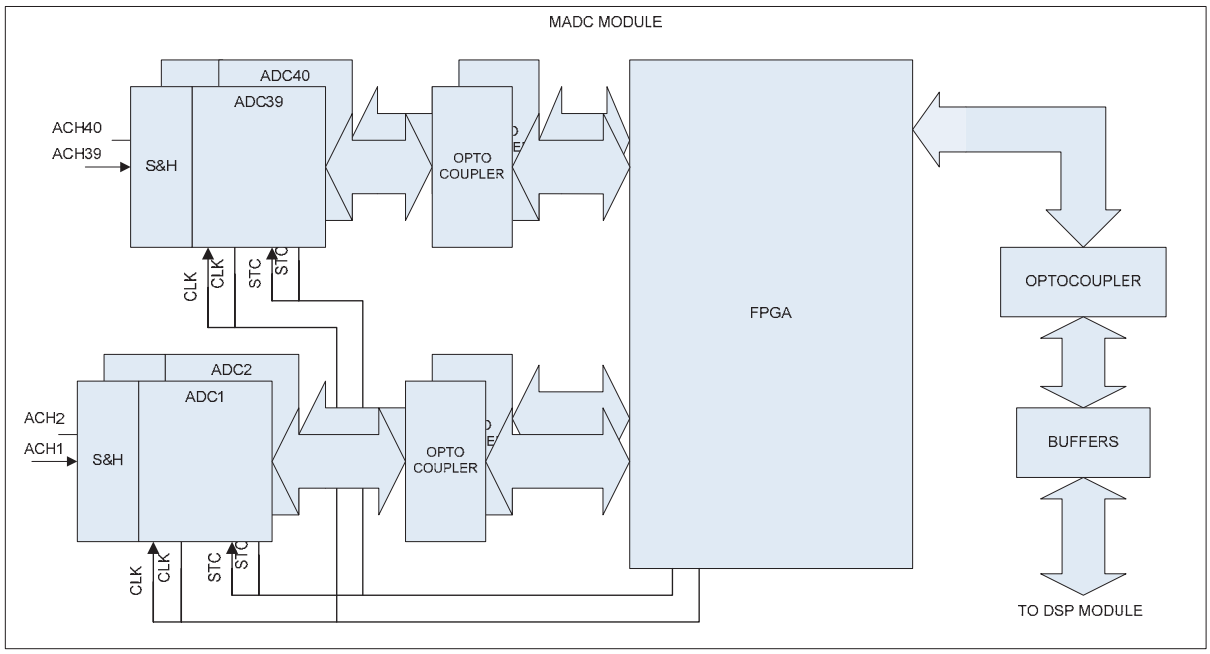

Fig.2. Block diagram of multichannel A/D converter module.

The acoustic processor in question uses 36 analogue-to-digital conversion channels.

Placed in the DSP module, the data processing algorithm is based on quadrature samples with complete information about echo signal and its phase. Conjugate samples are collected in a sequence that ensures that the frequency of sampling meets Nyquist criterion in relation to the sounding signal band.

The sampling sequence in the acoustic processor is as follows. All converters sample analogue signals with a frequency which is four times the carrier frequency of the sounding signal, i.e. f_s = 173,6 kHz. During the first two rates of sampling two signal samples are collected from the first channel. The time interval between the samples is equal to ¼ of carrier frequency duration. During the subsequent two rates quadrature samples are collected from the second channel, and in the next two rates they are collected from the third channel. The next two rates after that perform sampling from the first channel and the sequence is repeated through the entire time the echo signal is watched for the specific range of distance. The sequence is performed on twelve three channel groups of signals. As a result, the echo signal in each channel is sampled in quadrature every 3/2 of carrier frequency duration.

The data used for further processing comes from every third data series which significantly reduces their number. This can be done due to oversampling in relation to the width of the echo signal band. Next, samples obtained from conversion are converted in a serial-parallel shift register defined in the FPGA matrix. The register's operating diagram is illustrated below.

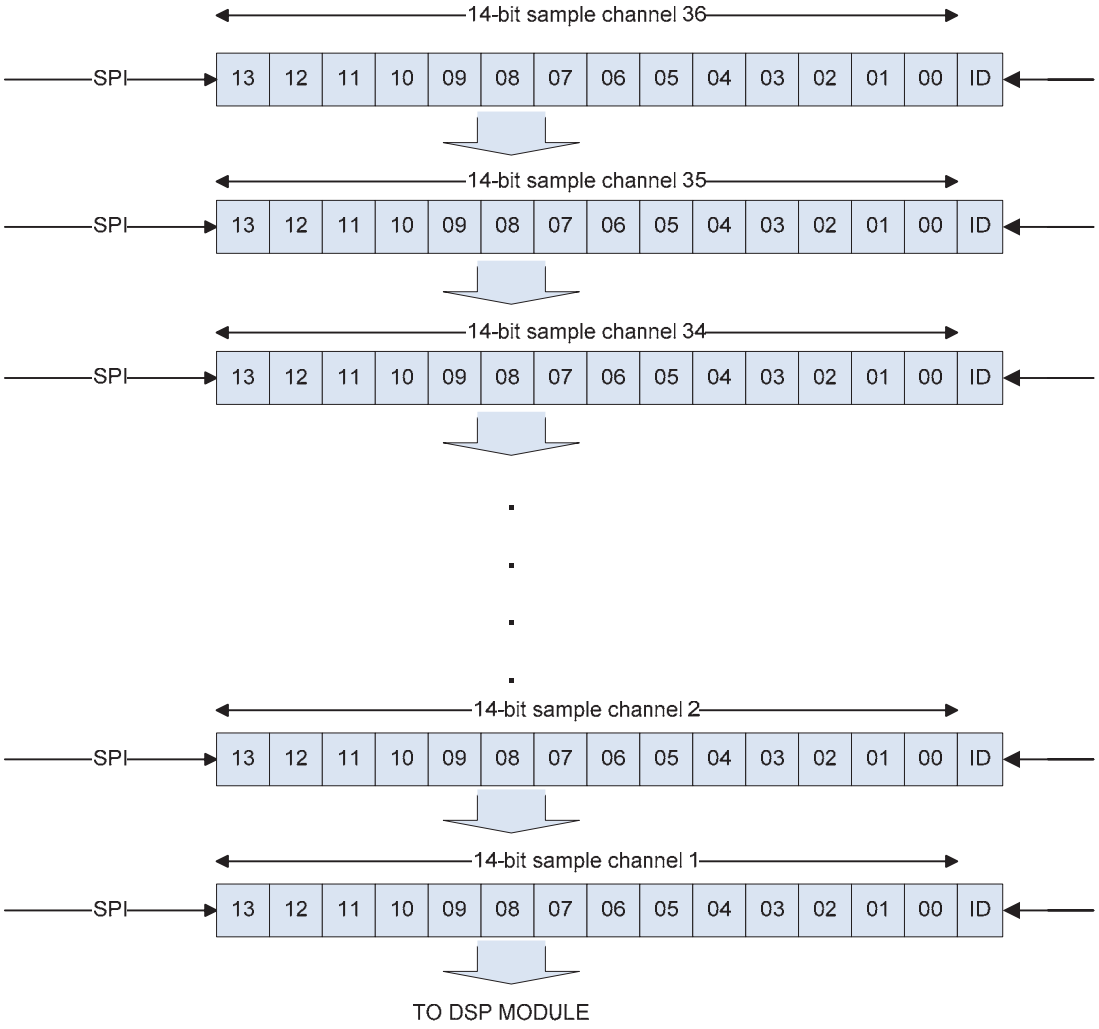

Fig.3. Serial-parallel shift register.

As already mentioned, oversampling of analogue signals means that data processing algorithms use every third data series. The sequence of selecting the right samples is performed in the FPGA matrix. Each of the 36 samples is assigned a marker identified as "ID" in the figure above. The field of the marker is set to the logical value of "1" when the sample is important in the specific cycle of conversion. Once the FPGA matrix has read all samples, the data are transferred from the shift register to FIFO memory on the DSP module's board. The only samples transferred to the memory are those whose marker is set to the logical "1". The way it works is that as shift register data are read out in the subsequent cycles, channel 1 register is read every time. When read out, the content is overwritten with channel 2 register value which is then replaced with channel 3 register value. The overall sequence of register data rewriting is as follows:

$$Rejestr_{k(n)} = Rejestr_{k(n+1)}, dla\ k = 1,..,35$$

This is made possible thanks to a very short time of digital signal propagation in the FPGA matrix, a mere 4ns. As can be easily calculated the theoretical time needed to rewrite all samples in the shift register is only 144ns and significantly less than the interval between the subsequent sampling moments of time which in the system in question is equal to 5,76µs.

The communications interface between the MADC card and DSP processor board is based on LVDS technology. LVDS buffers convert binary unipolar signals into differential form which is more resistant to interference. This solution ensures that data exchange and commands controlling the MADC module remain secure.

2. DIGITAL SIGNAL PROCESSING MODULE

The processor's digital signal processing card has the following functions: it processes measurement data based on the algorithms of the beamformer, low pass digital filters and high pass anti-reverberation filters and sends processed data to visualisation computers via the VMEBus. The illustration below shows the block diagram of the DSP module.

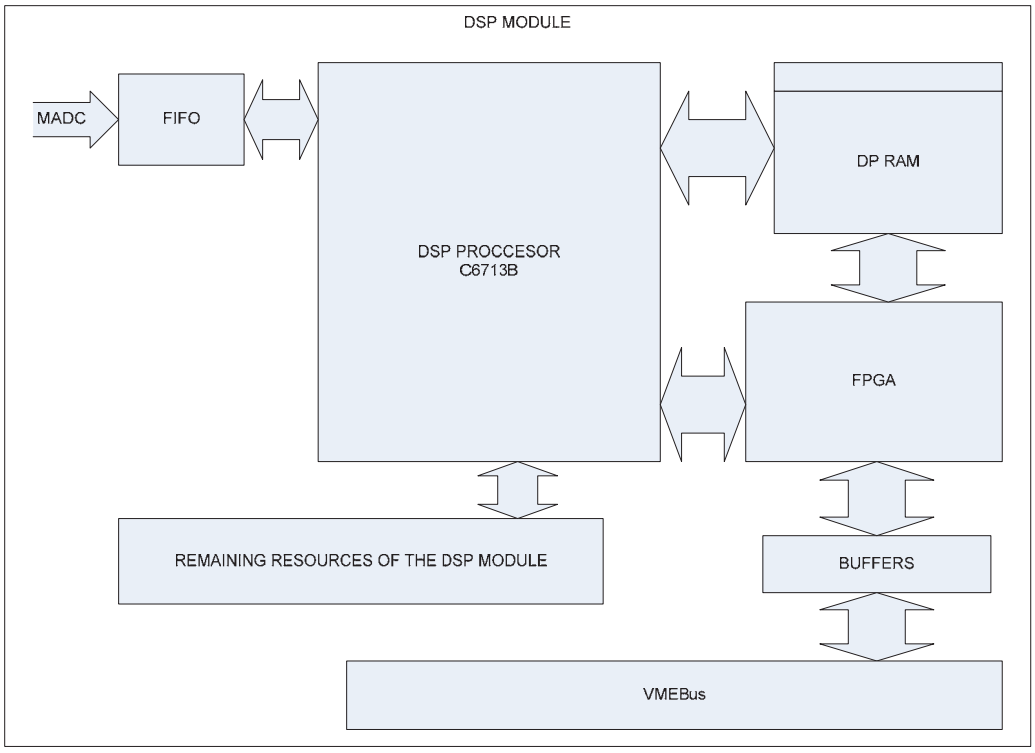

Fig.4. Block diagram of the digital signal processing module.

The digital signal processing module's CPU is a Texas Instruments TMS320C6713B DSP processor with a 300 MHz clock. The signal processor's peak computational power is 1.8 GFLOPS. It has 64MB of dynamic memory and 1MB of FLASH memory (programme memory). The DSP's other important elements include a Dual-Port RAM memory and a Xilinx FPGA matrix from the Spartan 3 family. A data buffer the size of 512K x 36 bits was implemented in the Dual-Port RAM. It is used for exchanging processed measurement data between the DSP and visualisation computers. The memory area can be seen in the DSP's address space and from the VMEBus. The buffer can store processed measurement data from the longest measurement range. This has made it possible to read the resulting data via the VMEBus as a single continuous block. The advantage of this is that the data exchange protocol is kept simple. Visualisation computers communicate with the DSP module via the FPGA and its VMEBus. The following functional modules are defined in the bus: Slave and Interrupter. The interface supports referrals to the DSP card in the A16/D32 mode – access to the card's general registers and in the A32/D32 mode – access to Dual-Port RAM. Data are

exchanged between the DSP and visualisation computers using a cycle of block data transmission BLT – Block Transfer Cycle pre-defined in the VMEBus ANSI – 1014 1987 specification. The DSP notifies visualisation computers that they can collect measurement data using an interruption generated on the VMEBus.

Signal processing in the DSP modules in the majority of sonars involves a digital phase beamformer using conjugate samples. Analogue phase beamformers must use phase shifters. The more beams we want the beamformer to produce, the more phase shifters we need. The digital beamformer achieves this by replacing phase shifters with an adequately high number of mathematical operations on quadrature samples of echo signals. To move the phase of a sinusoidal signal represented by its quadrature samples, we must change the proportion between sine and cosine samples. The samples are multiplied by coefficients whose value (in the version without amplitude weighting) is equal to the sine and cosine from the desired phase shift. Next, the results of the multiplication are added and the result is sine and cosine samples with the phase changed. Following this transformation, the sine and cosine samples in 36 channels are summed up. The end result is one sine and cosine sample in each sampling cycle. The root of the sum of the squares of these samples is proportional to the value of the adequate beam pattern and the specific angle of wave incidence.

With the DSP equipped with 4 independent ALU units for floating point operations, we can significantly accelerate the computations by using the FFT algorithm for spatial frequencies. This is the solution applied in the acoustic processor. The downside of the FFT algorithm is the non-linear distribution of beam deflection angles which means having to adopt a linear distribution of phase shifts (rather than a sinusoidal one). What this means is that beams are not exactly 1° apart but given the 3° beam width, it is of no practical importance.

The FFT algorithm involves spatial frequencies and calculating their spectrum using Fourier transform. We can see that signal samples at array outputs have a sinusoidal pattern of a certain frequency. That frequency depends on the angle of wave incidence which gives it the name of spatial frequency. If we perform DFFT transform on signal samples, the result will be a discreet spectrum. The lines of the spectrum are assigned to specific spatial frequencies, i.e. to the angle of wave incidence to the array. The maximal value is reached by those lines which match the angles of wave reflected off targets. When calculating the DFFT transform from 36 conjugate signal samples, we would only receive 36 spectral lines, i.e. 36 distinct directions that match the beam patterns of an analogue beamformer. To increase the number of lines (beams) and improve the sonar's angular resolution, zero samples are added to the sequence of samples. As a result, in the algorithm used here the number of samples went up to 128, generating the desired number of 61 beams in a 60^0 angular sector. The number of samples could also be adjusted to meet FFT requirements. The shape and width of a single beam is the same as in the analogue beamformer which is the result of Fourier transform properties.

The next operation performed in the DSP module which is also part of the digital beamformer algorithm, is amplitude weighting of echo signals to reduce side lobes. The pattern of weighting is the same as in the transmitter. Amplitude weighting is performed by multiplying the values of sine and cosine samples by weight coefficients. The theoretical level of side lobes in digital beamformer patterns is –18 dB. In practice a slightly higher level of side lobes was applied as a result of sensitivity distribution of the different array elements.

In the next stage of processing, beamformer generated digital signals are filtered in digital low pass filters to improve the signal to noise ratio. Three basic low-pass filters are used with maximally flat amplitude patterns (Butterworth filters). They are filters of the 8^{th}

order with infinite pulse responses. The filter's transfer band depends on the duration of the sounding signal and amounts to 5 kHz for a 4 ms pulse, 2 kHz for a 10 ms pulse and 1 kHz for a 20 ms pulse.

In addition, the data processing process included anti-reverberation filtration which involves strong attenuation of low frequency components of echo signals received. This was achieved using attenuation filtration for very low frequencies. The width of an attenuation band is selected to match the length of the sounding pulse and amounts to 100 Hz for a 4 ms pulse, 40 Hz for a 10 ms pulse and 20 Hz for a 20 ms pulse. A digital high-pass Butterworth filter of the 4^{th} order was used as an anti-reverberation filter.

Signals after filtration are processed to a form that can be understood by visualisation computers and then sent to that part of the processor which is responsible for visualising measurement results.

3. VISUALISATION OF MEASUREMENT RESULTS IN THE ACOUSTIC PROCESSOR

The results of data processing are presented in different forms on the primary visualisation computer and auxiliary visualisation computer. The system operator has a number of visualisations to choose from typically used in this type of sonar. When the sonar is detecting and classifying targets, the operator can use a visualisation that he finds most useful at that stage. Below are some examples of visualisations.

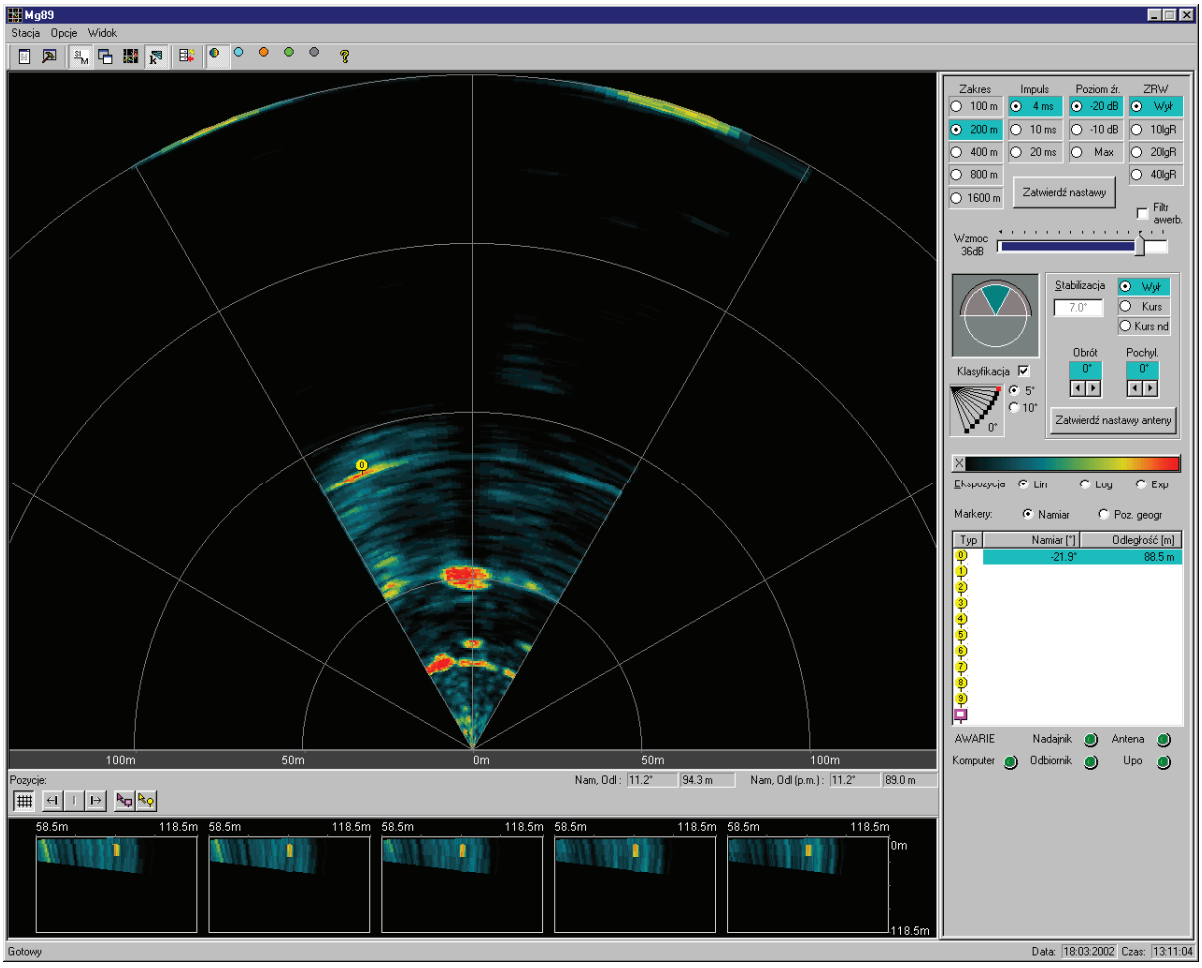

Fig.5. Primary visualisation with an additional visualisation during classification.

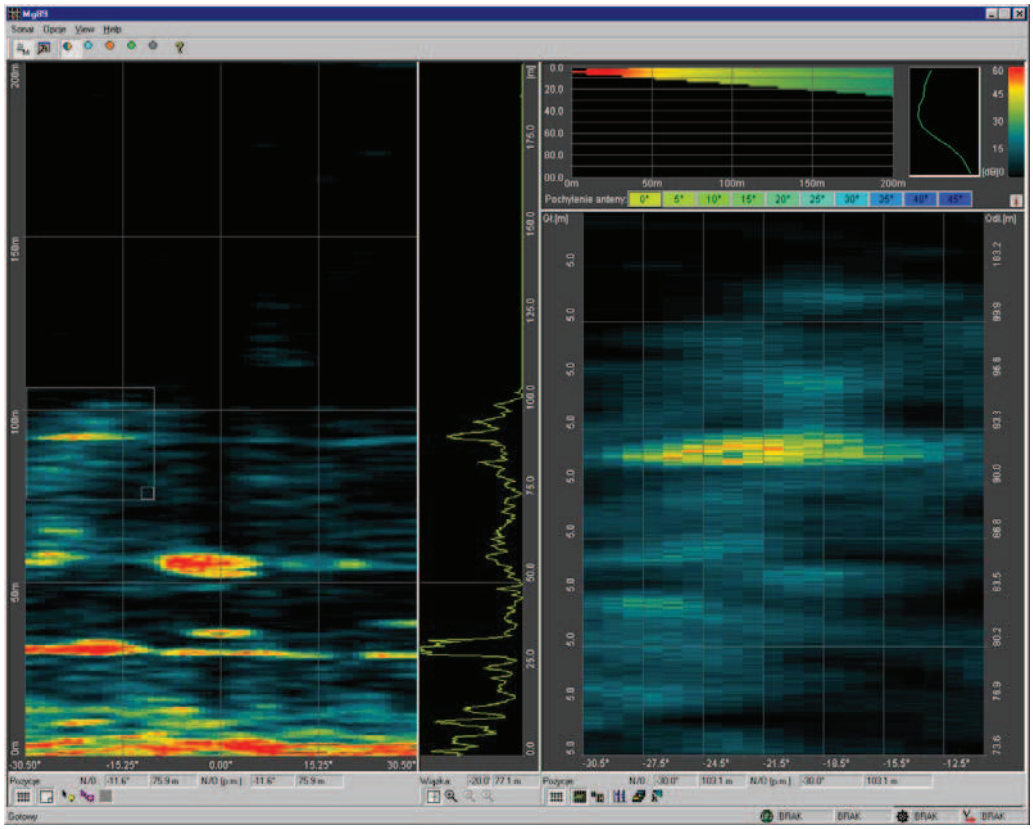

Fig.6. Auxiliary visualisation.

4. CONCLUSION

The acoustic processor described in the article is used in a number of mine countermeasure sonars operated on the Navy's ships. Over the years it has proved to be very useful for detecting and positioning bottom and pelagic mines. Sonar operators are very happy with its practicality, ease of use and reliability.

REFERENCES

[1] R. Salamon, Systemy echolokacyjne, GTN, s. 580 – 629, s. 759 – 769, Gdansk 2006.

[2] R. Salamon, J. Marszal, Optimiasing the Sounding Pulse of the Rotational Directional Transmission Sonar, ECUA2002, s. 295-300, Gdansk 2002.

[3] R. Salamon, M. Rudnicki, J. Schmidt, Hydroacoustics, Volume 5/6, s. 251 – 260, Gdynia 2002/2003.

[4] A. Raganowicz, L. Kilian, Z. Ostrowski, Special forms of echo visual representation in an ahead looking sonar, Volume 5/6, s. 47 – 52 , Gdynia 2002/2003.

[5] W. Leśniak, J. Marszal, R. Salamon, K. Zachariasz, J. Schmidt, Method for improving multibeam sonar bearing accuracy, Hydroacoustics 2009 - Vol. 12 s. 99-108.

[6] L. Kilian, A. Raganowicz, Evolution of imaging forms in acoustical echolocation systems, OSA, s. 65-69, Gdansk 2004.

[7] L. Kilian, J. Marszal, A. Raganowicz, Komputerowa symulacja zobrazowania efektów sondażu czołowego i bocznego, OSA, s. 157-162, Rzeszów-Jawor 2000.