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COMPACT MODELING OF LOW-POWER AND RF ANALOGUE MOSFET DEVICES

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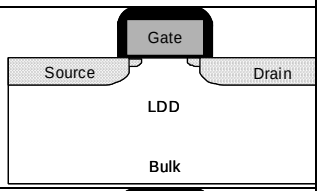
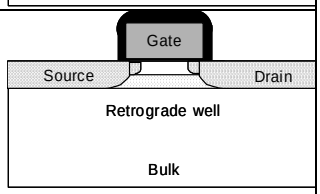
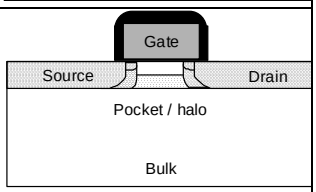
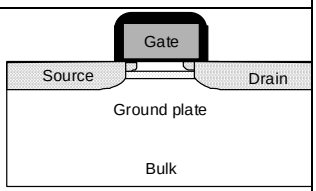
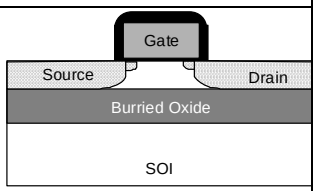
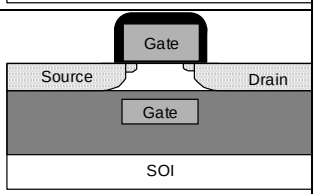
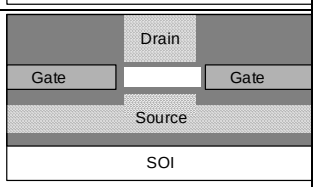
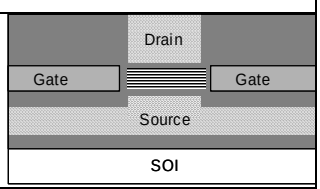
ABSTRACT

The technology of CMOS very large-scale integrated circuits (VLSI's) achieved remarkable advances over the last 25 years and the progress is expected to continue well into this century. The progress has been driven by the downsizing of the key devices: MOSFETs. Approaching these dimensions, MOSFET characteristics cannot be accurately predicted using classical modeling methods currently used in the most common MOSFET models such as BSIM3/4, EKV v2.6, HiMOS, MOS9 etc., without introducing large number of empirical parameters. Various physical effects that are needed to be considered while modeling UDSM devices: quantization of the inversion layer, mobility degradation, carrier velocity saturation and overshoot, polydepletion effects, bias dependent source/drain resistances and capacitances, vertical and lateral doping profiles, etc. In this paper, we will discuss the progress in CMOS technology and anticipated difficulties of the sub-0.25μm VLSI downsizing. Subsequently, basic MOSFET modeling methodologies that are more appropriate for low power and RF analogue applications of UDSM MOSFETs will be presented as well.

1. Advances in CMOS Developments

Over the last 25 years, technology of CMOS very large-scale integrated circuits (VLSI's) has achieved an advanced stage. However, even before the downsizing of the VLSI devices reaches its fundamental limits this process is expected to encounter severe technological and economic problems when the minimum features of the active devices are going to shift to dimensions below sub-quarter micron, the so called ultra deep submicron (UDSM) technology. This downsizing allows to minimize transistor dimensions and increase number the number of devices per a chip increases. Thus, the functionality, switching and operation speed of the VLSI's circuit is improved. Indeed, these continuous technology improvements are correctly predictable according the Moore's law [1]. Moreover, at the research level, more than several institutions have already reported successful fabrication of sub-0.1μm MOSFET devices operating at room temperature. As indicated in Fig. 1, for most aggressively scaled DRAM, the integration scale will reach 256Gbits by the year 2010 [2]. There seems to be no physical limitations for feature size down to 25nm. Furthermore, there are no apparent fundamental limits for silicon devices, in terms of tunneling and other quantum mechanical effects for the features size. The challenges to surmount these problems encompass almost all aspects of the device physics, processing, and integration including interconnection and patterning technologies. In long term, as the semiconductor feature size reaches the atomic limit, alternative means for computation will be needed to further increase the information throughput. This great success has been achieved with the scaling methods in miniaturizing MOSFET's down to gate lengths of 0.18μm at the VLSI product level and 0.01μm at the research level, respectively. However, the actual scaling of the parameters has been different from that originally proposed [3]. The major difference is the supply voltage reduction. The supply voltage was not reduced in the early stage of the VLSI generation in order to keep a compatibility with the supply voltage of conventional systems and also to obtain higher operation speed at higher electric fields. The supply voltage started to decrease at the level of 0.5μm CMOS processes due to the electric field across the gate oxide exceeding values of 4MV/cm. This level is regarded as the maximum limitation in terms of time-dependent dielectric breakdown and hot-carrier induced degeneration for short channel transistors, generally speaking reliability issues of the MOSFET devices. Now,

Table 1. Scaling problems and possible technology solutions

Scaling Problem	Solution	Technology	Architecture
Hot electrons degenerate gate oxide and reduce device reliability	Reduction of the high electric potential drops in drain region	Additional lightly doped drain (LDD) ion implantation	
Subsequent increase of the channel doping increase S/D capacitances	Decoupling of both parameters through additional vertical implantation in the substrate	The retrograde well using additional implantation in the substrate	
Parasitic leakage currents in the substrate (punch through). The potential barrier at S/D junction is reduced by high potential (DIBL)	Higher doping concentration increases S/D potential barrier	Introduction of the pocked/halo implantation step	
Complex and difficult to control implantation steps introduces large variations of the process related device parameters	Substitution of the ion implantation by well controlled thin layer deposition	Improved MBE and/or CVD process steps	
Bulk MOSFET are difficult to scale because of very complex implantation profiles	Substitution of the classic pn-junction by a insulator barrier	Bulk Si wafers are replaced by SOI wafers with buried oxide	
Limit of the optical photolithography (alternative lithography systems are not ready)	Introduction of the 3D planar processes (Double Gate MOST) GAA(Gate all around)	Buried Si-SiO_2 interface as additional channel region	
Lithography of the planar structures are no more possible (constant channel length)	FinFET devices Lithography independent channel scaling using thin atomic layers	Vertical Double Gates are defined channel by thin atomic layers	
Classic MOST are not scalable. MOST operation is dominated by quantum effects	New quantum level devices (i.e. based on the tunnel barrier)	Multi tunnel junction (MTJ) technologies	
Atom level scaling (?)	Optimum of the Si technology is reached	Additional improvements of the IC performance are possible only on an algorithmic level.	

however, it is not easy to reduce supply voltage because of difficulties in reducing the threshold voltage of the MOSFET. Too low threshold voltage leads to significant subthreshold leakage current and enforcing designers to design ICs operating in moderate inversion regime. The supply voltage, higher then expected from the original scaling rules, is one of the reasons for the increased distributed power [2]. An increase of the number of transistors in a chip by more than factor of K2 is another reason for the power increase. In fact, the transistor size decreased by a factor 0.7 while the transistor area decreased by a factor of 0.5 for every generation. Present complex digital designs cannot wait for the downscaling and the actual chip size has increased by factor of 4, more than predicted by standard scaling rules. Introducing new technologies such as multilayer interconnections, double polysilicon and further complicated cell structures for the memories partially solves the problem of insufficient IC area.

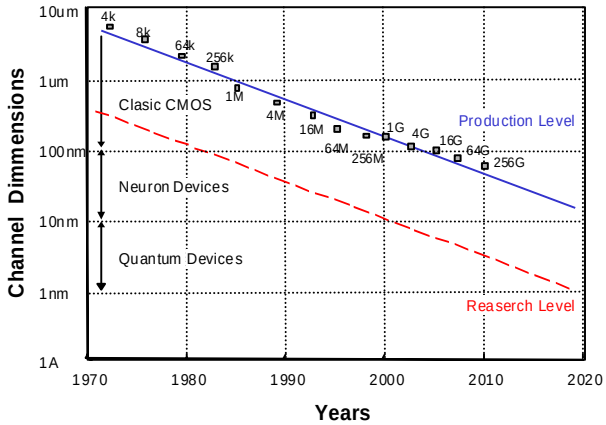


Fig. 1. Trends of the MOSFET gate length scaling in advanced VLSI technologies [2].

Recent progress in the CMOS scaling has been achieved through the use of improved DUV lithography tools. Originally, targeted at the 0.35µm devices, these tools were successfully introduced at 0.25µm level and are being used in the current 0.18µm generation. The use of these tools is projected at least for 0.15µm devices. Further progress is required to adapt popular reticle enhancement techniques (RETs) such as proximity correction and phase shift mask (OPC/PSM) to obtain improved packaging densities. From the extrapolation of traditional scaling, UDSM devices are expected to have excellent drive current and the projected performance suggests circuits operating at frequencies up to 10GHz. On the other hand, one should remember that there are serious technological and economic limitations for further, accelerated improvements of the standard CMOS technologies and the transistor performance could be, to some extent, compromised. In aggressively sized technologies, oxide scaling leads to rapidly increased gate currents, regardless of the oxide quality. Further improvements in the reduction of the gate tunneling currents require the use of alternative gate dielectric materials. High-k materials are good candidates to replace standard gate oxides. Similarly, potential solutions (e.g. low energy implantation) for advanced source/drain extension engineering, which would approach the physical limit of ultra-shallow but low-resistance junctions, have been discussed in the literature.

2. Compact MOSFET modeling

As previously mentioned, in aggressively scaled UDSM technologies, the gate oxide thickness is approaching the inversion layer thickness resulting in high fields at the silicon surface. These high electric fields at the surface cause various physical effects such as quantization of accumulation/inversion layers (QM effect), carrier saturation velocity and velocity overshoot that must be taken into account while developing UDSM transistor model. Other physical effects, which are additional to the short channel effects are polysilicon gate depletion effect, impact of nonuniform channel doping profile on threshold voltage, bias dependent source/drain resistances and capacitances, drain induced barrier lowering (DIBL) are relevant to UDSM modeling, as well.

First of all, the regional approach, which is the most frequently used, combines different equations for different regions of device operation and then pieces them together by smoothing function to avoid eventual discontinuities. There are a number of advantages. Firstly, it allows for a simple implementation of the short channel effects using empirical relations. Then it offers relatively fast computation time, which is not always true for some models like BSIM3. Nevertheless, it has some disadvantages such as ignoring the inversion layer thickness and consequently the quantization the inversion layer. This leads to wrong deduction of the non-physical gate oxide thickness (T_{OX}) which in turn results in inaccurate capacitance simulations. The model scalability over the full range of available device dimensions (W, width and L, length) is rarely possible without so-called parameter binning. The binning is artificially introduced in to the model structure and usually generates discontinuities across the boundaries. Most common way of including L and W dependence on a parameter P is:

$$P = P_0 + \frac{P_1}{L} + \frac{P_2}{W} \qquad (1)$$

assuming that the model parameters are inversely proportional to L and W. However, a better binning scheme has been proposed in [4]:

$$P = P_0 + P_1\left[\frac{1}{L} - \frac{1}{L_{ref}}\right] + P_2\left[\frac{1}{W} - \frac{1}{W_{ref}}\right] + P_3\left[\frac{1}{L} - \frac{1}{L_{ref}}\right]\cdot\left[\frac{1}{W} - \frac{1}{W_{ref}}\right] \quad (2)$$

where: L_{ref} and W_{ref} are large reference device length and width, respectively.

To model UDSM technology processes, more and more parameters are introduced into models based on the regional approach. The increased number of adjustable parameters complicates the parameter extraction process and model usage.

Most of above mentioned shortcomings of the regional based models are solved using surface potential approach. The full operation range of the MOSFET device from weak inversion through moderate to strong inversion is described in a physical and continuous way. Artificial smoothing functions are not necessary. This physical description of the MOSFET characteristics is also most accurate because gate bias dependence of the surface potential is taken into account in a continuous manner. Unfortunately, the biggest disadvantage is that the surface potential needs to be solved at each bias point iteratively due to the implicit nature of the bias dependence of the surface potential. Thus, the drawback of this approach is computation time because of the iteration procedure.

The third approach is the hybrid approach, which combines regional and surface based methods to take advantages of both. The hybrid methodology allows the incorporation of all the essential physics of scaled UDSM MOSFET devices such as short channel and narrow width effects, reverse short channel effect (RSCE), bias dependent S/D resistances, and channel length modulation (CLM). Successful modeling of UDSM devices with channel length of 0.1μm has been reported.

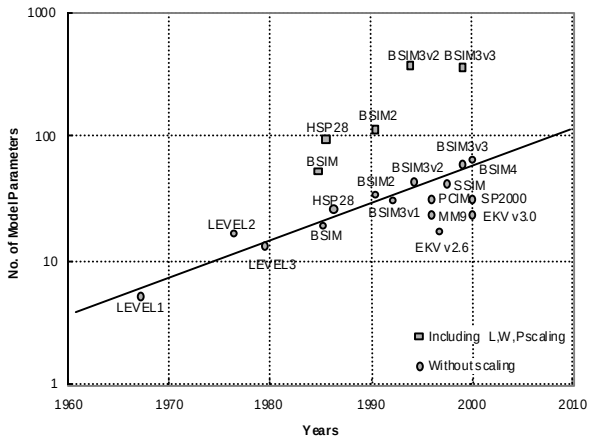


Fig. 2. Number of DC current parameters versus the year of the model introduction. Most recent versions of the EKV, SSIM, SP models are included.

Growing complexity of the most commonly used compact models (including recent versions of BSIM3 [5], MM9 [6], EKV [7], SSIM [8], SP2 [9–11]) can be clearly visible in Fig. 2, which shows also the increase of the number of the intrinsic DC parameters. This figure indicates that models are becoming more and more empirical rather than physical in their description.

3. Analogue CMOS modeling

A high performance UDSM CMOS technology has been developed with process modules allowing its usage as a base for a wide range of applications: from RF circuits to low power mobile ICs including non-volatile memory. Three core devices are provided in combination advanced technologies with ultra thin gate oxide and dedicated MOSFET transistor structure. These new devices have to be precisely modeled and special attention is needed while analyzing new UDSM effects.

3.1. Gate Current

As the gate length of UDSM devices is approaching 0.1μm regime, gate oxide thickness of sub-20Å prevails in CMOS processes [2]. Besides the benefits of high drive current and low DIBL effect, such thin oxide yields significant gate leakage current by various direct tunneling mechanisms [12], with undesirable effects on standby current as well as memory operation. Simple and accurate dielectric leakage model for MOS capacitors has been proposed [13]. Recently new gate dielectric leakage current model suitable for compact MOSFET models was introduced [14]. This model considers all three major leakage components (the gate-to-substrate leakage current; parasitic leakage currents through gate-to-S/D extension overlap region; and gate-to-inverted channel tunneling current) and also is accurate in direct-tunneling regime with excellent *Tox* scaling capability yielding satisfying test results.

3.2. Polydepletion effects

The presence of the polysilicon depletion layer in a MOSFET gate reduces the active region surface potential and the device current driving capabilities. The effect is emphasized by reduction of the gate oxide thickness and needs to be implemented into standard compact MOSFET model used in circuit simulators. The traditional approach is based on so-called regional model where both strong and weak inversion regions are modeled independently and only afterwards joined using artificial smoothing function to be able model a complete device IV characteristic.

A new polysilicon depletion model, which correctly predicts drain current, all transcapacitances as well as includes mobility reduction, has been recently published [15]. Figure 3 illustrates the new analytical model, which is compared to the numerical device simulation, and shows an excellent match for all bias conditions for all transcapacitances: C_{GG}, C_{DG}, C_{SG} and C_{BG}.

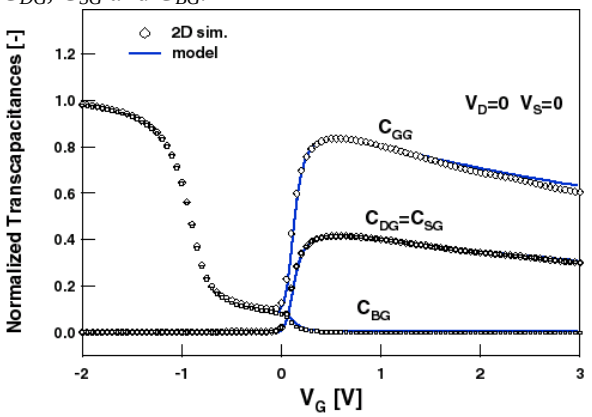


Fig. 3. Normalized transcapacitances versus gate voltage for n-channel device showing polysilicon depletion. The new analytical model (lines) is compared to 2D numerical devices simulation (markers).

An alternative as well as analytical approximation of the polydepletion effect on the surface potential in MOSFET has been proposed [16] and incorporated into new surface based compact MOSFET model.

3.3 New NQS models

The current gain of a MOS transistor is frequency dependent. For the operating frequencies approaching a device-dependent limit the current gain of MOSFET transistors begin to decrease. This effect is related to the fact that the modulation of the channel charge distribution due to fast varying external potentials can no longer be considered instantaneous. Thus, correct physics based modeling of these non-quasi-static (NQS) effects in the MOSFET devices is important to predict correct high-frequency behavior of the RF circuits.

Despite various efforts devoted to high frequency and transient modeling of the MOS transistor, using both numerical and analytical approaches for bulk [17–18] and SOI [31] devices, only incomplete sets of first-order NQS expressions were proposed for the kind of model discussed here [19]. A new model, published recently in [20], offers an exact analytical solution of small signal NQS behavior, valid in all modes of operation and from DC to high frequencies. This is derived from a general charge based approach and uses the framework of the EKV model. It has been demonstrated that only four independent transadmittances are needed to fully characterize the small signal operation of the device. All quantities in the model are expressed in terms of normalized variables, which are independent of the process parameters. Only six independent real parameters (four transcapacitances and two transconductances) are needed to fully describe the low frequency, small signal, behavior of the intrinsic MOS transistor. It is also important to note that the intrinsic transcapacitances are nonreciprocal but satisfy the charge conservation condition.

4. RF MOSFET modeling

Silicon RF integrated circuits are well established for applications up to 2GHz while for higher frequencies compound semiconductors technologies are widely used. While state-of-the-art silicon technologies are approaching operation frequencies of 10GHz range they become an interesting alternative for multi-gigahertz integrated circuits as they offers significant cost reduction compared to III–V technologies as well as compatibility with digital CMOS modules.

4.1 Subcircuit RF models

Several approaches have been proposed to improve RF performance of compact models by simple modification of the MOSFET equivalent circuit. Modifications that use additional substrate resistances along with bulk diodes and series gate resistances were studied [21–24] and are implemented as a simple equivalent subcircuit. Elements such as gate resistance R_g and bulk resistance R_b cannot be neglected in RF operation because they are essential in forming the real part of the Y-parameters. Note that in some simulators, R_g and R_b are already parts of the MOSFET model, so that a subcircuit definition specific to RF is not needed (Fig. 4) [23], [24]. For medium- and long-channel MOSFET's, R_g can be neglected compared to the bias dependent, nonquasistatic (NQS) effects due to the distributed nature of the channel. Although any charge-based MOSFET model intrinsically provides a first-order fit of the transadmittance (through the transcapacitances), consistent modeling of the NQS effects requires more specific extensions of the compact model, for which the analytical model formulation is particularly suitable [20].

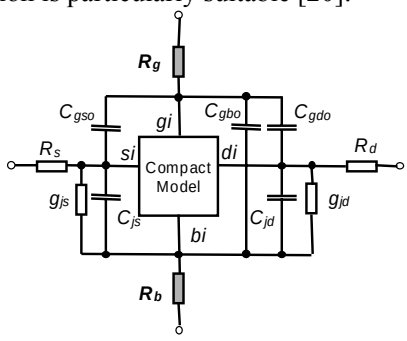


Fig. 4. Simple subcircuit RF MOSFET model includes additional gate R_g and substrate R_b resistances

A suitable compromise is obtained when simplifying the complete detailed equivalent circuit to the one presented in [25–32], which from experience has shown to be sufficient for most RF circuit simulation.

Note that all the terminal resistances as well as the substrate resistances are bias dependent. The bias dependence of the source and drain resistances is mostly due to the LDD regions. The bias dependence of the gate resistance is related to the distributed nature of the channel resistance and the oxide capacitance. The substrate resistance network may also be bias dependent accounting for the variations of the depletion regions below the poly gate and in proximity of the source and drain junctions.

4.2 RF and 1/f noise modeling

The noise modeling of the MOSFET devices is complex task because of different noise contributing together with their power spectral densities (PSD). They include: the noise at the drain, consisting of the channel thermal noise and flicker noise and the thermal noise of the S/D resistances and substrate region. The flicker noise mainly affects the low-frequency performance of the device and can be ignored at high frequency. In addition to the channel thermal noise at the drain, at RF the local noise sources within the channel are capacitively coupled to the gate and generate an induced gate noise [28–30].

5. Conclusions

The goal of this paper was to present advances in the VLSI technologies allowing the realization UDSM devices. Better understanding of the UDSM devices physics and MOSFET fabrication is required to continue compact modeling of these complex devices. As a result, the modeling community could provide better support for the analog and RF circuit simulation and analysis.

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