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Rapid Prototyping of Third-Order Sigma-Delta A/D Converters

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***Abstract*—Prototyping of third-order sigma-delta analog to digital converters (ΣΔ ADCs) has been presented in the paper. The method is based on implementation of field programmable analog arrays (FPAA) to configure and reconfigure proposed circuits. Three third-order ΣΔ ADC structures have been considered. The circuit characteristics have been measured and then the structure of the converters have been reconfigured to satisfy input specifications.**

***Keywords*—Sigma-delta converter, A/D converter, FPAA, MASH structure.**

I. Introduction

ADVANCES in VLSI technology result in manufacturing of mixed (digital and analog) circuits on a single chip. With increasing integration, the design and manufacturing of mixed circuits become very expensive and time consuming. Most of the ICs design tools are digital-oriented systems incorporating simulation, testability and BIST techniques which are hardly adopted to design analog part of the IC.

Whereas, functionality of analog circuits are usually simulated by the use of programs such as SPICE, before the circuit is manufactured. These tools are not adequate to design digital circuits. So the design and prototyping process of mixed signal systems is difficult and possible design errors may make the design and manufacturing processes emerge as a cost effective. A prototyping with reprogrammable devices may face the challenges for overwhelming cost effective manufacturing of the mixed signal circuits. Reprogrammable devices (CPLD and FPGA) are currently used as fast prototyping digital systems and some final application designs in digital circuits. There is a short list of programmable analog devices (FPAA). However they can be successfully used for prototyping of analog and some kind of mixed signal circuits [1]–[4]. Our idea was to build a cost effective mixed system with a help of FPAA. This method was introduced at ICSES'2012 [1], and the present publication is an extension of the paper included in the proceedings of the conference. As an example a ΣΔ analog to digital converter has been used to obtain prototype of the specified converter. For our work a FPAA device AN221E04 was used [4]. The AN221E04 device is based on switched capacitor technology. Its general structure is shown in Fig. 1. The basic CAB is composed of an OA surrounded by capacitor banks, local routing resources, local switching, clocking resources, global connection points and I/O pads.

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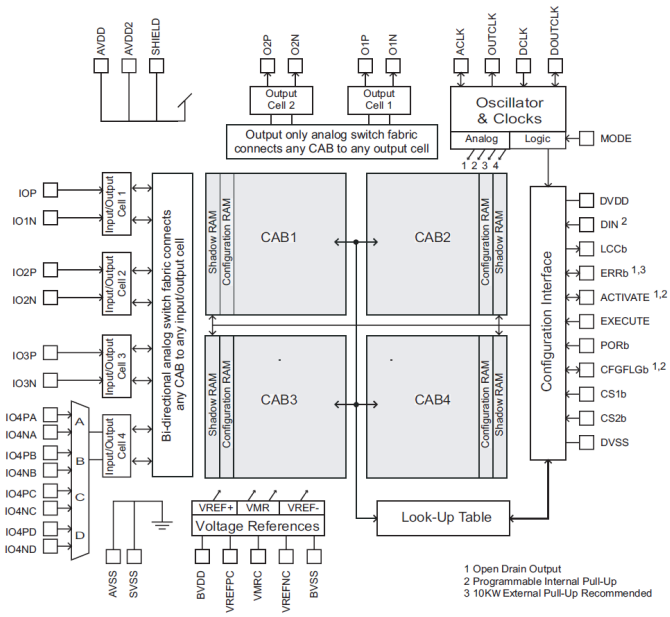

Fig. 1. General structure of the AN221E04 FPAA device.

II. ΣΔ ADC Structures

Sigma-delta modulators are analog oversampled circuits in which an analog input signal is sampled and converted to a single-bit digital stream. Oversampled converters have drawn considerable interest from integrated circuit designers as they offer high precision analog to digital conversion without requiring precision elements or accurate component matching. A number of high resolution and high speed monolithic ΣΔ converters have been realized in the past few years [5]–[8]. Their topologies comprise a series of integrators nested within multiple feedback loops. The number of integrators in the forward path defines the order of the modulator. Block diagrams of standard third-order, third-order feed-forward and multistage third-order modulators are shown in Figs. 2, 3 and 4, respectively.

The ΣΔ ADC performs analog to digital conversion and removes the quantization noise from the signal band of interest, by its noise shaping function. More efficient noise shaping can be obtained by increasing the order of the noise transfer function. The goal is to reduce the power spectral density of the quantization error in the band of interest, at the expense of increasing it at other frequencies, where it can be suppressed. Figure 2 shows the block diagram of a standard converter which implements a third-order modulator.

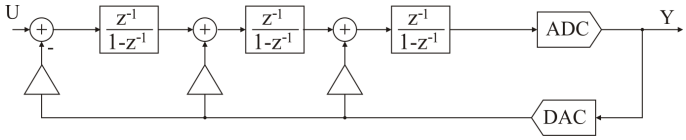

Fig. 2. A block diagram of standard third-order ΣΔ ADC.

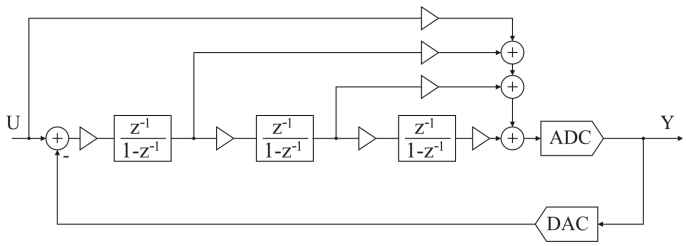

Fig. 3. A block diagram of third-order feed-forward ΣΔ ADC.

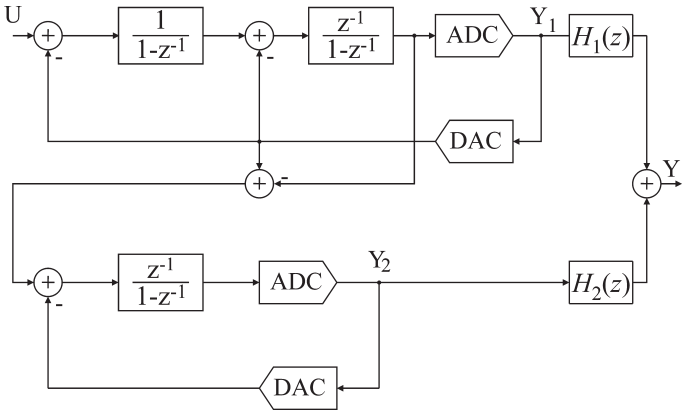

Fig. 4. A block diagram of third-order two-stage ΣΔ ADC.

In general, in this case, the Signal Transfer Function (STF) is:

$$STF = \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)} = z^{-3} \tag{1}$$

which consists of three delays, and the Noise Transfer Function (NTF) is given by:

$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} = (1 - z^{-1})^3 \tag{2}$$

In this way, the output signal for the ideal case can be written as:

$$Y(z) = U(z)z^{-3} + E(z)(1 - z^{-1})^3 \tag{3}$$

The output signal has only a pure delay in comparison with the real input signal $U(z)$, while the quantization error $E(z)$ will be pushed out of the output, as it passes through a third-order high-pass filter.

An alternative to standard ΣΔ modulator is an architecture using feed forward paths shown in Fig. 3. The feed-forwards paths are used to enhance a stability of converter, however, the noise transfer function efficiency is reduced.

Analysis of the linearised system shows that assuming an ideal DAC the ΣΔ modulator with the input-feed-forward path has the following signal transfer function:

$$STF = \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)} = 1 \tag{4}$$

and the noise transfer function:

$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} = (1 - z^{-1})^3 \tag{5}$$

the output signal for the ideal case can be written as:

$$Y(z) = U(z) + E(z)(1 - z^{-1})^3 \tag{6}$$

The loop filter $H(z)$ of input feed-forward ΣΔ ADC has to process the quantization noise only, while without the input feed-forward, the loop filter has to process the quantization noise in addition to the input signal. Distortion becomes independent of the input signal, which relaxes linearity requirements. However, the input feed-forward path presents a couple of complications, namely the reduced processing time and the analog adder at the quantizer input.

In the ΣΔ modulator without the input feed-forward path, the input-signal and the quantization noise are processed by the loop filter and feed to the quantizer. On the other hand, the input feed-forward path provides an alternate route for the input-signal. The processed quantization noise and the input-signal are then added just before the quantizer. Therefore, the quantizer inputs for both cases are similar. Furthermore, the loop filter is exactly the same for both cases. Therefore, there is no inherent tradeoff between distortion and noise performance in the modulator. The adder at the quantizer input adds thermal noise into the loop. However, noise injected at this point is greatly attenuated when referred back to the input and is therefore insignificant.

A different strategy of high order modulators is to use a multi-stage or MASH (Multi-stAge noise-SHaping) structure of the ΣΔ converter, which relies on the cancellation of the quantization noise. This structure improves the stability problems associated with higher-order modulators.

Using a linear approximation of the modulator in Fig. 4 wherein the quantization is modeled by signal-independent additive error sources, while the integrators are represented by their transfer functions in the z domain. $E_1(z)$ and $E_2(z)$ model the quantization error of the first and second-stage A/D converters, respectively. $E_2(z)$ also contains a representation of nonlinearity in the second-stage A/D converter, and $E_D(z)$ models the error resulting from nonlinearity in the multibit D/A converter in the second stage. A corresponding error source does not appear in the first stage because of the inherent linearity of the l-b D/A converter. The z transform of the output of the first-stage is:

$$Y_1 = z^{-1}U(z) + (1 - z^{-1})^2 E_1(z) \tag{7}$$

Thus, the output of the first stage includes the input to the modulator delayed by one sample period plus the second-order difference of the first-stage quantization error $E_1(z)$. The input to the second stage is $E_1(z)$ and the transform of the second-stage output is

$$Y_2 = z^{-1}(E_1(z) - E_D(z)) + (1 - z^{-1})E_2(z) \tag{8}$$

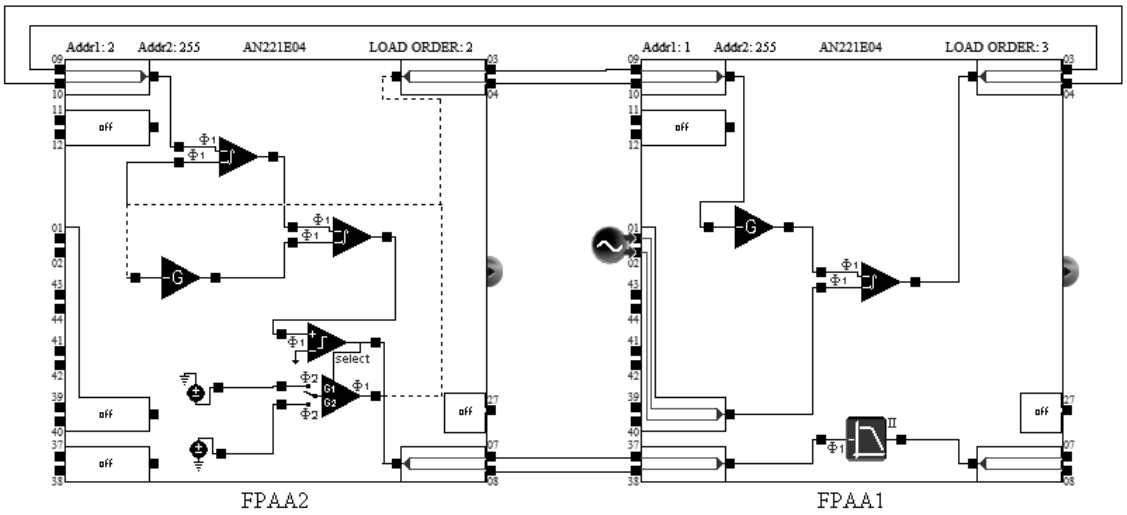

Fig. 5. Circuit realization of the standard third-order $\Sigma\Delta$ ADC.

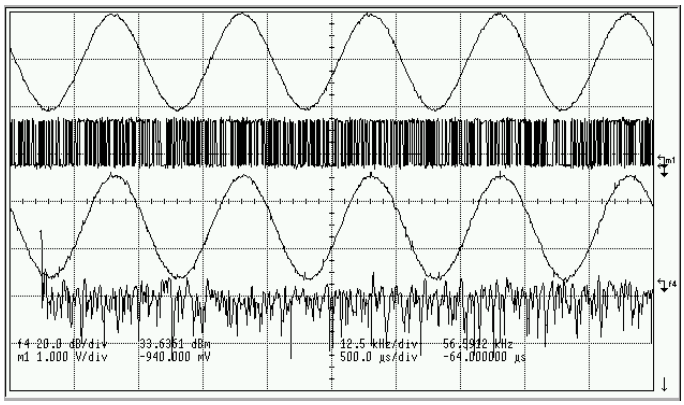

Fig. 6. Sinusoidal input and output waveforms of the standard third-order $\Sigma\Delta$ ADC.

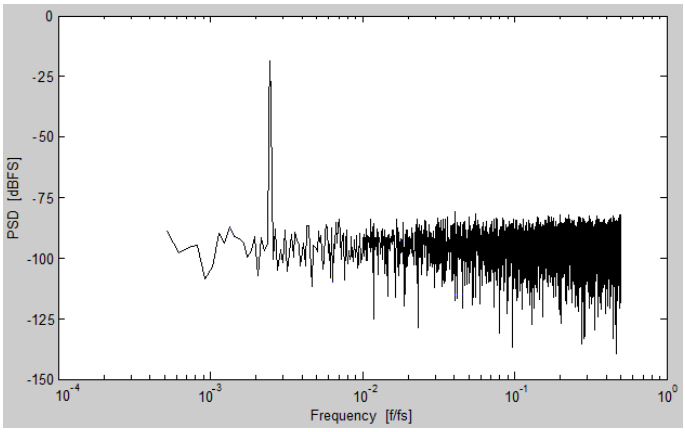

Fig. 8. An output spectrum of the standard third-order $\Sigma\Delta$ ADC excited by 1 kHz input signal.

The error cancellation logic combines the digital outputs from the two stages according to

$$Y(z) = H_1(z)Y_1(z) + H_2(z)Y_2(z) \tag{9}$$

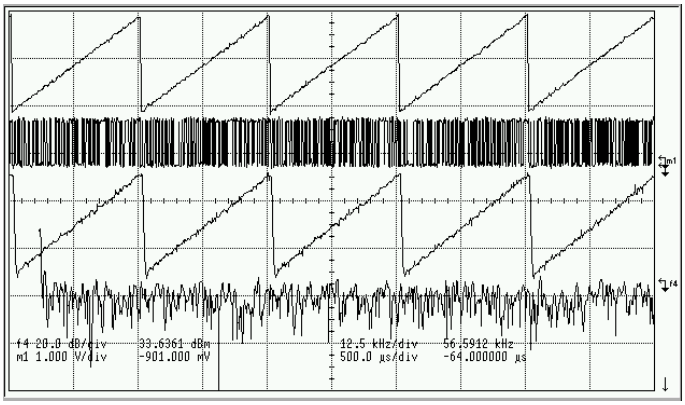

Fig. 7. Linear ramp input and output waveforms of the standard third-order $\Sigma\Delta$ ADC.

In order to cancel the quantization error of the first stage, the digital error cancellation logic is given by the following transfer functions in z plane:

$$H_1(z) = z^{-1} \tag{10}$$

$$H_2(z) = -(1 - z^{-1})^2 \tag{11}$$

The resulting output of the overall modulator is obtained by substituting (7), (8), (10) and (11) into (9) and can be expressed as follows:

$$Y(z) = z^{-2}U(z) + z^{-1}(1 - z^{-1})^2 E_D(z) - (1 - z^{-1})^3 E_2(z) \tag{12}$$

This is an equivalent of transfer function a standard third-order sigma delta converter, however this structure is stable. The output is now multi-bit, instead of single-bit. Also the cancellation of quantization error requires precise matching of the individual stages. This is challenging for an analog-to-digital converter (ADC). The first stage achieves first-order quantization noise shaping, while the whole modulator

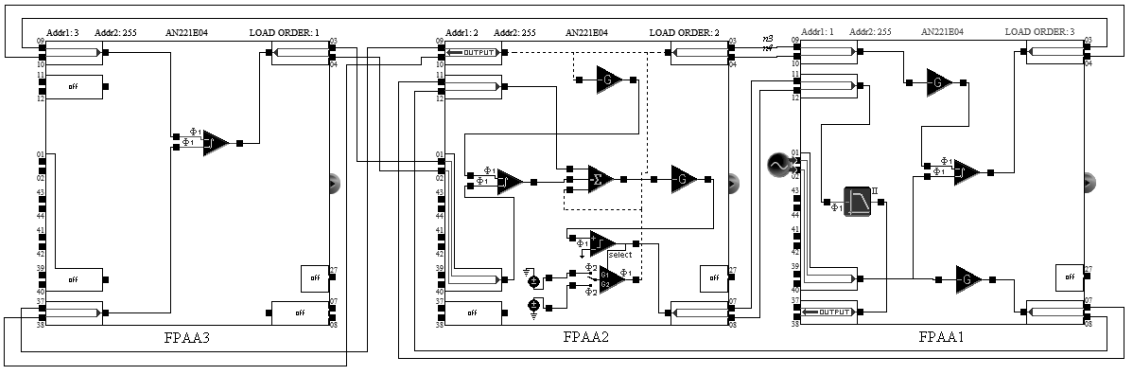

Fig. 9. Circuit realization of the third-order feed-forward ΣΔ ADC.

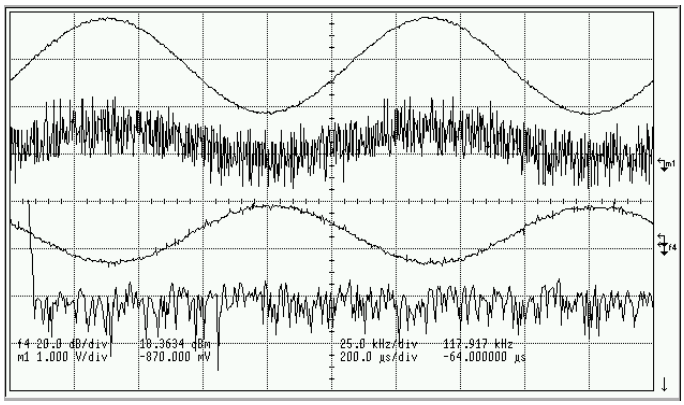

Fig. 10. Sinusoidal input and output waveforms of the third-order feed-forward ΣΔ ADC.

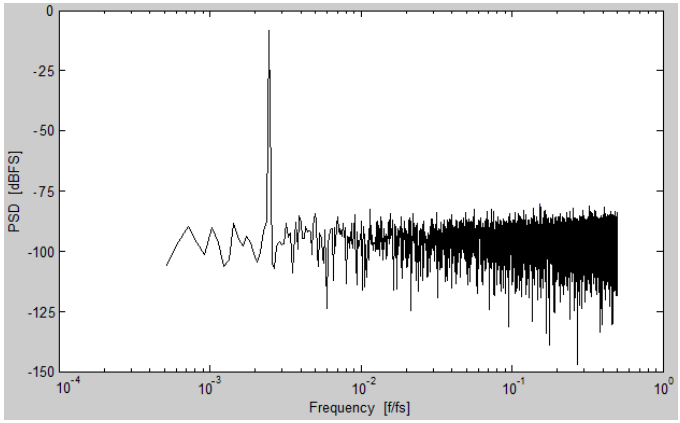

Fig. 12. An output spectrum of the third-order feed-forward ΣΔ ADC excited by 1 kHz input signal.

achieves the second order quantization noise shaping of the second stage noise. Provided exact cancellation of the noise from the first stage has been achieved.

III. ΣΔ ADCs Implementation

The standard third-order ΣΔ ADC has been designed and implemented using FPAA – Anadigm Development Board with three AN221E04 circuits. The prototypes were configured for the following specifications: sampling frequency $f_s = 4$MHz, bandwidth BW $= 20$kHz, input signal frequency $f_{in} = 1$kHz and oversampling ratio OSR $= 200$. The converter has been designed in AnadigmDesigner2 tool and next programmed at test board, as shown in Fig. 5. Third-order converter has been iteratively reconfigured from pre-calculated structure coefficients to achieve the best performance. Its measured output waveforms for a sinusoidal and for a linear ramp input voltages whose range is between ± 3V are shown in Figs. 6 and 7, respectively. The output signals have been achieved by lowpass biquadratic continuous time filtering. Finally a spectrum of the converter excited by the sinusoidal input with amplitude of 1 V pk-pk and a frequency of 1 kHz has been measured and shown in Fig. 8. The measured SNDR (using MATLAB) for a signal bandwidth of 20 kHz is 62.3 dB which is equivalent to 10-bit of resolution.

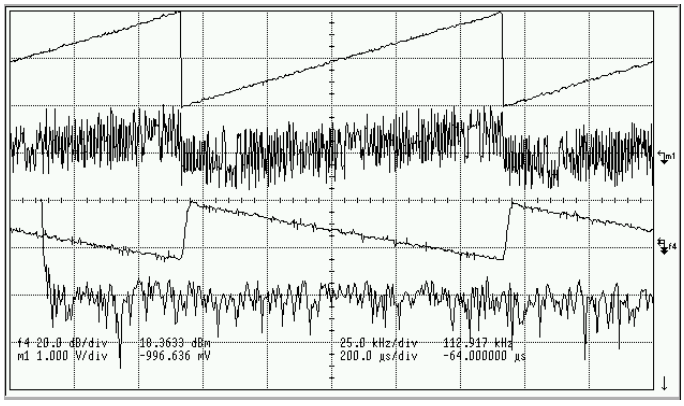

Fig. 11. Linear ramp input and output waveforms of the third-order feed-forward ΣΔ ADC.

As shown in Fig. 8, the fundamental problem with this architecture is the noise in the output waveforms. Fortunately, the programmable FPAA device enables to reconfigure improved converter architecture and to test it very quickly. To improve the noise shaping capability and improve stability in the architecture of the standard third-order ΣΔ ADC shown in Fig. 5, the third-order feed-forward path has been included and then the proposed third-order ΣΔ ADC has been implemented in the FPAA programmable structure. The third-order feed-forward structure is shown in Fig. 9.

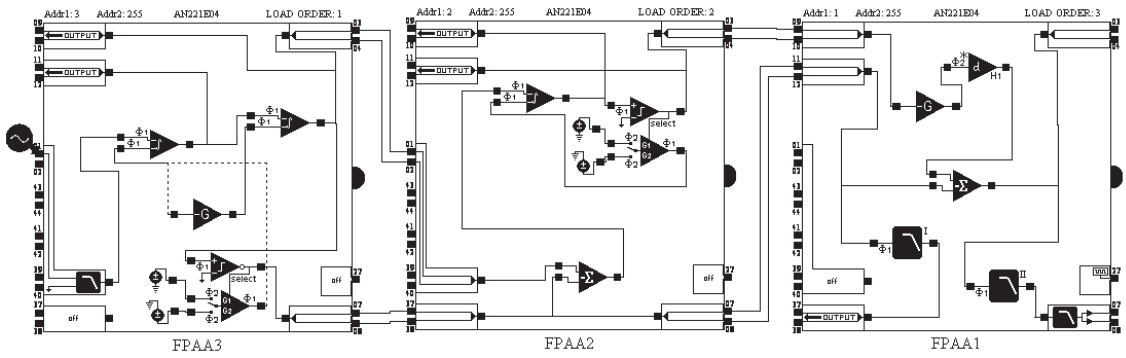

Fig. 13. Circuit realization of the 12-bit third-order multistage ΣΔ ADC.

Measured output waveforms of the third-order feed-forward ΣΔ ADC for a sinusoidal and for a linear ramp input voltages whose range is between ±3V are shown in Figs. 10 and 11, respectively. The output signals have been achieved by lowpass biquadratic continuous time filtering.

The ΣΔ ADC achieves the third order quantization noise shaping. The proposed feed-forward third-order converter digital outputs are post-processed in MATLAB, and the achieved SNDR for a sinusoidal input with amplitude of 1 V pk-pk and a frequency of 1 kHz is equal to 71.8 dB or 12 bits in resolution.

A different way to improve the noise shaping capability is using a multi-stage architecture of a third-order ΣΔ ADC, which increase the stability associated with high-order modulators. Two-stages converter has been implemented in the FPAA programmable structure, as shown in Fig. 13. In this converter the noise-shaping performance is essentially that of third-order single-loop converter, but stability behavior is that of a second-order one. This architecture has a direct feed-forward path from the input of the sigma-delta modulator to the ADC input, which results in suppression of the input signal component in the loop-filter. Therefore, the quantization noise is shaped by the integrators, thereby improving the distortion performance.

The third-order multistage ΣΔ ADC has been designed and implemented in FPAA for the following specifications:

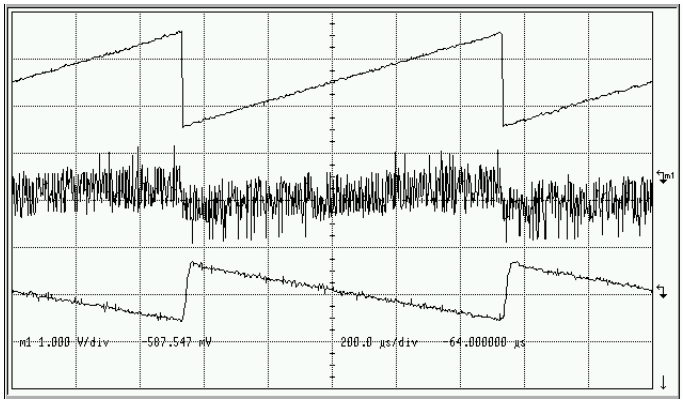

Fig. 15. Linear ramp input and output waveforms of the 12-bit third-order two-stage ΣΔ ADC.

sampling frequency $f_s = 4$MHz, bandwidth BW = 20kHz input signal frequency $f_{in} = 1$kHz and oversampling ratio OSR = 200. Its measured output waveforms for a sinusoidal and for a linear ramp input voltages whose range is between ±3V are shown in Figs. 14 and 15, respectively. The output signals have been achieved by lowpass biquadratic continuous time filtering. Finally a spectrum of the converter excited by the sinusoidal input with amplitude of 1 V pk-pk and a frequency of 1 kHz has been measured and shown in

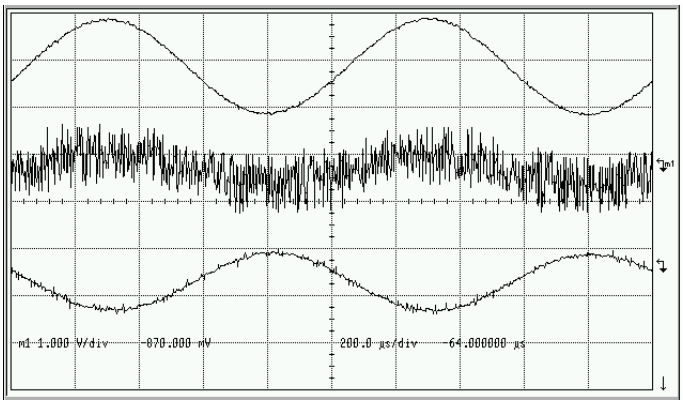

Fig. 14. Sinusoidal input and output waveforms of the 12-bit third-order two-stage ΣΔ ADC.

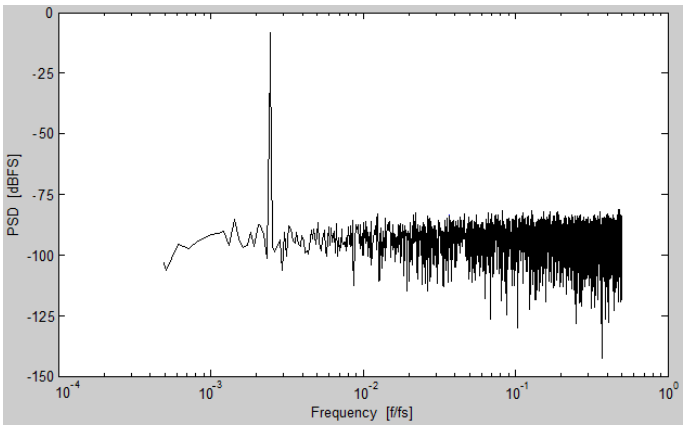

Fig. 16. An output spectrum of the third-order feed-forward ΣΔ ADC.

TABLE I
SUMMARY OF MEASURED PERFORMANCES

Converter architecture	Standard third-order	Feed-forward third-order	Multistage third-order
Oversampling ratio	200	200	200
Sampling frequency	4 MHz	4 MHz	4 MHz
Bandwidth	20 kHz	20 kHz	20 kHz
SFDR	68.4 dB	76.2 dB	75.8 dB
SNDR	62.3 dB	71.8 dB	70.4 dB
Resolution	10 bits	12 bits	11 bits

Fig. 16. The measured SNDR (using MATLAB) for a signal bandwidth of 20 kHz is 70.4 dB which is equivalent to 11-bit of resolution.

The summary of measured performances and comparison of noise shaping capability of the proposed standard third-order, third-order feed-forward and third-order multistage $\Sigma\Delta$ converters is presented in Table I. Figures 8, 12 and 16 show a FFT spectrum of a 1 kHz signal at a 4 MHz sampling frequency and a 20 kHz bandwidth with an OSR of 200. Spurious-Free Dynamic Range (SFDR) and Signal-to-Noise and Distortion Ratio (SNDR) have been computed and compared. Measured results showed that the third-order feed-forward converter has the best performances. the third-order multistage converter has 1.4 dB worse SNDR, but this architecture is less sensitive to the choice of structural parameters and improves the stability of high-order modulators.

IV. CONCLUDING REMARKS

Prototyping of higher order sigma-delta analog to digital converters has been presented in the paper. The method is based on implementation of FPAA AN221E04 to configure and reconfigure proposed circuits. A third-order $\Sigma\Delta$ ADCs has been considered. In first step the prototyped third-order converter was expanded to a third-order feed-forward architecture which improves the noise shaping capabilities. Next a multistage architecture was use to improve the stability associated with high-order modulators. Different prototyped structures are shown in Figs. 5, 9 and 13, respectively.

The circuit characteristics have been measured and then structure of the converters have been reconfigured to satisfy input specifications. The power signal density for converters have been computed using MATLAB. The standard third-order converter achieved SNDR 62.3 dB (10 bits), third-order feed-forward achieved SNDR 71.8 dB (12 bits) and third-order multistage achieved SNDR 70.4 dB (11 bits). Measured performances of the reconfigured converters confirm that FPAA reprogrammable devices such as AN221E04 may be useful for rapid and cost effective prototyping of mixed signal systems.

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