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Fast Low Voltage Analog Four-Quadrant Multipliers Based on CMOS Inverters

Witold Machowski, Stanisław Kuta, Jacek Jasielski, and Wojciech Kołodziejski

***Abstract*—The paper presents quarter-square analog four-quadrant multipliers, based on proprietary architecture using four CMOS inverters. The most important upgrade on already published own circuit implementation is the use of the same inverter "core" of the circuit with completely redesigned auxiliary and steering blocks. Two variants of new driving peripherals are considered: one with differential pair, the second with CMOS inverters. The proposed circuit solutions are suitable for RF applications in communication systems due to simple architecture comprising building blocks with RF CMOS transistors having sufficiently large biasing currents. Postlayout simulation results done on the basis of 180nm CMOS UMC Foundry Design Kit are also presented.**

***Keywords*—Analog VLSI, four quadrant multiplier, CMOS circuits, low voltage circuits.**

I. INTRODUCTION

ANALOG MULTIPLIERS are versatile building blocks used for numerous communication signal processing applications. In contemporary VLSI chips, the analog CMOS multipliers are widely applied in Phase-Lock Loops, automatic variable gain amplifiers, mixers, modulators, demodulators and to many other non-linear operations - including division, square rooting, frequency conversion etc. In most of applications, the desired multipliers features are good isolation between input/output ports (especially for RF systems), wide input dynamic range, wide bandwith, symmetric input/output delay, low power dissipation and low voltage suitability.

There are many diverse styles of designing CMOS multiplier circuits [1]. Most frequently, the variable transconductance technique operating on Gilbert's translinear circuit is used [2], [3]. The other efficient approaches in CMOS technology are based on quarter-square technique, using square-law transfer characteristics of the MOS transistors which are biased in saturation region [4], [5], [6], [7]. Many well known multiplier structures are not applicable in contemporary deep submicron highly scaled low-voltage process technologies, where gate voltage must be significantly reduced to prevent thin gate oxide breakdown.

Several authors have tackled a problem of designing low voltage CMOS RF multiplier architectures that allows satisfactory operation at frequency higher than 1 GHz [8], [5], [9], [10]. Generally speaking, any low-voltage CMOS multiplier circuit requires stacking of small number of MOSFETs in saturation region.

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W. Machowski, S. Kuta, and J. Jasielski are with the Department of Electonics, AGH University of Technology, Mickiewicza 30, 30-059 Kraków, Poland (e-mail: [machowsk, kuta, jasielsk]@agh.edu.pl).

W. Kołodziejski is with Department of Electronics and Telecommunications, State Higher Vocational School in Tarnów, Mickiewicza 8, 33-100 Tarnów, Poland (e-mail: compus2001@hotmail.com).

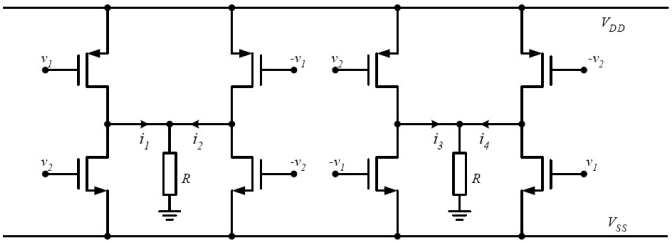

Fig. 1. Core of CMOS 4Q multiplier based on four inverters.

In the last decade the CMOS inverter is an object of increasing interest of analog designers [11], [12]. The quarter-square four-quadrant (4Q for short) multiplier based exclusively on CMOS invertes [13], [14] has an outstanding feature: – it is extremely suitable for low voltage operation and is fully compatible with digital CMOS. The supplying voltage for this circuit is the *limes inferior* for arbitrary mixed signal CMOS technology, since between the supply rails there is a stack of two transistors only.

The general concept of the multiplier exploits the quarter square technique (known and considered as "classic" already in 60s [6]) based on the identity from elementary algebra:

$$v_{OUT} = \frac{1}{4}\left((v_X + v_Y)^2 - (v_X - v_Y)^2)\right) = v_X \cdot v_Y \quad (1)$$

As it is obvious from (1), the technique in question requires the sum and the difference of factors as an auxiliary signals, which then undergo squaring. For symmetric drive, on the other hand, both sum as well as difference is required in raw and inverted form. In [14] we proposed the implementations performing both operations in current mode, while conversion of the input voltage into the current signal was done by balanced multiple output transconductor, similar to that, proposed by Nauta [15]. Our previous circuit comprise a lot of auxiliary current mode complex circuitry (70 MOSFETs alltogether) and therefore is not well suited for RF applications in communication systems. The chip presented in [13] was fabricated in AMIS (currently ON Semi) 0.35μm technology and has the cut-off frequency of single MHz only. In this paper we present a similar quarter-square analog 4Q multipliers, having significantly better HF performance thanks to completely redesigned auxiliary blocks. High-speed operation is possible due to simple building blocks using RF CMOS transistors with sufficiently large biasing currents. On the other

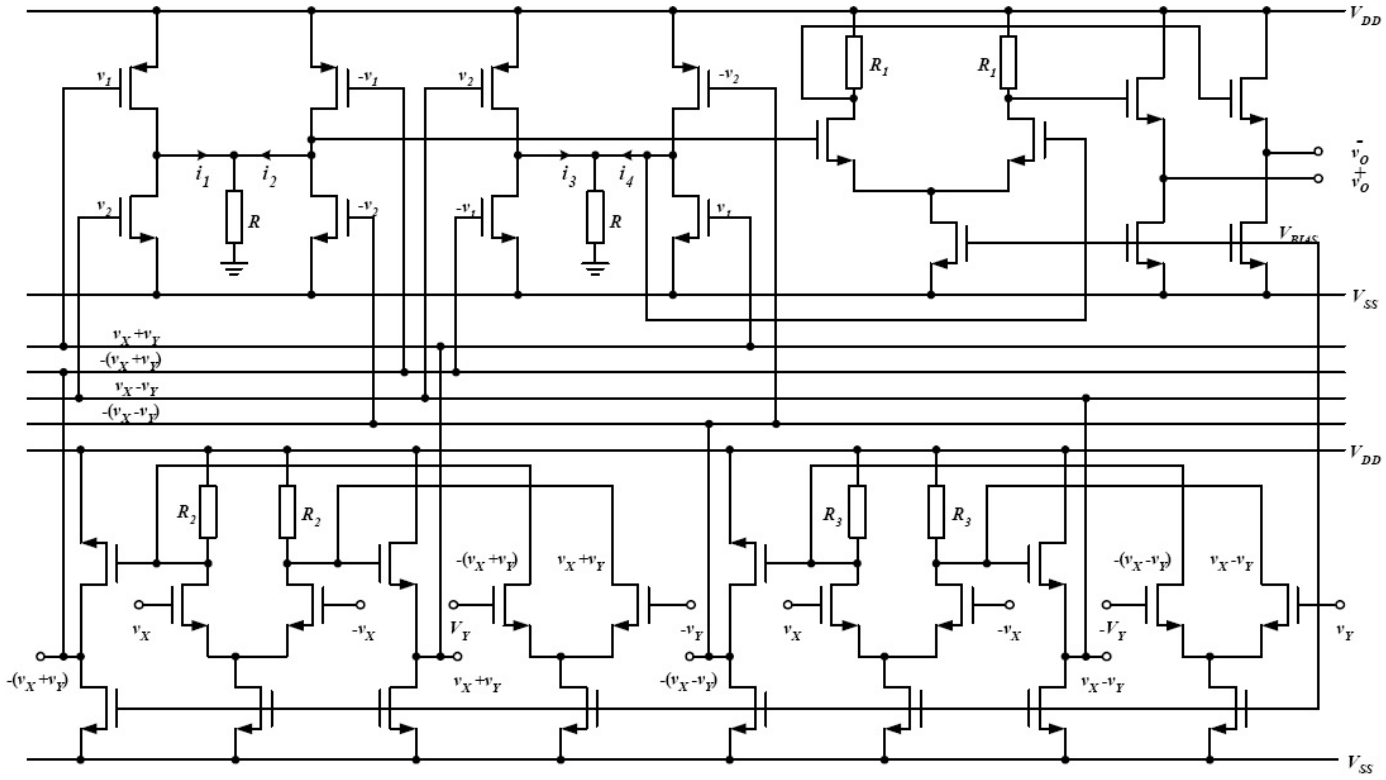

Fig. 2. Schematic diagram of entire multiplier variant with long tail pairs driving (inverting input amplifiers are omitted for picture clarity).

hand the circuit is redesigned with another techfile - 180nm from UMC, so positive simulation resuls prove the suitability of proposed general architecture for any conventional CMOS technology.

II. Principle of Operation

The core of multiplier is the double pair of appropriately driven CMOS inverters (Fig. 1). Let v_1 and v_2 will be the sum and difference of factor voltages, respectively: $v_1 = v_X + v_Y$, $v_2 = v_X - v_Y$. Assuming addionaly that all MOSFETs work in saturation region, which means

$$\begin{aligned} |v_1|; |v_2| &\le V_{DD} - V_C + V_{Tp} \\ |v_1|; |v_2| &\le |V_{SS}| - V_C - V_{Tn} \end{aligned} \tag{2}$$

and writing simple square-law equations for MOSFET currents we have

$$\begin{aligned} i_1 + i_2 \;=\; & \\ \frac{\beta_p}{2}\left(V_{DD} - V_C - v_1 + V_{Tp}\right)^2 \;+\; & \\ \frac{\beta_p}{2}\left(V_{DD} - V_C + v_1 + V_{Tp}\right)^2 \;-\; & \\ \frac{\beta_p}{2}\left(V_C + v_2 - V_{SS} + V_{Tn}\right)^2 \;-\; & \\ \frac{\beta_p}{2}\left(V_C - v_2 - V_{SS} + V_{Tn}\right)^2 & \end{aligned} \tag{3}$$

and similarly

$$\begin{aligned} i_3 + i_4 \;=\; & \\ \frac{\beta_p}{2}\left(V_{DD} - V_C - v_2 + V_{Tp}\right)^2 \;+\; & \\ \frac{\beta_p}{2}\left(V_{DD} - V_C + v_2 + V_{Tp}\right)^2 \;-\; & \\ \frac{\beta_p}{2}\left(V_C + v_1 - V_{SS} + V_{Tn}\right)^2 \;-\; & \\ \frac{\beta_p}{2}\left(V_C - v_1 - V_{SS} + V_{Tn}\right)^2 & \end{aligned} \tag{4}$$

V_C is the common mode reference voltage or artificial ground; to maximize input range of the circuit it should have value of:

$$V_C = \frac{\sqrt{\frac{\beta_p}{\beta_n}}\left(V_{DD} + V_{Tp}\right) - V_{SS} + V_{Tn}}{1 + \sqrt{\frac{\beta_p}{\beta_n}}} \tag{5}$$

For mathed transistors (which implies $\beta_p = \beta_n = \beta$ and $V_{Tn} = -V_{Tp} = V_T$) $V_C = (V_{DD} - V_{SS})/2$ and then the expression

$$\begin{aligned} & i_3 + i_4 - (i_1 + i_2) = \\ & (\beta_n + \beta_p) \cdot (v_1 - v_2) \cdot (v_1 + v_2) = (\beta_n + \beta_p) \cdot v_X \cdot v_Y \end{aligned} \tag{6}$$

is proportional to the product of input signals v_X and v_Y.

To have the functional multiplier on the chip, some additional operations of summing/subtracting input voltages/currents have to be done. Moreover we need this auxiliary signals in raw and inverted form. As we mentioned in the

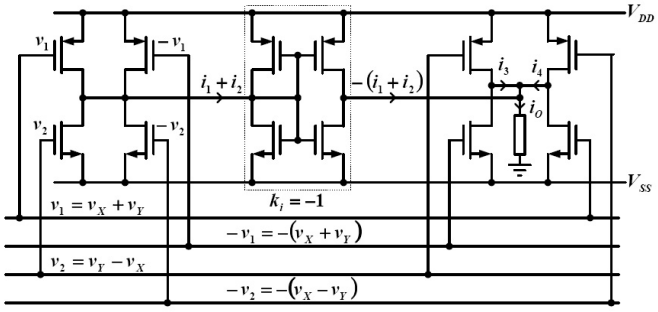

Fig. 3. Schematic diagram of multiplier variant with CMOS inverters.

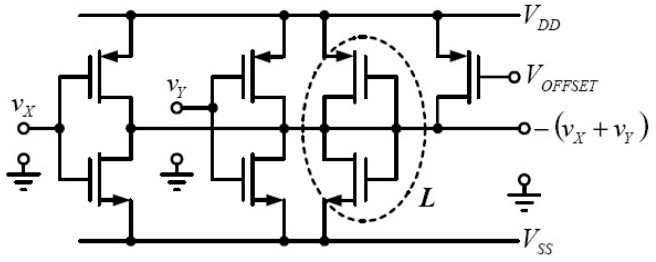

Fig. 4. The adder implementation with inverters only.

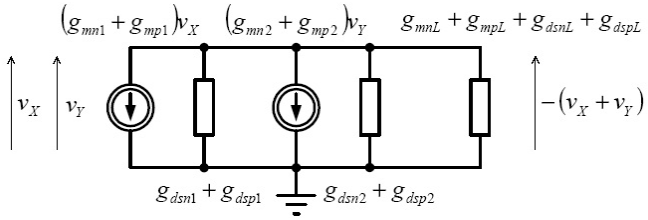

Fig. 5. Small-signal equivalent circuit of the adder.

previous section, the main drawback of previously proposed implementation was relatively poor HF performance, caused by auxiliary circuits rather than by the core from Fig. 1

III. New Driving and Auxiliary Circuitry

We designed and simulated two basic versions of auxiliary input/output circuits for the multiplier with the core described in the previous section. One circuit is based on differential pairs, while the second on CMOS inverters. Both utilize inverting voltage amplifier based on CMOS inverter and both have architecture of the whole multiplier significantly less complex than that of [13].

A. Variant with Differential Pairs [16]

In this variant both initial forming of $v_{1(2)}$ from v_X and v_Y as well as final subtraction of voltages across "left" and "right" resistor (Fig. 1) is performed in voltage mode using differential pairs. The schematic diagram is depicted in Fig. 2.

When two symmetrical differential pairs share the same drain resistances, and one of the differential pair is driven by v_X signal, while the second one by v_Y, then we receive two output signals, both are proportional to the input sum $v_X + v_Y$ and one signal is inverted, while the second one is not. To assure good linearity, the bias current of the applied RF MOSFETs has to be sufficiently large to guarantee almost constant value of the transistors transconductane. The source follower on each differential pairs output shifts the output voltage level to the ground one. Similar building block with sharing the load differential pairs gives inverted and non-inverted signals, which are proportional to difference of $v_X - v_Y$ input signals.

The only blocks missing in Fig. 2 are inverting voltage amplifiers used for driving the negative inputs of auxiliary differential pairs for generating v_1 and v_2 voltages. Because we consider the solution of 4Q multiplier architecture suitable for HF operation, it is better to use symmetrical driving of differential pairs. For this purpose, the additional inverting voltage amplifiers for v_X and v_Y signals, in the form of simple CMOS inverter with complementary diode connected transistors load, was used. This auxiliary circuit has been described in more detail in the next subsection, since it is strictly related with another auxiliary circuit implementation done entirely with the use of CMOS inverters.

B. Variant with CMOS Inverters [17]

This variant's most important part is presented in Fig. 3. The main difference with repect to the aforementioned implementation is the use of current mode for the output value, so there is only one output resistance for final current-to-voltage conversion. Auxiliary input sums and differences are obtained using the circuit depicted in Fig. 4. It consists of two linear amplifiers based on CMOS inverters working in parallel and having the active load of complementary diode connected transistors (embraced in oval labeled L in Fig. 4). Fig. 5 shows the small-signal, low-frequency equivalent circuit diagram of the above-mentioned circuit. Analysing this equivalent circuit under assumption of properly matched transistors we find:

$$v_O = -\frac{(g_{mn}+g_{mp})v_X + (g_{mn}+g_{mp})v_Y}{(g_{mnL}+g_{mpL})+(g_{dsnL}+g_{dspL})+2(g_{dsn}+g_{dsp})} \simeq -(v_X+v_Y) \quad (7)$$

where L index is used to point out parameters of the complementary diode-connected transistors working as a active load. The resulting output voltage is thus the opposite sign sum of $v_X + v_Y$. In similar way, but without second inverter we can obtain inverting voltage amplifier. An approproate combination of both mentioned blocks allows to realize four signals $\pm(v_X \pm v_Y)$ all necessary for desired functionality of the whole circuit. As it can be seen in Fig. 4, the block is equipped with additional p-channel transistor (exactly the same is used also in inverting voltage amplifier). This device is used for fine output offset compensation, because in the circuit from Fig. 4 the transistors' sizing for smooth (in the terms of output voltage characteristics) trasition between active operation of "upper" p-channel transistor and n-channel "bottom" transistor does not correspond with in-the-middle position of such transition. In other words the device in

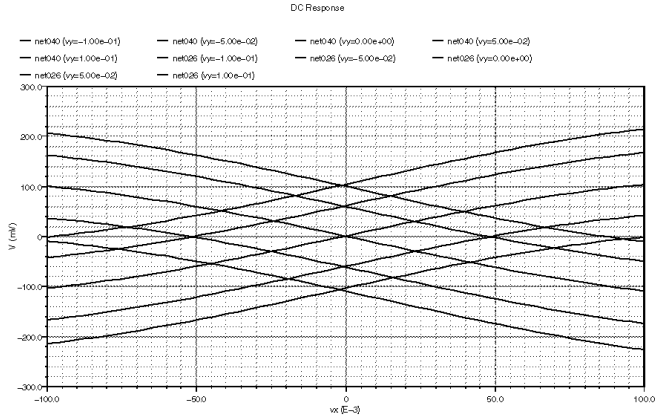

Fig. 6. Simulation results for auxiliary adder circuit based on differential pairs.

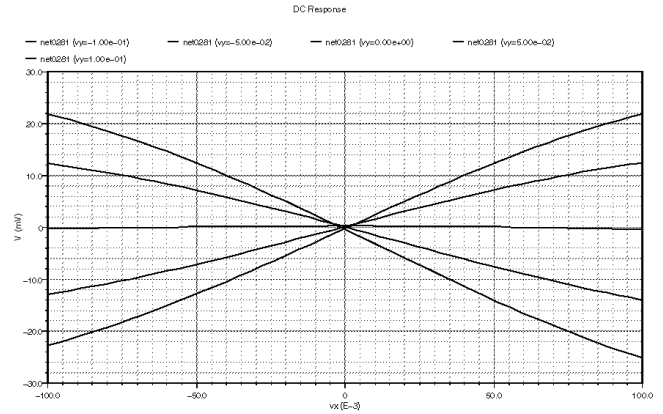

Fig. 7. Simulation results of the entire multiplier with differentail pair based driving circuitry.

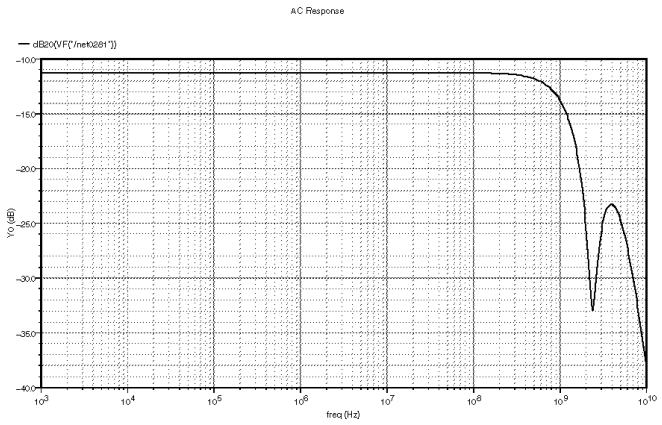

Fig. 8. Frequency response (magnitude) of the first circuit variant.

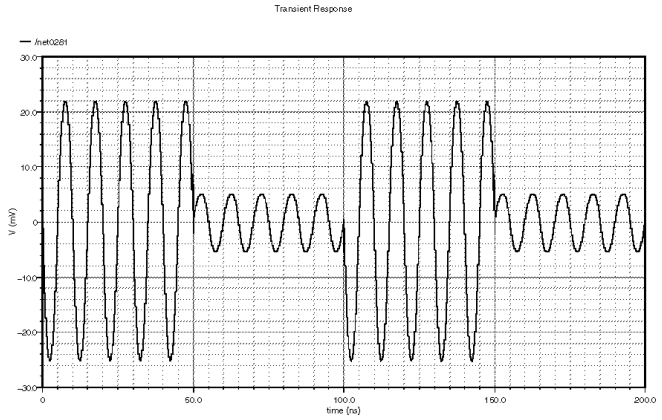

Fig. 9. Time domain simulation results for the first circuit variant.

question is necesssary to obtain both linearity as well as wider signal range.

IV. Simulation Results

All the described building blocks have been carefully sized and laid out using data avaliable in UMC 180nm Foundry Design Kit for Cadence environment. The layout of entire multiplier variant with diff-pair auxiliary circuits fits into $200\mu m \times 300\mu m$ rectangle, while the other variant is more compact and occupies approximately 65 $\mu m \times 65\mu m$ square only. All the presented simulation results are on the basis of postlayout extracted netlists without I/O cells.

The auxiliary inverting voltage amplifier utilized in both variants of entire multiplier implementation has excellent performance - its 3dB cut-off exceeds 3GHz with THD less than 0.5% for 100MHz and 200 mV_{p-p} signal.

A. Results for Differential Pair Variant

In Fig. 6 we show the DC simulation results for sum forming auxiliary circuit based on differential pairs. One input voltage was swept from 100 mV to 100 mV, while the second one was stepped from 100 mV to 100 mV by 50 mV. The results prove, that these blocks are operable in the range of about $\pm$100mV of input signal.

In Fig. 7 we present the results of simulation of DC transfer characteristics of whole multiplier. One input voltage is swept from 150 mV to 150 mV, while the second one is stepped from 100mV to 100 mV by 50 mV. Because there is not architectural symmetry in the circuit, it makes no sense to present complementary characteristics for otherwise arranged inputs.

Subsequent illustration (Fig. 8) shows the simulated results of multipliers frequency response. The magnitude reponse is flat up to over 500MHz, while 3dB cutoff frequency is close to 1GHz. Finally in Fig. 9 results of transient simulation (one input is driven by 100MHz carrier sinewave, while the second one by 10MHz square pulse) are shown.

Analyzing the results we find, that proposed circuit seems to be operable at high frequency (up to 1GHz), however the linearity is rather poor (calculated THD was about 4-5% for 100mV magnitude at 100MHz). The simulated power consumption was about 27mWatt, which is relatively big value. Moreover corner model simulations indicated that circuit is rather sensitive for process variation (unfortunately FDK does not provide the user with full Monte Carlo data for this technology node, so it was not possible to estimate the influence

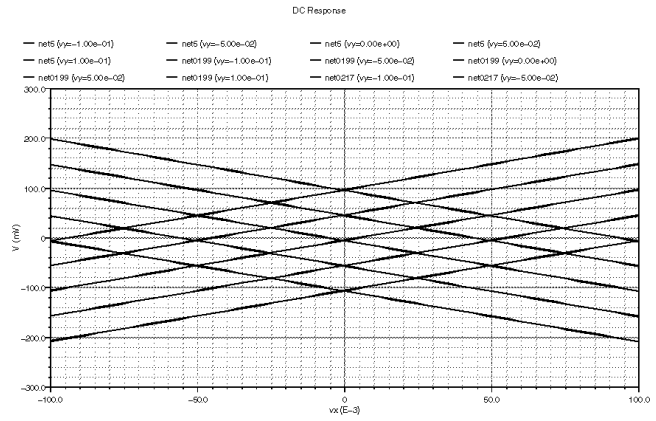

Fig. 10. Simulation results of CMOS inverter adder variant.

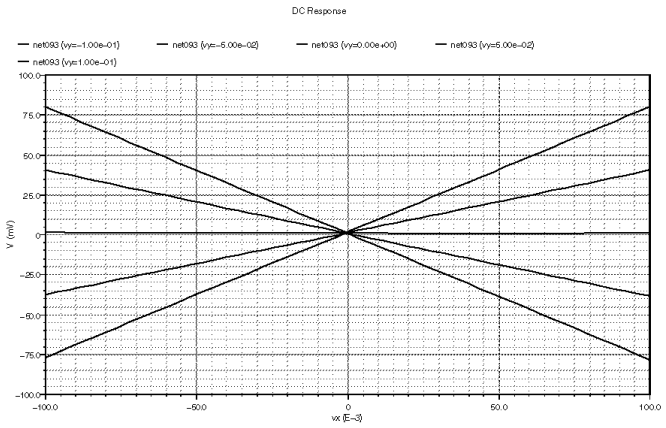

Fig. 11. DC simulation results for entire second variant multiplier.

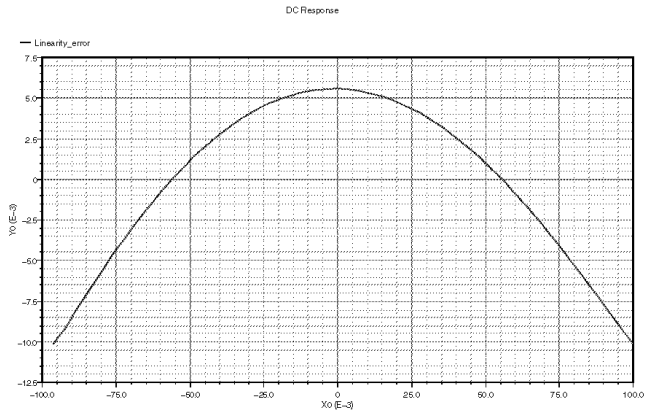

Fig. 12. Simulated DC linearity error versus input voltage for the second variant of multiplier.

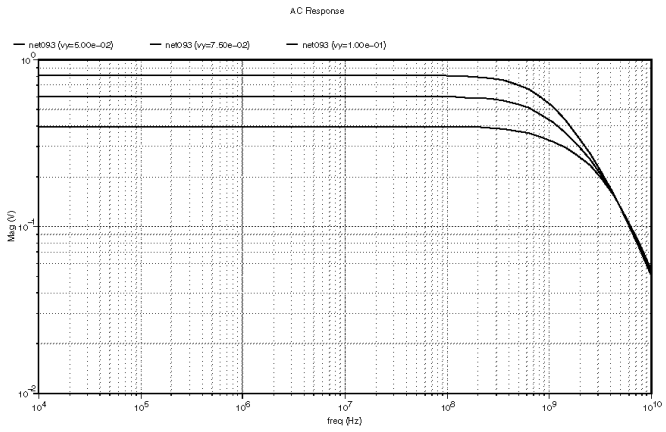

Fig. 13. Time domain simulation results for the second circuit variant.

of local process variations or element mismatch)

B. Results for Sole CMOS Inverter Variant

In Fig. 10 the results of DC simulation of auxiliary adder/subtractor for the second variant of the circuit are shown. It is visible at a glance that the results are significantly better than that of Fig. 6. The same apply for the whole multiplier - Fig. 11. This variant is fully operable within the input range of $\pm$ 100mV, and the deterioration from linearity (understand as the relative deviation of the curve's derivative with respect to the mean value of this derivative) within this input range does not exceed 1 percent (Fig. 12).

Much better linearity was not paid by significant reduction of circuit speed. Small signal frequency response simulation (Fig. 13) with one input stimulated by AC source, and the second one having constant yet stepped input voltage shows that this variant has only slightly worse HF properties. 3dB cut-off frequency does not reach 1GHz as before, but without any doubt is far beyond half of this value. Since small-signal simulations may be misleading, especially for strongly nonlinear circuits like multipliers, good HF performance of the second variant of multiplier was also confirmed by simulations in transient domain. In Fig. 14 simulated transient response of the multiplier driven by 1GHz sine and 20mV/ns ramp has been presented. Estimated power consumption of this circuit was 9.36 mWatt with 1.8 V supply.

Probbably the most important feature of this variant is noticeable (at least when compared with differential pair implementation) smaller sensitivity to process variations.

To close the presentation of simulation results, we just mention, that a third version of the multiplier was investigated, simulated and prepared for manufactuing by the silicon foundry. Somewhat another dimensioned second architecture multiplier suitable for 1.5 V supply has similar DC properties, but its estimated power consumption is 345 μWatt only. Obviously, this micropower version has significantly worse frequency response (3dB cut-off is about 8MHz), so it is not wery well suited for communication circuits, but due to its relatively high precision may be implemented in many other applications not requring very fast operation - like e.g. hardware neural networks.

V. CONCLUSIONS

Two architectures of quarter-square analog four-quadrant multiplier, based on own earlier implementation based on CMOS inverters[14] have been proposed. The work focused on re-use of the four CMOS inverter core and development of

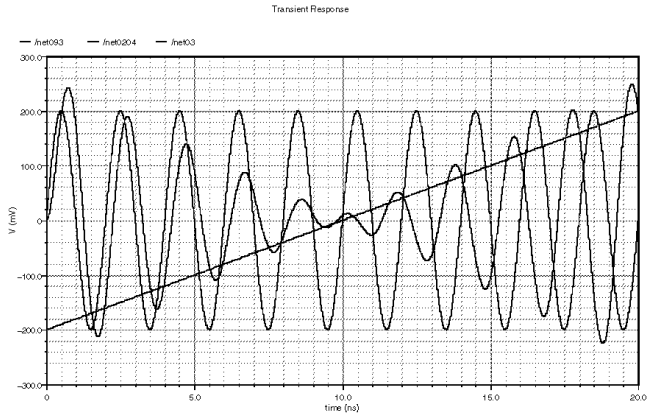

Fig. 14. Time domain simulation results for second circuit variant

TABLE I
SIMULATED FIGURES OF MERIT FOR MULTIPLIERS UNDER STUDY

Parameter	Circuit 1	Circuit 2	Circuit 3
Supply Voltage [V]	1.8	1.8	1.5
Power consumption [W]	27m	9.4m	350μ
Input range [mV]	$\pm$ 100	$\pm$ 100	$\pm$ 100
THD@100mV/100MHz [%]	4.8	0.24	0.55
Cut-off frequency [Hz]	$\simeq$ 1G	$>$ 500M	8M
Silicon area [μm$\times\mu$m]	200$\times$300	60$\times$60	60$\times$60

improved auxiliary circuits, more suitable for HF operation. We investigated in more detail two such solutions. One with differential pairs and using pure voltage mode, the second one with CMOS inverters only and exploiting internally current mode. The second circuit comprise stacks of at most two MOSFETs, so it is another variant of four quadrant analog multiplier based exclusively on CMOS inverters.

The first variant of the multiplier is definitely the fastest one, but unfortunately has rather poor linearity. The voltage budged did not allow to introduce any linearization techniques for differential pair. The circuit may be although used as a coincidence detector, or other applications requiring high speed without very precise operation.

The "inverter only" solution has much better overall performance - very good linearity, high speed and moderate power consumption.

The most important benchmarks of investigated circuits are summarized in Table I. The input range may seem to be not very impressive, especially in the terms of absolute values, but is comparable with other proposals made for similar technology node, supply voltage and frequency range.

All the described have been laid out and merged into single test chip recently sent for fabrication via EUROPRACTICE MPW prototyping service.

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