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Computer-Aided Multi-Layer Design of Switch-Mode Power Circuits

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***Abstract*—Switch-mode circuits are used as power processors, e.g. DC/DC converters, synchronous rectifiers, high-frequency resonant power amplifiers. Their efficient computer-aided design is a technical problem only partly resolved so far. This paper presents a multi-layer CAD methodology for switch-mode power circuits. It discusses several levels of modeling of switching devices. First rough design verification is feasible using ideal switch models. It gives a satisfactory first-cut design. Then full models and general-purpose tools provide more exact verification of the design. At this exact step the design procedure makes use of interactive improvement followed by automatic optimization of some quality based objective functions. The proposed methodology is shown to be especially useful for high power class-D voltage-switching resonant amplifiers, where the so far used experimental optimization is extremely cost consuming.**

***Keywords*—Switch-mode circuits, power electronics, class D resonant amplifier, interactive design, computer-aided design.**

I. Introduction

SWITCH-MODE CIRCUITS are of growing interest in power electronics and communications. They are used in power supplies of electronic devices, in radio transmitters as h.f. amplifiers and power modulators, and in industrial electronics (induction and dielectric heating). In these applications switch-mode circuits serve as power stages in high-efficiency power converters, operating at frequencies ranging from a few kHz to even a few GHz. Pertinent questions in the simulation and design of these circuits are how to find periodic steady state response, calculate losses in active and passive components, and maximize energy processing efficiency. It is also important to analyze transient responses in order to detect over-voltages and over-currents in such cases as: turning on and off the supply voltage, driving signals, load resistance and stepping operating frequency.

Power converters are often modeled by circuits with topology controlled by switches. In the simplest case switching transistors are modeled by ideal switches which leads to zero transistor power losses. This simple model is adequate for the first-cut design of converters in which transistor power losses can be neglected. If losses are of importance then the model with ideal switches must be upgraded with series resistances, parallel capacitances or even nonlinear, full physical models of the transistor have to be used.

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A. State of the Art

Existing design methods for switch-mode power circuits are not general; they are based on design equations [14], [20], [26], [54], [55], [61], [70] and are applicable only to specific types of circuits. Sometimes we observe exceedingly large discrepancy between simulation of the schematic and measurements of a breadboard circuit [64]. Power circuits convert high volume of power and parasitic couplings resulting from the physical layout may change their operation. Therefore**,** testing prototypes requires not only a genuine knowledge, but also deep designer's experience.

Experienced designers and teachers claim that the design process based on computer simulation is the most advantageous [3], [49]. Classical SPICE-like circuit simulators have one drawback in application to the switch-mode power circuits: they may spend up to 90% of the total simulation time on exactly tracing the response at switching instances. In early design stages such accuracy is not needed and less accurate idealized-switch-level simulation is satisfactory. Idealized-switch simulators allow for reduction of the computation time and volume of numerical results but require specialized numerical algorithms.

Idealized switch is a zero resistance/zero conductance and zero switching time element with the equation

$$s(p)\cdot v-\left[1-s(p)\right]\cdot r\cdot i=0\,, \tag{1}$$

where i, v are terminal signals, r - an arbitrary non-zero coefficient, and $s(p)$ describes the state of the switch (0 for OFF and 1 for ON) controlled by the function $p=p(\mathbf{v},\mathbf{i},t,s_{old})$ dependent on circuit responses $\mathbf{v}$, $\mathbf{i}$, time t, and the last state of the switch s_{old}. Ideal switches bring possibility of inconsistent initial conditions (IIC) at switching instances. KVL and/or KCL satisfied before the switching become violated due to a change in switch settings and circuit topology [43]**.** As a result currents through or voltages across ideal switches may contain Dirac impulses at switching instances. This causes the well known theoretical paradox of energy discontinuity: the values of energy stored in a capacitor or inductor before and after a switching instant E^-, E^+ may be different. In real switch-mode circuits the difference E^- - E^+ is dissipated in switched transistor during turn on (switching loss).

Simulation methods for circuits with ideal switches make use of dedicated algorithms based on circuit equations in such a form that discontinuities and IIC are overridden [4], [5], [6], [8], [10], [12], [15], [16], [19], [23], [27], [31], [32], [34], [37], [38], [40], [41], [46], [47], [52], [56], [57], [58], [59], [63], [65], [68], [71], [73]. Among these algorithms there are ones based on: average analysis based on behavioral models [6], accurate analyses: based on switching of network topology

and solution of substitute equations at switching instances [4], [5], [15], [40], [41], [57], [58], [59], [68], [71], [73], on formulation of dedicated forms of state equations [34], [56], [65], as well as based on piece-wise linear equations [46], [47]. Due to elimination of switching effects, these specializes algorithms are of higher numerical efficiency comparing to traditional methods, e.g. in SimPowerSystem-MATLAB toolbox [35]. The latter contains a package accepting ideal switches but uses ordinary numerical integration with all drawbacks of this approach, e.g. spending most of computer time on exact tracing responses at switching instances, numerical stability.

One of essential tasks in switch-mode circuit simulation is steady-state analysis. Switch-mode circuits are characterized by slow convergence to a steady-state. Therefore, algorithms must be extremely efficient since they are repeated a lot of times to reach convergence. A wide spectrum of steady-state analysis algorithms have been elaborated, so far, for these circuits [1], [2], [7], [9], [13], [17], [18], [22], [24], [28], [29], [30], [33], [39], [45], [57], [60], [62], [66]. One of very efficient approaches is the secant method [7], [39], implemented in SWITCH [40], [41] and OPTIMA [39].

All above discussed works are dedicated to different methods of efficient mathematical modeling of switch-mode circuits. Little research effort was engaged in developing CAD algorithms, where simulation was only a part of a more general design optimization problem as it is in this paper.

B. Scope of the Paper

This paper is dedicated to a methodology of CAD of switch-mode circuits which leads a designer from initial approximate design elaboration to its final optimization. Since improvement of design quality cannot be performed in one step, hence a multi-layer approach is proposed. On initial stages designs are evaluated by means of coarse circuit modeling, with a low numerical complexity. A final stage needs high complexity models but a design is already roughly tuned and needs only multi-objective quality optimization Our design procedure consists of four stages based on different models of switch-mode circuit elements.

- The first stage consists of rough engineer calculations based on idealized switches (Fig. 1a) and approximate relationships describing circuit operation. This quick method gives one or several initial solutions.
- On the second stage we apply idealized models with capacitances to initially accepted solutions (Fig. 1 b,c) and use a dedicated time-domain simulation [4], [5], [6], [8], [10], [12], [15], [16], [19], [23], [27], [31], [32], [34], [37], [38], [40], [41], [46], [47], [52], [56], [57], [58], [59], [65], [68], [63], [72], [73] (e.g. switching topology or piecewise-linear). In this work we use our own simulator SWITCH [40], [41] working in the MATLAB environment. Its advantage is availability of DC, transient, steady-state and Dirac impulse analyses (the latter to verify switching conditions). SWITCH offers also models shown in Fig. 1c that take into account switching and conduction losses.
- On the third stage accurate simulation is performed by means of SPICE-like simulators [42], [48], [50] with physical models of elements including non-idealities and parasites. This gives a more detailed information about the circuit behavior and enables its improvement.
- Finally, on the fourth stage, which is essential for this work, a designer gets a chance to perform multi-criteria optimization (similar to [44]) by means of SCAD software. First, plots of basic circuit performance measures (power efficiency, output power, etc.) versus selected design parameters are obtained. They enable to play interactively with a design to learn its properties and improve it. Then it is possible to perform automatic screening of design parameters – to determine most influential ones. If the exploration reveals the need for further design improvement then the final step of multi-objective optimization is performed. The fourth stage of design process has been prototyped in our experimental SCAD (Switch-mode Circuit Analysis and Design) software.

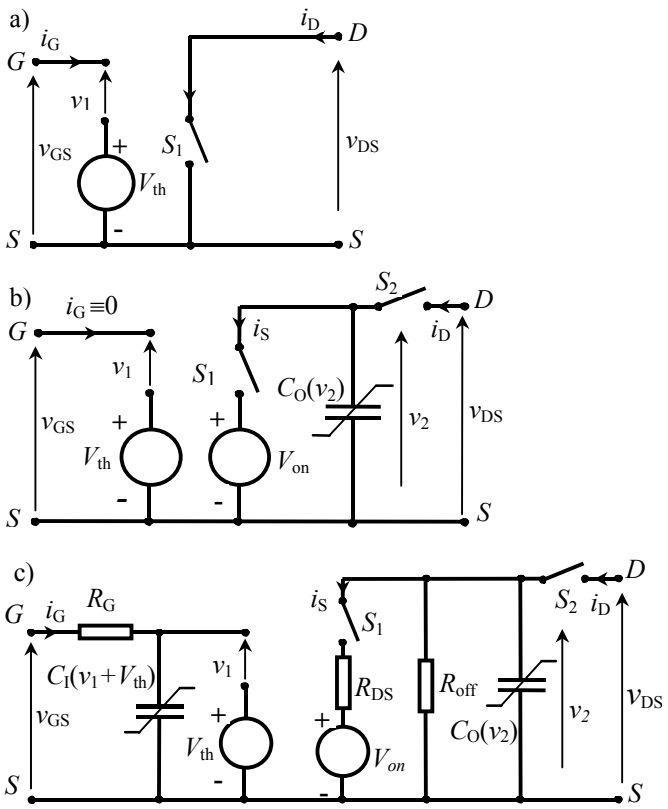

Fig. 1. Models of switching elements based on ideal switches: a) idealized model, b) idealized model with capacitance, c) simplified physical model.

The above listed four-stage design methodology is described in Chapter II. Chapter III contains a design example of class D resonant amplifier. Final conclusions are collected in Chapter IV.

II. Switch-mode Circuits Design

A. First Stage – Initial Engineering Design

At the first design stage we use simple engineering calculations which are possible thanks to the engineer experience and ingenuity accompanied with assumption of idealized switches

– as it is shown in Fig. 1a. Idealized switch S_1 is controlled by driving signal v_{GS} and output voltage v_{DS} (in MOSFETs due to the parasitic anti-parallel diode).

$$S_1(p_{11}, p_{12}) = \begin{cases} 1 & \text{if } p_{11} \geq 0 \cup p_{12} \geq 0 \\ 0 & \text{if } p_{11} < 0 \cap p_{12} < 0 \end{cases} \quad (2)$$

where $p_{11} = v_1 = v_{GS} - V_{th}$, $p_{12} = V_D - v_{DS}$, v_{GS}, v_{DS} are input and output voltages of the modeled element, V_{th} is the threshold voltage, V_D is the anti-parallel diode voltage ($V_D \approx 0.7$V) . Such a simplification causes that the conduction and switching losses in switching elements are zero. In real switch-mode circuits switching losses can be ignored only if the operating frequency is sufficiently low (even in hard-switched non-ZVS and non-ZCS PWM converters). Switching losses can be also neglected in high-frequency soft-switched (ZVS and ZCS) circuits (e. g. class E or DE amplifiers), but in this case output capacitances of power transistors should be absorbed by the resonant circuit. Thus, for soft-switched high-frequency circuits the simplest model of the switching element has to contain ideal switch of equation (2) shunted by the parallel capacitance C_O of the open switch (a model with capacitance shown in Fig. 1b). For power elements this capacitance is in reality non-linear [73]. Consideration of this capacitance will be performed at the second stage.

B. Second Stage – Simulation on Idealized Switch Level

The second stage is the computer evaluation stage where a design elaborated on the first stage by means of engineering intuition, knowledge, and rough calculations, based on the engineering formulae is verified and improved on the base of a fast turn-around simulation, which helps to detect impulses in the response caused by non-zero voltage switching on (non-ZVS) or by non-zero current switching off (non-ZCS) and calculate switching losses resulting from these impulses. Due to the spreads of the values of elements, impulses may appear at switching instances even in ZVS circuits (designed for zero capacitor voltages) and in ZCS circuits (designed for zero inductor currents) [34].

If the model of Fig.1b including capacitances is used in the analysis of non-ZVS circuits (e.g. resonant class D amplifiers or DC/DC PWM converters) then Dirac impulses occur in the current i_S through switch S_1. In non-ZVS converters energy stored in capacitance C_O just before turn-on $W_{Co}=0.5C_O(V_{DS}^-)^2$ is dissipated in the switching element causing switching losses. This energy can be also expressed in terms of the area Q_{SW} of the Dirac impulse in the current through switch S_1:

$$W_{diss} = \frac{1}{2} Q_{SW} V_{DS}^- \quad (3)$$

Non-linear input and output capacitances of power transistors are often described by a small-signal value as a function of input or output voltage. These functions are published by the transistor manufacturers or can be extracted from an exact, SPICE-like simulation, using a physical model of power-transistor [73]. It is also a common practice that in the simplified large signal analysis non-linear capacitance is replaced by an averaged linear capacitance.

When the averaged linear capacitance is extracted then we can proceed to rough computer verification based on idealized models with the on-voltage source V_{on} and the capacitance – as it is shown in Fig. 1b and verify initial designs with dedicated simulators: e.g. [40], [41] which can handle circuits on idealized switch level [4], [5], [6], [8], [10], [12], [15], [16], [19], [23], [27], [31], [32], [34], [37], [38], [40], [41], [43], [46], [47], [52], [57], [58], [60], [63], [65], [68], [71], [73], to considerably reduce time of its time-domain analysis comparing to traditional simulators exploiting full physical models of switches. During this analysis Dirac impulses of the time response are also calculated.

This quick simulation moreover allows for calculating also conduction power loss of a switching element: $p_{diss}(t)=V_{on}\, i_S(t)$. This yields an average conduction power loss estimate of a multi-switch circuit, $P_{Cdiss}= \Sigma V_{onk}\, I_{Dk}$, where I_{Dk} is the DC component of the output current of the k-th switching element. Other physical phenomena incorporated into idealized models are dissipation of power and self-destruction. In Fig. 1b switch S_2 models self-destruction by open-circuiting of the device when maximum GS voltage v_{br1} or DS voltage v_{br2}, or maximum junction temperature T_{jmax} are overridden. S_2 is controlled by the function

$$S_2(p_2) = \begin{cases} 1 & \text{if } p_2 \geq 0 \\ 0 & \text{if } p_2 < 0 \end{cases}, \quad (4)$$

$$\text{where } p_2 = \begin{cases} v_{br1} - |v_{GS}| & \text{for gate destruction} \\ v_{br2} - v_{DS} & \text{for drain junction destruction} \\ T_{jmax} - T_j & \text{for thermal destruction.} \end{cases}$$

Switch self-heating is modeled by the temperature dependent voltage sources $v_{th}(T_J)$ and $v_{on}(T_j)$. Transistor output capacitance C_O may be temperature independent, or dependence $C_O(v_2,T_j)$ is extracted from physical, SPICE-like, simulation. If power emission and diffusion are considered, a thermal RC-macromodel may be used [72].

On this stage also losses can be analyzed approximately, if linear loss-resistances are introduced – as it is shown in Fig. 1c. However this approach is insufficient, and a more accurate simulation based on physical nonlinear models is more advantageous. This physical approach is proposed on our third design stage.

Idealized models shown in Fig. 1 cannot describe active operation of switching elements. Hence, in non-ZVS circuits they neglect the Miller's effect and its impact (e.g. cross-conduction current in push-pull class-D amplifiers). In non-ZVS and non-ZCS (hard-switched) circuits, losses caused by finite time of turn-on and turn-off are also omitted.

C. Third Stage – Physical Simulation and Improvement

This is a design exploration stage, when physical elements are considered to check their influence upon basic circuit functionality. General purpose simulators with full models of elements are employed. A designer can quantitatively characterize circuit performance, e.g. power loss and efficiency in steady state, over-voltages and over-currents during transient responses. We exploited three general-purpose simulators: PSPICE [48], OPTIMA [42], and SPECTRE [50]. The advantage of SPECTRE and OPTIMA is availability of a quick steady state analysis. Manufacturers of electronic

elements furnish advanced models for general-purpose simulators: IGBT, bipolar and MOSFET transistors [21], [48], [51], inductors and transformers, with non-linear core, saturation and sometimes even hysteresis (though the latter often causes convergence problems). They usually give accurate though time-consuming results and are useful only if a design has been selected from many possibilities at first and second design stages.

Physical modeling of high-speed switch-mode power circuits should consider parasitic effects brought in by the printed board technology. Their models fall into two groups: introduction of auxiliary RLC transmission lines and incorporation of limits arising from electrical and thermal strength of a path. At moderate power levels and frequencies, influence of field effects is in practice negligible except for some resonant circuits [25], [69]. Modeling of the thermal strength of a printed board and self-destruction of elements can be performed using switches similar to those introduced in Fig. 1b.

D. Optimization-based Design Improvement

Optimization-based design is a semi-automatic process, composed of design exploration and optimization. At the exploration phase an ad-hoc composition of interactive simulation, techniques of experiment planning and numerical optimization are used to reveal the most influential design parameters, tune the circuit (to offset inaccuracy of the simple engineering formulae), learn trade-offs between competing performance measures. Design improvement is stopped if a satisfactory performance has been reached. Otherwise, the best design point and information on the design trade-offs from the exploration phase are used to formulate and solve an optimization problem. In our approach design exploration results are presented as curves of system performance functions versus selected parameters, and as Pareto curves of optimal trade-off between two most important performance measures.

This stage requires integration of different tools, including commercial and experimental problem-specific software. We created an experimental environment SCAD, tailoring the ideas developed earlier in the Generic System for Statistical Improvement of Performance – GOSSIP [44]. SCAD can perform stochastic or deterministic exploration of the design space (see also example in sec. 3.3).

In the course of calculations an engineer may check validity of the models used, find the most influential design parameters **x** and determine basic design tradeoffs. For the optimization-based design it is crucial to formulate design figures of merits $\mathbf{f}=[f_1, f_2,...,]^T$. Typically, each objective f_i is a result of some numerical processing of raw time responses. Simple examples are: minimum, maximum or peak-to-peak values of a response; more complex are power related (e.g. efficiency) or harmonic distortion measures. Then for each f_i the designer specifies the target values or a set of bounds that determine feasibility of a particular design parameter set. Altogether we obtain a multiple-objective optimization problem that can be solved with a specialized optimizer or with a least-squares, generalized least p-th function [44] or mini-max optimizer. If the goal is to find the set of design parameters **x** and for each function f_i (**x**) it is possible to formulate two levels: u_i - the largest acceptable value, and l_i - the desirable value, then the scalar quality factor can have the form:

$$F(x) = \max_i \frac{f_i(\mathrm{x}) - l_i}{u_i - l_i}. \quad (5)$$

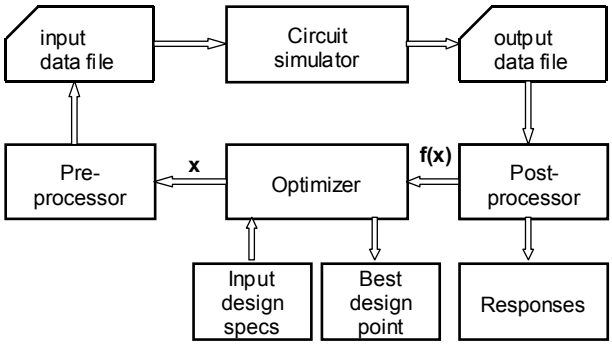

Fig. 2. Computational structure of SCAD software.

In optimization-based design the design parameters do not necessarily coincide with a set of parameters of circuit model, because some design parameters may influence values of several circuit parameters (e.g. some parameters track each other). Furthermore, changing the circuit simulator (to move from an idealized switch model to a more realistic one) requires changes of computer representation of the input data. To make our MATLAB-based SCAD software flexible the computational structure shown in Fig. 2 was used, patterned after that of GOSSIP [42]. Pre-processor converts designable parameter vector to the input file of currently selected circuit simulator, while post-processor transforms the output file (or files) to a set of scalar figures of merit f_i. The post-processing is in fact done in two steps. First a data converter extracts from the raw output file tables of raw responses. Then MATLAB M-functions (developed by the user) extract figures of merit and produce the vector of figures of merit ***f***.

The SCAD environment supports the following modes of operation:

1. Evaluation of selected design performance measures and figures of merit for a range of values of one or two design parameters at a time. From visualization a designer can learn dependencies between performance measures (trade-off), and dependencies of these measures on design parameters. Even experienced designers can gain from such an analysis of design properties.
2. A generalized Latin square experiment [69] can be automatically set up to investigate dependence of performance measures on numerous design parameters. The goal is to eliminate large number of design parameters from further consideration, and leave the most influential ones. In fact after this experiment more detailed examination (as in p. 1) can be setup. Such a sequence of steps can be suggested for new circuit topologies, when engineering experience is insufficient to guarantee appropriate selection of most influential design parameters.
3. Multi-objective design optimization (generalized least-squares or mini-max) can be performed using MATLAB's Optimization Toolbox. Transformation of performance measures to figures of merit is done according to (5) [44].

The user weights importance of different performance measures by selection of two levels: u_i – the largest acceptable value, and l_i - the desirable value. Optimizer tries to decrease each f_i below u_i until l_i is reached. Control of trade-offs with l_i and u_i is thus performed using design specific satisfaction levels, not abstract weighting coefficients – as is typical in such a case.

Our MATLAB-based design environment SCAD blends well established and proven design automation ideas of multi-layer simulation, design of experiments and multi-criteria optimization. It should be underlined, that such an approach is novel in switch-mode power circuits practice.

III. Design Example

As an illustrative example we design the class-D voltage-switching resonant power amplifier. It explains the proposed multi-layer design methodology and shows the features and drawbacks of the developed or adapted software tools.

We assume that the amplifier should deliver an approximately sinusoidal 1MHz signal of power 100W (±10%) to the load resistance when DC supply voltage is 95V. The value of load resistance R_L=18Ω is assumed. Small harmonic distortions of the output voltage are acceptable (THD≤5%).

A. Properties of the Considered Amplifier

It is a push-pull circuit (Fig. 3); transistors T_1, T_2 operating in non-ZVS and ZCS mode are driven alternatively by a periodic input signal [11], [25]. The output circuit is a selective series-resonant circuit with the resonant frequency equal to the input-signal frequency. Because the load impedance transformation is not required we applied a simple series R_L C L circuit (Fig. 3). The output current and voltage across R_L are approximately sinusoidal if the loaded quality factor Q_L is sufficiently high (Q_L>*3*).

Efficiency of the class D voltage-switching amplifiers is limited by losses in coil L and capacitor C, as well as conduction and switching losses in transistors T_1, T_2. Switching losses result from charging and discharging output capacitances of T_1, T_2 [25], and can also be generated by cross-conduction current pulses in T_1, T_2 (if gate driving voltage waveforms v_{GS1}, v_{GS2} overlap [11], [25]) The overlapping gate voltages can be caused by the Miller's effect or by a high rate of rise of drain-source voltage (in the class D amplifiers with MOSFETs) [21], [25]. Switching losses resulting from cross-conduction current are high and can destroy power transistors. In a correctly designed class D resonant amplifier they have to be eliminated (assuring ZCS turn on and turn off of the transistors).

Harmonic distortions in the output voltage and current depend on the frequency response of the output R_L L C circuit. For a simple series resonant circuit frequency response is a function of the loaded quality factor $Q_L=\omega_O L/R_L$. Thus, in the analyzed amplifier (Fig. 3) the ratio of the n-th odd harmonic amplitude I_{on} of the output current (voltage) to the amplitude of the first harmonic I_{O1} is equal to

$$\frac{I_{On}}{I_{O1}}=\frac{U_{On}}{U_{O1}}=\frac{1}{\sqrt{n^2+Q_L{}^2\left(n^2-1\right)^2}}, \qquad (6)$$

where n=1, 3, 5, 7, ... (even harmonics cancel).

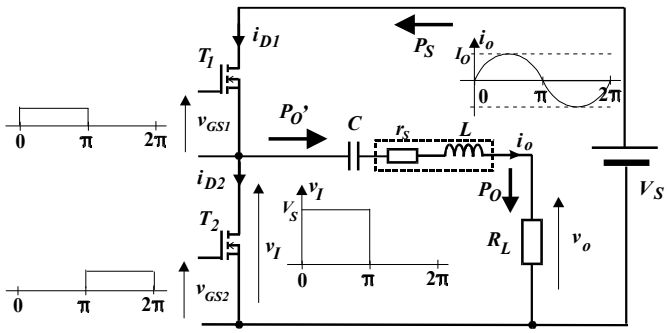

Fig. 3. Class-D resonant power amplifier – principle of operation.

B. First Stage – Initial Engineering Design

The first step of design of the class D amplifier is based on the idealized model of switching transistors (Fig. 1a, Fig. 4a) and a high value of Q_L is used. These simplifying assumptions allow for calculation, using a scientific calculator only, approximate values of R_L, L, C and amplitude I_O of the output current i_O for the required values of the output power P_O, supply voltage V_S, operating frequency f_O, and loaded quality factor Q_L. Assuming Q_L=5 we obtain:

$$R_L\approx\frac{\left(\frac{2}{\pi}V_S\right)^2}{2P_O}=18.288\Omega,\quad L=\frac{Q_L R_L}{2\pi f_O}=14.553\mu H$$

$$C=\frac{1}{4\pi^2 f_O{}^2 L}=1.7405nF,\ I_O\approx\frac{2V_S}{\pi R_L}=3.307A. \qquad (7)$$

In the amplifier we used L=14 μH coil with Q_O≅170 at 1MHz (series resistance r_S=0.52Ω), C=1.809nF, and load resistance R_L=18Ω. Efficiency of the resonant circuit is sufficiently high (η_O=97.1%). Total harmonic distortion of the output current and voltage can be numerically calculated using (6). For Q_L=5 we obtain THD≅2.7%.

Values of V_S, I_O help to choose type of the power transistor. The maximum drain-source voltage must satisfy the condition: $v_{DSmax} > V_S$, and maximum continuous drain current $I_{Dmax} > I_O/\pi$. For this, the following 100V low-cost switching power transistors can be considered: IRF510, IRF520, IRF530.

In the second step of design (Fig. 1b, Fig. 4b) we take into consideration conduction and switching losses in the amplifier operating without cross-conduction current. The following parameters are calculated:

a) Amplitude of the output current and output power

$$I_O=\frac{2V_S}{\pi\left(R_L+r_S+R_{on}\right)}, \qquad (8)$$

$$P_O=\frac{1}{2}R_L I_O{}^2. \qquad (9)$$

b) Power losses in L

$$P_L=\frac{1}{2}r_S I_O{}^2. \qquad (10)$$

c) Conduction and switching losses in transistors

$$P_{Ctot}=\frac{1}{2}R_{on}I_O{}^2. \qquad (11)$$

$$P_{SWtot}=2f_O C_O V_S{}^2. \qquad (12)$$

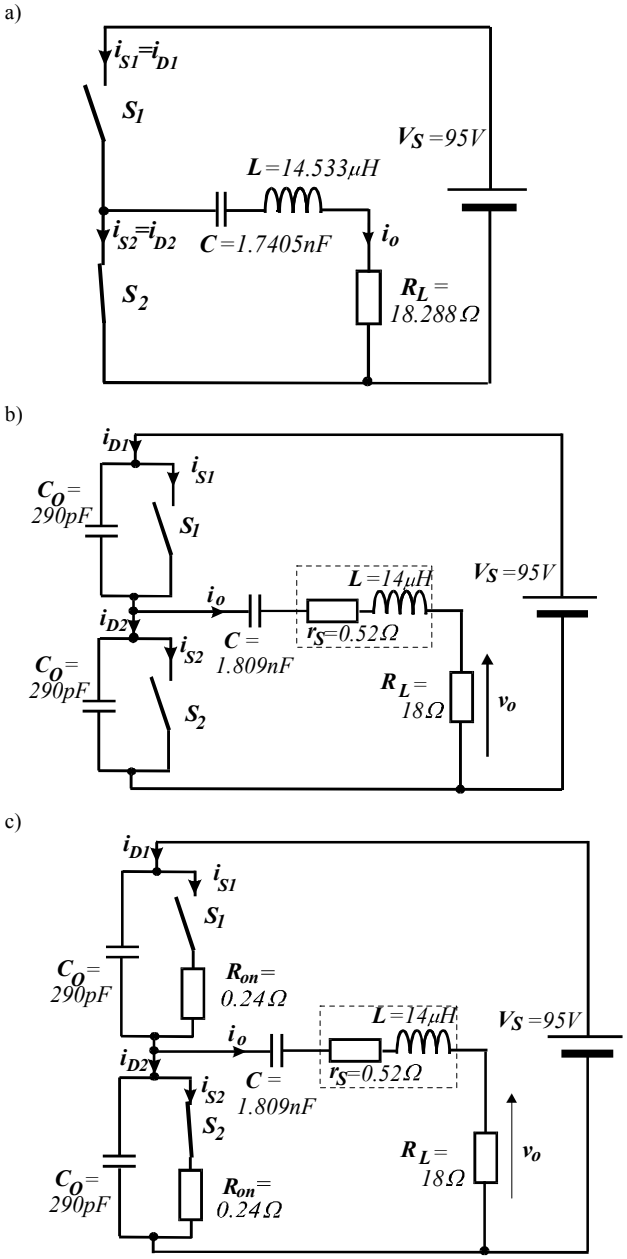

Fig. 4. Models of the 1MHz class-D resonant amplifier; a) loss-less model of transistors with idealized switches for the first-cut design, b) model with capacitances used by simulator SWITCH-1, c) model with conduction losses and switching losses used for the second-cut design.

TABLE I
BASIC PARAMETERS OF THE CLASS-D AMPLIFIER WITH TRANSISTORS IRF510, IRF520, IRF530

Transistor	P_{Dmax}	I_{Dmax}	R_{on}	C_O	I_O	P_O	P_{Ctot}	P_{SWtot}	η_D
	W	A	Ω	pF	A	W	W	W	%
IRF510	33	4.9	0.76	80	3.137	88.56	3.739	1.444	91.96
IRF520	46	8.0	0.38	180	3.200	92.16	1.946	3.249	92.14
IRF530	67	12.2	0.24	290	3.224	93.56	1.247	5.234	91.06

Transistor parameters P_{Dmax} and I_{Dmax} for t_C=60°C, R_{on} – for t_J=80°C. C_O is the equivalent linear large-signal output capacitance calculated for v_{DS} variations in the range 0 – 100V.

Using (9 - 12) we obtain power efficiency of the amplifier

$$\eta_D = \frac{P_O}{P_O + P_{Ctot} + P_{SWtot} + P_L}. \quad (13)$$

The values of I_O, P_O, P_L, P_{Ctot}, P_{Swtot} and η_D calculated for transistors IRF 510, IRF520, IRF 530 are in Table 1. The required output power can be ensured only by IRF520 and IRF530 transistors. For further analysis and design transistor IRF530 has been selected to secure the highest output power.

C. Second Stage – Simulation on Idealized Switch Level

The initial design of the amplifier with two transistors IRF530 has been simulated by the ideal-switch-level simulator SWITCH-1 using the model of Fig. 4b. Steady-state plots of switch current (i_{Dmax} =3.266A) and the areas of parasitic Dirac impulses (Q_{SW}= 55.1nC) are presented in Fig. 5. The computed amplitudes of output current I_O and the power P_O are a little bit larger then those obtained by (8,9). Conduction losses may be estimated using the value of I_O obtained by simulation and formula (11). On the contrary, switching losses caused by charging and discharging output capacitances of both power transistors are obtained exactly

$$P_{SW} = f_O Q_{SW} V_S = 5.234\,\text{W}. \quad (14)$$

In the second-cut cut design the value of capacitance C_S bypassing the supply (Fig. 6) is to be chosen. A minimum value of C_S providing 1% h.f. ripples in the supply voltage is [36]

$$C_{Smin} \cong \frac{5.6}{f_O R_L} = 0.31\mu\text{F}. \quad (15)$$

The above assumed situation (no cross-conduction current) depends on the parameters of power transistors and gate driving circuits. Therefore, the next step is designing the gate driving circuits. Let us assume a typical gate driving circuit (Fig. 6). It consists of a driving generator (equivalent parameters e_g, r_g), a coupling transformer Tr with two secondary windings and clamping circuits (C_1, C_2, R_{GS1}, R_{GS2} and diodes D_1, D_2). Let us assume that BAT 18 Schottky diodes are used and the circuits C_1, R_{GS1} and C_2, R_{GS2} do not distort rectangular gate-source pulses

$$R_{GS1}C_1 = R_{GS2}C_2 >> 0.5T_O = 500\text{ns}. \quad (16)$$

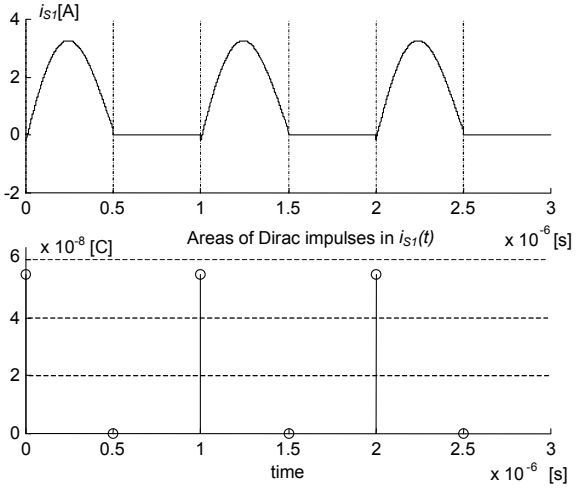

Fig. 5. Current through switch S_1 for the model from Fig. 4c calculated using simulator SWITCH-1.

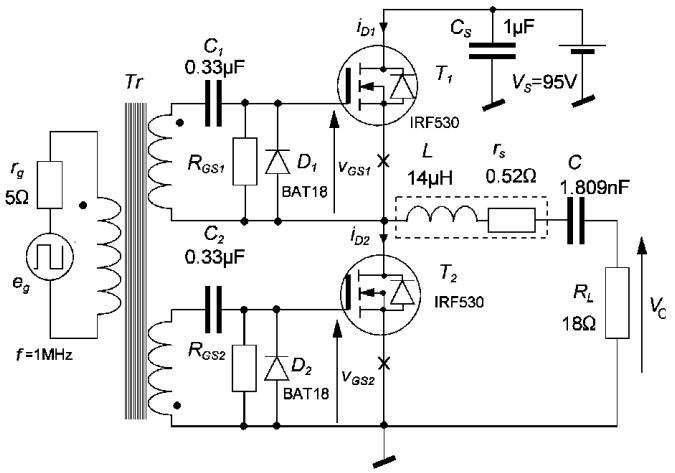

Fig. 6. Circuit diagram of the analyzed 95W/1MHz Class-D resonant amplifier.

D. Third Stage – Physical Simulation and Improvement

The gate-source driving voltage waveforms of T_1, T_2 are complex functions of the amplifier designable parameters, particularly in the ON and OFF transition instances. The waveforms are distorted due to non-ideal coupling transformer *Tr* (specifically its leakage inductance). In a correctly designed amplifier components should be adjusted to avoid cross-conduction current through T_1, T_2. In the initial design it is difficult to check it. This problem can be resolved by using the full physical model of power transistors. In the SPICE simulation driving waveforms and some parasitic components can be incorporated (e.g. leakage inductances, main inductance and series resistances of the transformer) but it offers only the transient analysis. The quality factor of the output resonant circuits is high (Q_L=5) and it can be assumed that waveforms generated by PSPICE during simulation .TRAN can be regarded as the steady state after 300 periods (300μs).

The driving waveforms v_{GS1}, v_{GS2} (Fig. 7) can be corrected by series or parallel dumping resistances in the gate driving circuit, e.g. shunt resistors R_{GS1}, R_{GS2}, Fig. 6. We try to adjust resistances R_{GS1}, R_{GS2} to avoid a cross-conduction current for the assumed parameters of the driving signal source (e_g, r_g) and the coupling transformer *Tr* leakage inductance L_l.

The first simulation was carried out for R_{GS1}=R_{GS2}=1kΩ, C_1=C_2=0.33μF, and the rectangular 0.5 duty cycle driving voltage $e_g(t)$ – Fig. 6. The leakage inductance of the transformer *Tr* was assumed L_l=0.15μH, the main inductance - L_m= 22μH. These values are typical in a bifilar-wound ferrite 1MHz transformer used in the discussed amplifier. The output resistance of the driving signal source was r_g=5Ω - a typical value of MIC4423 driver. The peak-to-peak value of $e_g(t)$ was E_g=10V.

SPICE results (Figs. 7a,b,c) show that for these conditions pulses of the cross-conduction current through the power transistors are high (8A), causing high losses (38.0W in both transistors) and low efficiency (69.8%). These conditions cannot be accepted, although the output power is correct (94.1W).

The second simulation was performed for the modified input circuit of the analyzed amplifier. Instead of the single 0.5 duty cycle generator e_g, r_g and 3-wire transformer *Tr* (Fig. 6)

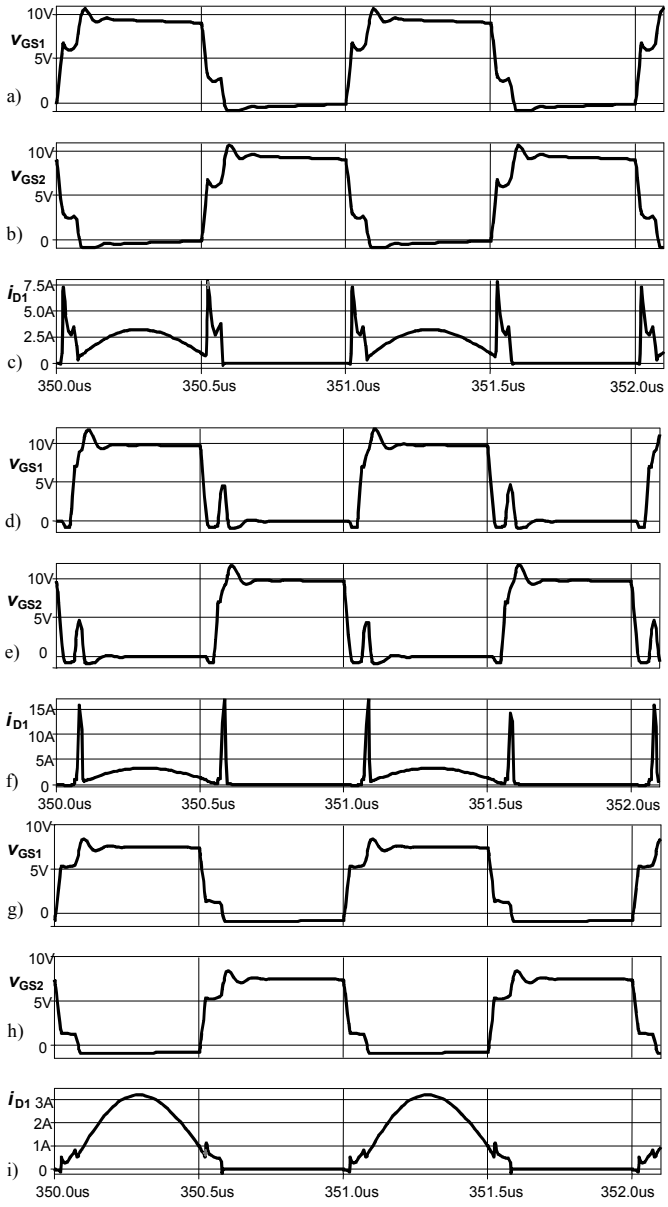

Fig. 7. PSPICE simulations of 1MHz Class-D resonant amplifier; a) - c) basic gate-drive circuit (Fig. 6) and R_{GS}=1kΩ, d) - f) modified gate-drive circuit with 45ns dead time and R_{GS}=1kΩ, g) - i) basic gate-drive circuit (Fig. 6) and R_{GS}=100Ω.

two π-phase shifted gate-drive generators with 45ns dead time were used (and two coupling 1:1 transformers with L_l=0.15μH). Values of E_g, r_g, R_{GS1}, R_{GS2}, C_1, C_2 remained the same. The results (Fig. 7f) show that for R_{GS1}=R_{GS2}=1kΩ, C_1=C_2=0.33μF dead time cannot eliminate cross-conduction current pulses. Losses slightly increased (43.0W) and efficiency decreased (67.2%). This effect is caused by the parasitic gate pulses resulting from differentiation of the rising edge of the drain-source voltage by the transistor gate-drain capacitance (Figs. 7 d, e). These pulses can be reduced in two ways: by decreasing the slope of drain-source voltage (class DE operation) or by decreasing internal resistance of the gate-drive circuit.

The third simulation was for the modified, more complicated gate-drive circuit (with two π-phase shifted gate-drive generators and 45ns dead time) and R_{GS1}, R_{GS2} reduced ten times, i.e. to 100Ω. For these values parameters were satisfactory: P_O= 93.14W, η_D=92.1%.

The fourth simulation was performed for the basic simple gate-drive circuit (Fig. 6) with R_{GS1}, R_{GS2} equal to 100Ω. This decreased the cross conduction current pulses (Figs. 7g, h, i), reducing losses in power transistors to

$$P_{\mathrm{Ddiss}} = 6.214W\,, \tag{17}$$

and increasing efficiency to

$$\eta_{\mathrm{D}} = 91.69\%\,. \tag{18}$$

The output power equals

$$P_{\mathrm{O}} = 93.81W\,. \tag{19}$$

These values are close to the values calculated in the initial design (see Table I, IRF 530) and satisfy the design specifications. This fact confirms that the presented initial-design of the Class-D amplifier (Section IIIB) was correct.

Effects of parasitic inductances in the amplifier were tested in the subsequent simulations. These simulations proved that even a very low inductance (e.g. 50 - 100nH) connected in series with the drain or source changes notably voltage and current waveforms in the amplifier. In particular, parasitic inductance of the transistor source connection (marked by *x* in Fig. 6) must be as low as possible.

Effects of non-ideal 0.5 duty cycle of the driving voltage $e_g(t)$ (Fig. 6) were also investigated. Simulations proved that small inaccuracy of this parameter (0.45–0.55) does not disturb the amplifier operation: output power was at least P_{Omin}=90.6W, efficiency above η_{Dmin}=91.5%, and THD below 3.6%.

E. Fourth Stage - Optimization-based Design Improvement

The values of η_D (18) and P_O (19) are acceptable but we are not sure whether these parameters cannot be increased. Besides, by decreasing resistances R_{GS1}, R_{GS2} we increased the drive power delivered by the generator and reduced power gain of the amplifier. Adjustment of component values that optimize the amplifier properties using SPICE simulations is rather labor-consuming. This task can be solved using the SCAD environment with SPECTRE as a co-operating simulator. We demonstrate sample results (Fig. 8) of the design exploration. In this example influence of the gate-source resistors R_{GS1}=R_{GS2}=R_{GS} and peak-to-peak voltage of the driving generator E_g on the output power P_O, efficiency η, power dissipated in both transistors P_{Ddiss}, and power gain G_P have been investigated. The obtained plots show that with the increase of R_{GS} parameters η, P_{Ddiss} are getting worse but another parameters improve (P_O and G_P). Contrary, with the increase of E_g only the output power P_O is improved but the other parameters become worse. Negative effects of increasing E_g can be compensated by decreasing R_{GS} (except for power gain G_P). From the presented relationships we conclude that the values

$$E_{\mathrm{g}} \in (9.5 \div 10)\mathrm{V}, \quad R_{\mathrm{GS}} \in (100 \div 200)\Omega., \tag{20}$$

parameters of the amplifier are sufficiently good: P_O≥94,3W,

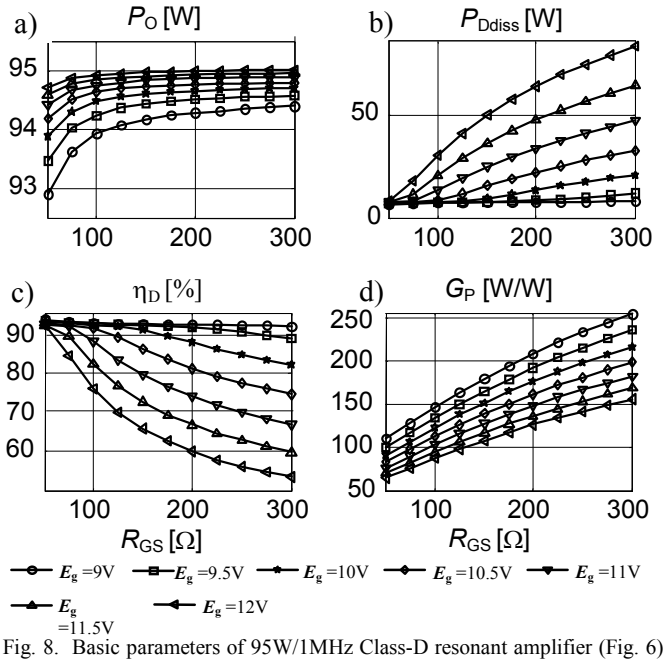

Fig. 8. Basic parameters of 95W/1MHz Class-D resonant amplifier (Fig. 6) vs. gate-source resistance R_{GS} for different values of E_g obtained by design exploration using SCAD environment with SPECTRE; a) output power, b) power loss in both transistors IRF 530, c) total efficiency, d) power gain.

η_D≥88%, G_P≥125W/W. However, by adjustment of E_g, R_{GS} some amplifier parameters can be improved (e.g. P_O and η_D).

SCAD software can also be used for optimization-based design of the amplifier. We propose the bi-objective Pareto maximization of the output power P_O and the efficiency η_D equivalent to the solution of the scalar problems with parametrized η_{Di}

$$\max_{R_{\mathrm{GS}},E_{\mathrm{G}}} \{P_{\mathrm{O}} \mid \eta_{\mathrm{D}} < \eta_{\mathrm{Di}}\} \tag{21}$$

SCAD solution of (21) gives a final solution in the form of the Pareto curve shown in Fig. 9a accompanied with the optimal relation of G_P versus efficiency η_D in Fig. 9b. A set of optimal parameter values R_{GS}, E_G are collected in the caption of Fig. 9. We observe a trade-off between output power and efficiency. A maximal output power can be achieved only with unacceptably low efficiency and power gain levels. Hence, a final selection of one point on the Pareto curve is a designer decision.

In our design to increase power gain the following parameters giving a small decrease of the output power have been selected: R_{GS}=100.2Ω, E_g=10.5V, P_O=94.6W, η_D=91.3%, G_P =112.7W/W (point A on the curve in Fig. 9).

F. Experimental Verification

The designed Class-D amplifier (Fig. 6) was built and tested to verify the presented design procedure. In the resonant circuit a large coreless toroidal coil and 4 connected in parallel ceramic high-frequency capacitors were applied. Measured loaded quality factor of this circuit was high (Q_L=170) and the self-resonance frequency of the coil was f_{res}=12.8MHz.

The gate-source resistances were fixed at the value R_{GS}=100Ω and the peak-peak voltage of the driving generator was E_g=10.5V.

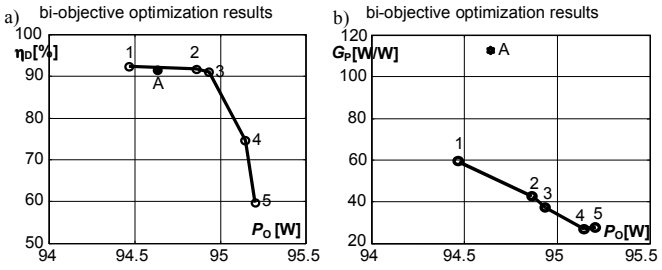

Fig. 9. Results of bi-objective design of the Class-D amplifier: a) Pareto curve representing an optimal trade-off between efficiency and output power; b) power gain versus output power; symbols 1 – 5 and A denote 6 possible designs equivalent in Pareto sense, but differing in P_O and η_D.
1: R_g=36.9Ω, E_g=11.9V, P_O=94.46W, η_D=92.34%, G_P =59.7W/W
2: R_g=32.8Ω, E_g =13.9V, P_O=94.86W, η_D=91.7%, G_P=42.8W/W
3: R_g =29.9Ω, E_g =14.8V, P_O=94.93W, η_D=91.1%, G_P =37.4W/W
4: R_g=29.6Ω, E_g =17.4V, P_O=95.1W, η_D=74.6%, G_P =27.0W/W
5: R_g =37.2Ω, E_g =17.6V, P_O =95.2W, η_D =59.7%, G_P =27.7W/W
A: R_g =100.2Ω, E_g =10.5V, P_O =94.6W, η_D =91.3%, G_P =112.7W/W

The amplifier was assembled on a double-sided printed circuit board with one conducting surface used as the ground. The dc supply V_S is bypassed (C_S, Fig.6) by two 0.1μF ceramic and two 0.47μF polypropylene capacitors. Transistors T_1, T_2 and bypassing capacitors were mounted on opposite sides of the printed circuit board and connections between these components were made short and wide. In this way parasitic inductance of T_1, T_2, C_S mesh was minimized.

The experiments confirm that the designed amplifier operates correctly without parasitic oscillations. Waveforms measured from the prototype (Fig. 10) are very similar to the waveform obtained from SPICE (Fig. 7).

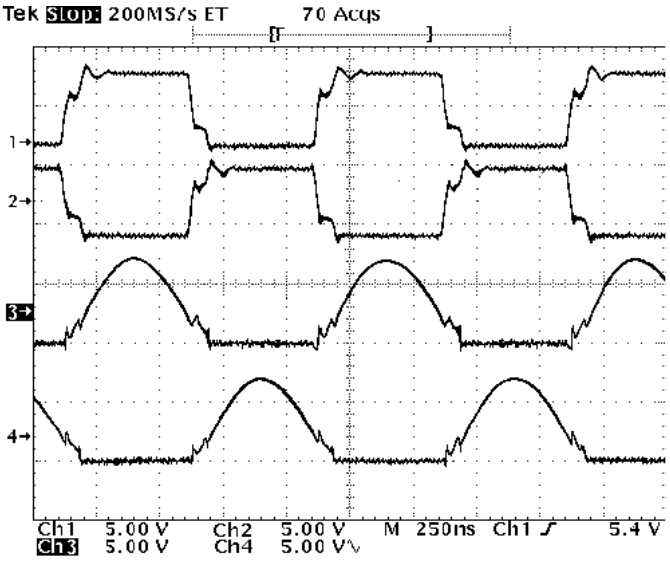

Fig. 10. Measured signals in the experimental 95W/1MHz Class-D amplifier; (1) – u_{GS2}, (2) – u_{GS1} (using auxiliary wide-band 1:1 transformer), (3) - i_{D2} (using 2V/A transformer current probe), (4) - i_{D1} (using 2V/A transformer current probe).

The measured output voltage was V_O=41.5V (rms) and power supply – P_S=104.1W. The output power was

$$P_O = 95.7W \tag{22}$$

which results in the amplifier efficiency

$$\eta_D = 91.9\% \tag{23}$$

Powers dissipated in both transistors were measured independently using the thermal method: P_{Ddiss}=7.6W. Thus, considering the loaded quality factor (Q_L=5) and the quality factor of the inductance (Q_O=170) the more accurate estimation of the total efficiency is

$$\eta_D = \left(1 - \frac{Q_L}{Q_O}\right)\frac{P_S - P_{Ddiss}}{P_S} \cong 90.0\%. \tag{24}$$

The measured values of the amplifier parameters are close to the results of the PSPICE simulations (18, 19), to the initial design (8, 12) (due to the elimination of cross-conduction current) and to the slightly improved optimized design (Fig.9).

IV. Conclusions

The paper presents a multi-layer methodology to the design of switch-mode power circuits. It discusses modeling, simulation, design exploration, multi-objective optimization, and experimental verification. Models of switching active elements on different levels of complexity have been exploited.

A four-layer approach to the switch-mode power circuit design has been proposed and explored. First, idealized models of switching elements and simple engineering formulae produce a design far from optimal. Then on the second layer SWITCH simulator has been used. Also other similar simulators are available, one of advantages of our SWITCH simulator is implementation of the secant algorithm for the steady state. Idealized models of switches considerably reduce simulation time. Our experience has shown (see the design example) that results from such a simulation roughly reflect circuit operation and enable cheap elimination of unacceptable designs and selection of the best engineering ideas as a good starting point for further interactive and then optimization-based design improvement.

At the second layer a more exact simulation, based on physical models, is applied. SPICE-type simulators analyze them with large computational effort, especially in the neighborhood of critical switching instances. This layer has provided computer verification and improvement of our initial design.

At the most advanced fourth layer we have proposed an improvement of the design obtained from the layer three, based on multi-objective SCAD optimization. This software provides design exploration and curves of optimal trade-offs which can be used by the designer as a support of his decision. Efficiency and convenience of this software in engineering practice has been confirmed in Section III.

The proposed methodology and software tools significantly reduce expensive and labor-consuming experimental design procedure based on SPICE-like simulation and empirical improvement of the built prototype. On the second layer SWITCH-like simulation eliminates about 80% of simulation time. The third layer is time-consuming but due to the efficient first layer it can be limited to a small number of good initial designs. The fourth layer is very fast comparing with

equivalent SPICE-based interactive procedure, where curves of optimal trade-offs are unavailable. Crucial point of the third layer simulation and the fourth layer optimization is availability of accurate, reliable transistor models. Though physical models of switching transistors are of quite high numerical complexity this computer optimization is of extremely small time-consumption comparing to experimental optimization where designers have to assembly several circuit prototypes of and increase their quality experimentally.

A final conclusion is that according to the introduced four-layer design procedure a class-D resonant amplifier has been successfully designed, with the final values of parameters being a good compromise between several quality criteria (confirmed by measurements of an experimental real circuit). We have shown that even the basic simple circuit provided very good features comparable to the class-E and class-DE amplifiers.

REFERENCES

[1] J. Abu-Qahouq and I. Batarseh, "Unified steady-state analysis of soft-switching DC-DC converters", *IEEE Transactions on Power Electronics*, vol. 17, no. 5, pp. 684-691, Sept. 2002.

[2] D. del-Aguila-Lopez, P. Pala-Schőnwalder, P. Molina-Gaudo, and A. Mediano-Herdia, "A discrete-time technique for the steady-state analysis of nonlinear class-E amplifiers", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 6, pp. 1358-1366, June 2007.

[3] Ch. Basso, "Switch-mode power supplies: Spice simulations and practical designs", McGraw-Hill Professional, 2008.

[4] D. Bedrosian and J. Vlach, "Time-domain analysis of networks with internally-controlled switches", *IEEE Transactions on Ciruits and System I: Fundamental Theory and Applications*, vol. 39, no. 3, pp. 199-212, Mar. 1992.

[5] D.G. Bedrosian and J. Vlach, "An accelerated steady-state method for networks with internally controlled switches", *IEEE Transactions on. Circuits and Systems I: Fundamental Theory and Applications,* vol. 39, no. 7, pp. 520-530, Jul. 1992.

[6] S. Ben-Yaakov, "Average simulation of PWM converters by direct implementation of behavioral relationships", in *Proc. Applied Power Electronics Conference*, San Diego, USA, 1993, pp. 510-516.

[7] M. Bukowski, "Steady-state time-domain analysis of nonlinear circuits with periodic input via secant method", in *Proc. European Conference of Circuit Theory and Design*, Istanbul, 1995, pp. 135-138.

[8] J.M. Burdio and A. Martinez, "A unified discrete-time state-space model for switching converters", *IEEE Transactions on Power Electronics*, vol. 10, no. 6, pp. 694-707, Nov. 1995.

[9] M. Celik, A. Atalar, and M.A. Tan, "A new method for the steady-state analysis of periodically excited nonlinear circuits", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications.*, vol. 43, no. 12, pp. 964-972, Dec. 1996.

[10] C.C. Chan and K.T. Chau, "A fast and exact time-domain simulation of switched mode power regulators", *IEEE Transactions on. Industrial. Electronics*, vol. 39, no. 4, pp. 341-350, Aug. 1992.

[11] W. J. Chudobiak and D. F. Page, "Frequency and power limitations of Class-D transistor amplifiers", *IEEE J. Solid State Circuits*, vol. SC-4, no 1, pp. 25-37, Feb. 1969.

[12] H.S.-H. Chung and A. Ioinovici, "Fast computer-aided simulation of switching power regulators based on progressive analysis of the switches' state", *IEEE Transactions on Power Electronics*, vol. 9, no. 2, pp. 206-212, Mar 1994.

[13] J.C. Contreras-Sampayo, J. Usaola-Garcia, and A.R. Wood, "Steady-state algorithm for switching power electronic devices", *IEE Proceedings Electric Power Applications*, vol 148, no. 2, pp. 245-250, Mar. 2001.

[14] K. B. Dalaci, K. Gulez, and G. Cansever, "The design of a push-pull switch-mode power supply for AC drives", in *Proc. 30th Annual Conference of IEEE Industrial Electronics Society,* vol. 2, Busan Korea, 2004, pp. 1201-1206.

[15] B. De Kelper, L.A. Dessaint, K. Al-Haddad, and H. Nakra", A comprehensive approach to fixed-step simulation of switched circuits", *IEEE Transactions on Power Electronics*, vol. 17, no. 2, pp. 216-224, Mar. 2002.

[16] N. Femia, G. Spagnuolo, and V. Tucci, "Internal analysis in power electronics", *Journal of Ciruits, Systems, and Computers*, vol. 5, no. 3, pp. 317-336, Sept. 1995.

[17] N. Femia, G. Spagnuolo, and M. Vitelli, "Steady-State analysis of soft-switching converters", *IEEE Transactions on Circuit and. Systems I: Fundamental Theory and Applications,* vol. 49, no. 7, pp. 939-954, Jul. 2002.

[18] N. Femia, G. Spagnuolo, and M. Vitelli, "Steady-state analysis of PWM DC-to-DC regulators", *IEEE Transactions on Aerospace and Electronic Systems*, vol. 39, no. 1, pp. 318-334, Jan. 2003.

[19] F. Guinjoan, J. Calvente, A. Poveda, and L. Martinez, "Large-signal modeling and simulation of switching DC-DC converters", *IEEE Transactions on Power Electronics*, vol. 12, no. 3, pp. 485-494, May 1997.

[20] G. Hua, E.X. Yang, Y. Jiang, and F.C. Lee, "Novel zero-current transition PWM converters", *IEEE Transactions on Power Electronics*, vol. 9, no. 6, pp. 601-606, Nov 1994.

[21] *IRF Hexfet Power MOSFETs*, International Rectifier, USA, 2010. Available at: *www.irf.com*

[22] T. Kato, "Efficient steady state analysis method with sensitivities of switch timings by the shooting method", in *Proc. Power Conversion Conference*, Yokohama, Japan, 1993, pp. 550-556.

[23] T. Kato, "Multi-rate transient analysis of power electronic circuits by the envelope-following method with sensitivities of switch timings", in *Proc. IEEE Power Electronics Specialists Conference*, vol. 2, Taipei, Taiwan, 1994, pp. 1277-1281.

[24] T. Kato and W. Tachibana, "Periodic steady-state analysis by a modified shooting method for a power electronic circuit", *Proc. Power Conversion Conference*, Nagaoka, Japan, 1997, pp. 367-372.

[25] M. Kazimierczuk and D. Czarkowski, "Resonant power converters", John Wiley, 1995.

[26] M. Kazimierczuk, "RF Power Amplifiers", J. Wiley, 2008.

[27] D.J. Kessler and M.K. Kazimierczuk, "Power losses and efficiency of class-E power amplifier at any duty ratio", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 9, pp. 1675-1689, Sept. 2004.

[28] K.S. Kundert and A. Sangiovanni-Vincentelli, "Steady-state methods for simulating analog and microwave circuits", Kluwer, Boston, 1990.

[29] D. Li and R. Tymerski, „A comparison of steady-state methods for power electronic circuits", *Proc. IEEE Power Electronics Specialists Conference*, 1998, pp. 1084-1090, vol. 2.

[30] Z. Lizhong and J. Vlach, "Analysis and steady-state of nonlinear networks with ideal switches", *IEEE Transactions on Circuits and System I: Fundamental Theory and Applications*, vol. 42, no. 4, pp. 212-214, Apr. 1995.

[31] A.M. Luciano and A.G.M. Strollo, "A fast time-domain algorithm for the simulation of switching power converters", *IEEE Transactions on Power Electronics*, vol. 5, no. 3, pp. 363-370, July 1990.

[32] D. Maksimović and S. Ćuk, "Switching converters with wide DC conversion range", *IEEE Transactions on Power Electronics*, vol. 6, no. 1, pp. 151-157, Jan. 1991.

[33] D. Maksimovic, "Automated steady-state analysis of switching power converters using a general-purpose simulation tool", in *Proc. IEEE Power Electronics Specialists Conference*, vol. 2, St. Louis, USA, 1997, pp. 1352-1358.

[34] A. Massarini, U. Reggiani, and M. Kazimierczuk, "Analysis of networks with ideal switches by state equations", *IEEE Transactions on Circuits and System I: Fundamental Theory and Applications*, vol. 44, no. 8, pp. 692-697, Aug. 1997.

[35] *SimPowerSystems 4 User Guide*, The Mathworks, Inc., Massachusettts, 2007.

[36] J. Modzelewski, "Power supply problems of class-D and class-DE high-frequency tuned power amplifiers", in *Proc. 1st National Conference on Electronics*, Kolobrzeg, Poland, 2002, pp. 325-330.

[37] Z. Mrcarica, T. Ilic, and V. B. Litovski, "Time-domain analysis of nonlinear switched networks with internally controlled switches", *IEEE Transactions on Circuit and. Systems I: Fundamental Theory and Applications*, vol. 46, no. 3, pp. 373-378, Mar. 1999.

[38] M. Nakahara, "A fast computer algorithm for switching converters", *IEEE Transactions on Power Electronics.*, vol. 12, no. 1, pp. 180-186, Jan 1997.

[39] J. Ogrodzki, "Circuit simulation methods and algorithms", CRC Press, Boca Raton, 1994.

[40] J. Ogrodzki and M. Skowron, "The charge-flux method in simulation of first kind switched circuits", in *Proc. European Conference of Circuit Theory and Design,* Stresa, Italy, 1999, pp. 475-478.

[41] J. Ogrodzki, M. Skowron, J. Wojciechowski, L.J. Opalski, M. Bukowski, J. Modzelewski, and K. Zamłyński, "SWITCH-1. Prototype circuit simulator for switch-mode circuits. Users Guide", Technical Report, Warsaw University of Technology, Warsaw, Poland, 1999.

[42] J. Ogrodzki, "OPTIMA version 2.0e – Users Guide", Technical Report, Warsaw University of Technology, Warsaw, 1995.

[43] A. Opal and J. Vlach, "Consistent initial conditions of linear switched networks", *IEEE Transactions on Circuits and Systems*, vol. 37, no. 3, pp. 364-372, Mar. 1990.

[44] L. J. Opalski and M. A. Styblíński, "GOSSIP– a generic system for statistical circuit design", in *Proc. European Design Automation. Conference*, Hamburg, Germany, 1992, pp. 572-577.

[45] P. Pala-Schonwalder and J.M. Miro-Sans, "A discrete-time approach to the steady-state analysis and optimization of non-linear autonomous circuits", *International Journal of Circuit Theory and Applications*, vol. 23, pp. 297-310, July/Aug. 1995.

[46] P. Pejović and D. Maksimović, "A method for fast time-domain simulation of networks with switches", *IEEE Transactions on Power Electronics*, vol. 9, no. 4, pp. 449-456, July 1994.

[47] P. Pejović and D. Maksimović, "A new algorithm for simulation of power electronic systems using piecewise-linear device models", *IEEE Transactions on Power Electronics*, vol. 10, no. 3, pp. 340-348, May 1995.

[48] *PSPICE - Circuits Analysis Reference Manual, ver. 8.0*, MicroSim Corp., July 1997.

[49] A. Shirsavar, "Teaching practical design of switch-mode power supplies", *IEEE Trans. Education*, vol. 47, no. 4, pp. 467-473, Nov. 2004.

[50] *SPECTRE Users Guide*, Cadence Design System, 1997.

[51] *STM Transistor Families*, ST Microelectronics, Available at: *www.st.com*

[52] T. Suetsugu and M. K. Kazimierczuk, "Analysis and design of class E amplifier with shunt capacitance composed of nonlinear and linear capacitances", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 7, pp. 1261-1268, July 2004.

[53] M.M. Tabrizi and N. Masoumi, "High frequency class E switch-mode power amplifier design and optimization with random search algorithm", in *Proc. The 16th International Conference on Microelectronics*, Tunis, Tunisia, 2004, pp. 283-286.

[54] C.H. Trevisio, O.C. De Freitas, and V.J. Farias, "A ZVS-ZCS-PWM self-resonant DC-DC sepic converter", in *Proc. International Conference on Industrial Electronics.*, *Control and Instrumentation*, vol. 1. Bologna, Italy, 1994, pp. 176-181.

[55] C. Tseng and C. Chen, "On the ZVT-PWM Cuk converter", *IEEE Transactions on. Industrial. Electronics*, vol. 45, no. 4, pp. 674-677, Aug. 1998.

[56] K.K. Tse, H.S-H. Chung, and S.Y.Hui, "Quadratic state-space modeling technique for analysis and simulation of power electronic converters", *IEEE Transactions on Power Electronics*, vol. 14, no. 6, pp. 1086-1100, Nov. 1999.

[57] J. Valsa and J. Vlach, "SWANN - A programme for analysis of switched analogue non-linear networks", *International Journal of Circuit Theory and Applications*, vol. 23, pp. 369-379, July/Aug. 1995.

[58] J. Vlach, J.M. Wojciechowski, and A. Opal, "Analysis of nonlinear networks with inconsistent initial conditions", *IEEE Transactions on Circuit and. Systems I: Fundamental Theory and Applications*, vol. 42, no. 4, pp. 195-200, Apr. 1995.

[59] J. Vlach and A. Opal, "Modern CAD methods for analysis of switched networks", *IEEE Transactions on Circuit and. Systems I: Fundamental Theory and Applications*, vol. 44, no. 8, pp. 759-762, Aug. 1997.

[60] E. Ven den Ejinde and J. Schoukens, "Steady-state analysis of a periodically excited nonlinear system", *IEEE Transactions on Circuit and. Systems*, vol. 37, no. 2, pp. 232-242, Feb. 1990.

[61] V. Vorpérian, "Quasisquare-wave converters: Topologies and analysis", *IEEE Transactions on Power Electronics.*, vol. 3, no. 2, pp. 183-191, March 1988.

[62] Q. Wang and J.R. Marti, "A waveform-relaxation technique for steady-state initialization of circuits with nonlinear elements and ideal diodes", *IEEE Transactions on. Power Delivery*, vol. 11, no. 3, pp. 1437-1443, July 1996.

[63] J. White and S.B. Leeb, "An envelope-following approach to switching power converter simulation", *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 303-307, Apr. 1991.

[64] T. G. Wilson, "Life after the schematic: The impact of circuit operation on the physical realization of electronic power supplies", *Proceedings of the IEEE*, vol. 76, no 4, pp. 325-334, Apr. 1988.

[65] B.K.H. Wong and H.S.H. Chung, "A general-oriented simulation technique for power electronic systems using quadratic branch voltage extrapolation", *IEEE Transactions on Industrial Electronics*, vol. 44, no. 4, pp. 492-501, Aug. 1997.

[66] B. K. H. Wong and H.S.H. Chung, "Steady-state analysis of PWM DC/DC switching regulators using iterative cycle time-domain simulation", *IEEE Transactions on Industrial Electronics*, vol. 45, no. 3, pp. 421-432, June 1998.

[67] B.K.H. Wong and H. Chung, "Dual loop iteration algorithm for steady-state determination of current-programmed DC/DC switching converters", *IEEE Transactions on Circuit and. Systems I: Fundamental Theory and Applications*, vol. 46, no. 4, pp. 521-526, Apr. 1999.

[68] J. Wojciechowski, B. Sawionek, Z. Michalski, and J. Vlach, "Symbolic large-signal analysis of switched circuits", *Circuits, Systems, and Signal Processing Journal*, vol.17, no. 3, pp. 321-334, March 1998.

[69] M.K.W. Wu, C. K. Tse, and O.B.P. Chan, "Development of an integrated CAD tools for switching power supply design with EMC performance evaluation", *IEEE Transactions on Industry Applications,* vol. 34, no. 2, pp. 364-373, March/Apr. 1998.

[70] V. Yaskiv, "The new methods of switch-mode power supply designing for computer facilities", in *Proc. International Workshop on Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications*, 2001, pp. 87-90.

[71] F. Yuan and A. Opal, "Computer methods for switched circuits", *IEEE Transactions on Circuit and. Systems I: Fundamental Theory and Applications*, vol. 50, no. 8, pp. 1013-1024, Aug. 2003.

[72] K. Zamłyński and J. Ogrodzki, "Electrothermal analysis of ICs", in *Proc. IEEE Internationall Symposion on Circuits and Systems*, London, U.K., 1994, pp. 17-20.

[73] K. Zamłyński, "Idealized models of switches for SPICE and OPTIMA simulation of circuits with internally controlled elements", in *Proc. XXI National Conference on Circuit Theory and Electronic Circuits*, Poznań, Poland, 1998, pp. 287-292.