ELECTRON TECHNOLOGY
ISSN 1897-2381
http://www.ite.waw.pl/etij/
Internet Journal

EM EMISSIONS OF ICs IMPLEMENTED IN FPGA – INFLUENCE OF FLOOR PLAN AND ELECTRIC FUNCTION

J. SZCZĘSNY, J. F. KOŁODZIEJSKI

Institute of Electron Technology, al. Lotników 32/46, 02-668 Warszawa, Poland

Received Febr. 2, 2007; modified April 6, 2007; accepted April 17, 2007; published April 30, 2007

ABSTRACT

In the paper some investigations are presented aiming to check the influence of IC floor plan and the circuit function on its electromagnetic emissions. As the test vehicle Xilinx FPGA XCV800 type was used, in which two types of multiplicators were implemented. To compare the effects, high frequency currents in supply and ground pins of the circuits as well as near field disturbances were measured over the circuits.

1. Introduction

Current and voltage transients related to high frequency switching and short rise/fall times of useful signals cause electromagnetic (EM) emissions of digital ICs [1–3]. Transients resulting from circuits activity spread out as the conductive signals that may couple onto the power, control and signal lines and through the IC pins reach the co-operating components on the PCB. We can differentiate three emission mechanisms: conducted emission through supply lines, conducted emission through input/output lines, direct radiated emission from the circuit. The simultaneous switching of large numbers of output buffers inside complex synchronous IC can produce fluctuations of current on supplying lines, known as a simultaneous switching noise (SSN) or $L(di/dt)$ noise (or delta-I noise). Resulting voltage glitches are proportional to the switching speed, number of gates that switch simultaneously and the effective inductance of the power line. Inductance determines the impedance of digital circuit power supply network and has significant influence on distribution of circuit currents, especially at high frequencies and when the supplying system impedance is higher than package impedance [3], [4]. Each interconnection line has an associated self-inductance L_S and mutual inductance M to surrounding lines. To minimize di/dt noise the inductance of wires, bonding structures and package pins should be minimized, mainly by increasing their cross-sectional dimensions, placing signal lines close to ground line or plane and keeping them as short as possible. Multiple power and ground connections as well as decoupling capacitors can also be very helpful. The above-specified factors are generally of different importance in various circuits. To find their influence on the EM emissions we choose an indirect method, based on the measurement of high frequency currents in ground and supplying pins of the two circuit versions implemented in the same FPGA as well as the measurement of their radiated emission [5]. Conducted emission through supply lines and radiated emission were considered in the work as a measure of inherent circuit activity. The results of realized work have rather quantitative (comparative) character.

2. Tested objects

As the basic test-circuit Xilinx FPGA of Vertex family XCV 800 type was used [6]. Two multiplication circuits were implemented in the FPGA. They represented two commonly known multiplicators versions. The first one was combinational (parallel), in which the digits to be multiplied are supplied simultaneously into the parallel inputs of multiplicator and multiply operation is realized by combinational circuit (see Fig. 1). The second one was sequential (series), in which one of the multiplied digits appears parallel on the multiplicator inputs and the other digit sequentially. The operations realized by the circuit are presented in Fig. 2.

The first impression coming from Fig. 1 and Fig. 2 is that in the case of combinational circuit switching operations appeared more often than in the case of sequential circuit, while the number of used signals available on the circuit pins was higher in the last case.

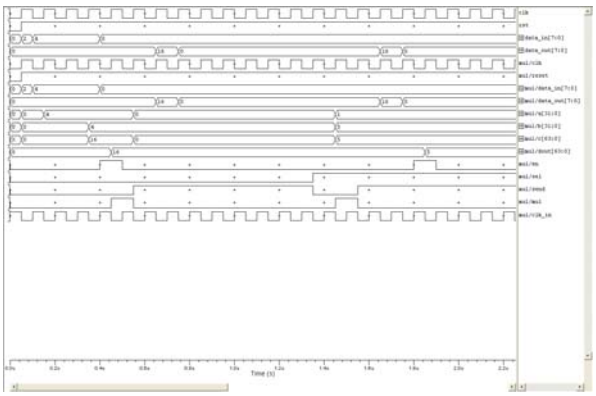


Fig. 1. Combinational multiplication – signals on the pins.

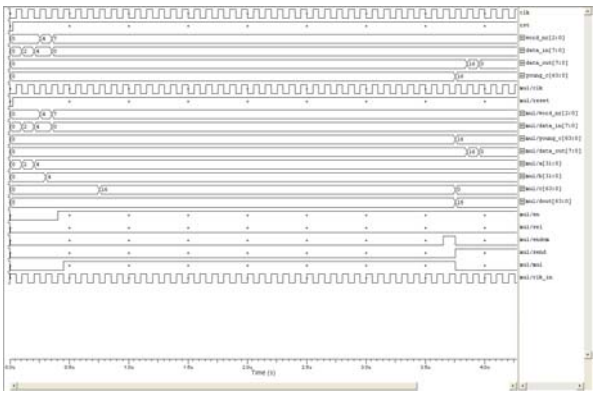


Fig. 2. Sequential multiplication – signals on the pins

The basic multiplicator circuits of both types were equipped with logical blocks having implemented RS 232 interface for data transmissions between the FPGA and PC. Other two circuits were prepared without this interface. These four projects of multiplicator circuits were further area and speed optimized, using the standard procedures offered by Xilinx software [7].

The following multiplicator circuits were then implemented in the FPGA:

- seq_area – sequential multiplicator circuit with RS 232 interface, optimized for minimum number of logical blocks;
- seq_speed – sequential multiplicator circuit with RS 232 interface, optimized for maximum speed of multiplication;
- seq_no_io_area – sequential multiplicator circuit without RS 232 interface, optimized for minimum number of logical blocks;
- seq_no_io_speed – sequential multiplicator circuit without RS 232 interface, optimized for maximum speed of multiplication
- comb_area – combinational multiplicator circuit with RS 232 interface, optimized for minimum number of logical blocks;
- comb_speed – combinational multiplicator circuit with RS 232 interface, optimized for maximum speed of multiplication;
- comb_no_io_area – combinational multiplicator circuit without RS 232 interface, optimized for minimum number of logical blocks
- comb_no_io_speed – combinational multiplicator circuit without RS 232 interface, optimized for maximum speed of multiplication;
- comb_area_replaced – comb_area circuit where the part of logical blocks were intentionally moved from its original places to the other ones.

The number of: engaged logical gates (total equivalent gate count for design), structures (total number of lookup tables) and blocks (number of occupied slices) of tested circuits are assembled in Table 1.

Table 1. Comparison of logical design features of the tested circuit

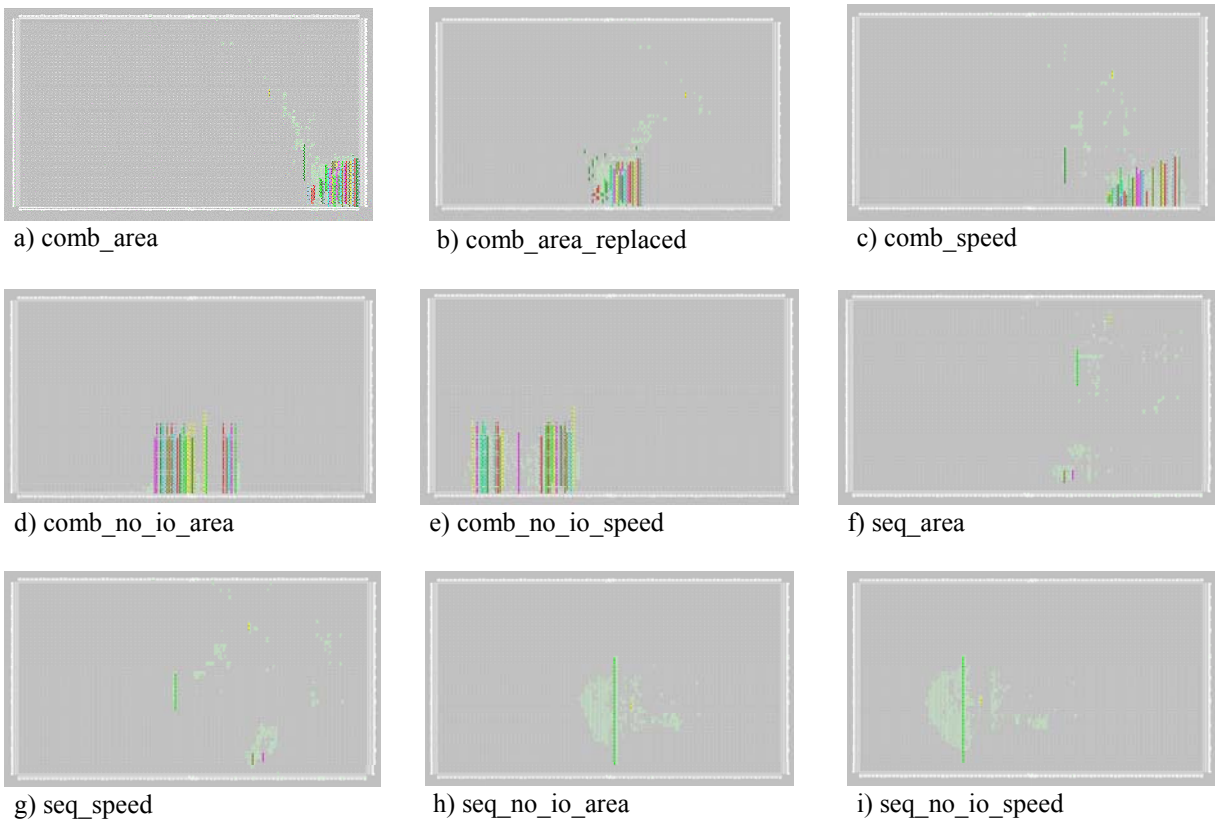
Tested circuits	Logical gates	Log. struct	Logical blocks	Configur.
1	2	3	4	5
comb_area	9 453	724	412	grouped + scattered
comb_area_replaced	9 453	724	412	grouped + scattered
comb_speed	9 775	725	496	grouped + scattered
comb_no_io_area	12 552	893	569	compact
comb_no_io_speed	13 448	893	719	compact
seq_area	3 404	260	178	scattered
seq_speed	3 423	268	183	scattered
seq_no_io_area	6 071	609	367	grouped + scattered
seq_no_io_speed	7 145	730	460	grouped + scattered

Only small part of generally available 9 408 of logical blocks in the used FPGA was engaged for implemented multiplier circuits. The smallest number of logical blocks, about 1%, was occupied by seq_area circuit and the largest number of these blocks, i.e. 7%, by the comb_no_io_speed circuit. The locations of logical blocks inside the examined circuits are presented in Fig. 3.

In the seq_speed circuit (Fig. 3g) logical blocks occupied the largest area of the FPGA while the number of these logical blocks was the smallest (similarly like for seq_area). The largest number of logical blocks was engaged in comb_no_io_speed, (Fig. 3e) and comb_no_io_area (Fig. 3d) circuits; all these blocks were grouped together. For the rest of combinational circuits, presented in Fig. 3a – c, only part of the logical gates were brought together while others were spread over the array. The logical blocks of all combinational multiplicators were located closer to the array edge than in the case of sequential circuits.

3. Measurements

Conducted emissions of investigated multiplicator circuits were measured in frequency and time domain. As the conducted disturbances, generated by



a) comb_area b) comb_area_replaced c) comb_speed

d) comb_no_io_area e) comb_no_io_speed f) seq_area

g) seq_speed h) seq_no_io_area i) seq_no_io_speed

Fig. 3. The plans (floorplans) of the active logical blocks of examined circuits inside the FPGA.

the circuits, we took into account high frequency currents flowing through supply V_{DD} and ground GND pins as well as the currents appearing inside the FPGA chip. These currents were measured with the help of a miniature magnetic field probe, as described in IEC 61967-6, which was placed in the fixed points approximately 1 mm over PCB tracks going to the mentioned pins and over the middle zone of FPGA package. Magnetic probe was connected through preamplifier to wideband oscilloscope or spectrum analyzer with upper frequency equals to 1 GHz. In time domain, about one hundred readings of peak-to-peak values, proportional to H component of near field, were regarded to calculate the average voltage in the given point. Radiated emissions were checked by measurement of electric component of the EM field with the help of near field Langer EMV-Technik probe (2x8 mm) fixed in the middle zone of FPGA package over the chip. During the measurement, tested circuit realized its prescribed multiply operation. It was possible to change the clock frequency in the range of 1 MHz to 50 MHz.

4. Obtained results

4.1. Disturbances measured in frequency domain

4.1.1. Conducted disturbances

High frequency currents in V_{DD} and GND pins for combinational and sequential circuits were measured at clock frequencies up to 50 MHz. Number of harmonics and occupied frequency band as well as amplitudes initially increased with clock frequency. The first peaks appeared in the range of 200 – 300 MHz. The harmonic frequencies were expanded to 1 GHz with the growth of the clock rate to approximately 10 MHz. The greatest number of harmonics and their highest amplitudes were observed for the clock rate 25 – 30 MHz. Unexpectedly, the number of harmonics and they amplitudes decreased for higher clock frequencies up to 50 MHz. The spectra of RF currents flowing through V_{DD} pin of the comb_area circuit are presented in Fig. 4 for 3 selected frequencies.

Only for the comb_no_io_speed and seq_no_io_speed circuits, the V_{DD} and GND pins RF currents and their spectrum components grew up within the whole range of clock frequency. The higher number of harmonics was observed in the case of comb_no_io_area and comb_no_io_speed circuits. The most pronounced harmonic content of high frequency currents was noticed in V_{DD} pin between 200 and 600 MHz and in GND pin in the range of 100 – 500 MHz.

A little higher amplitudes and larger number of harmonics of high frequency currents flowing through the V_{DD} and GND pins were observed for sequential circuits. The maximal amplitude values appeared in seq_no_io_speed circuit. On the other side, the smallest level of EM emissions was observed for seq_area and seq_speed circuits.

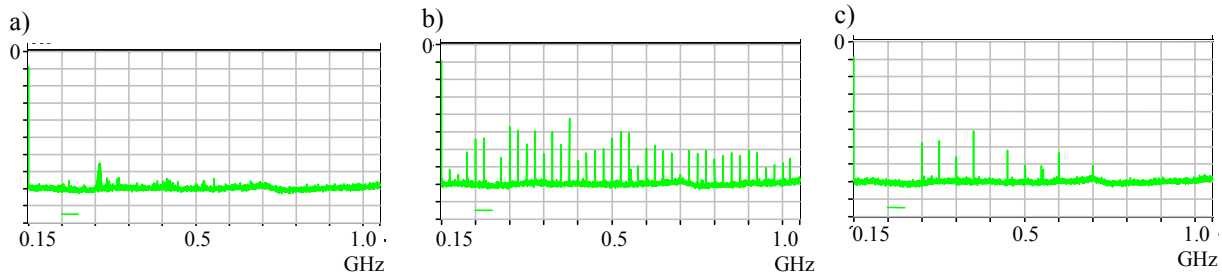


Fig. 4. comb_area circuit - spectrum of HF current in V_{DD} pin for clock frequency: a) 1 MHz, b) 25 MHz, c) 50 MHz; 10 dB/division.

The high frequency currents flowing through the middle zone of the FPGA (package) for both circuit types were measured also as a function of clock frequency. The highest values of harmonic amplitudes and their largest number were observed at about 30 MHz for combinational and at 25 MHz for sequential circuits. The number of high frequency current spectral components which appeared in the middle zone of the FPGA was larger than observed for currents flowing through V_{DD} pin. The main harmonic band for combinational circuits was noticed between 200 MHz and 700 MHz, while for sequential circuit harmonics appeared in narrower band from about 150 MHz to 300 MHz.

Generally, above spectra show that the largest high frequency currents were observed in V_{DD} pins and the smallest one in GND pins for both the sequential and combinational circuits. Since the sum of all currents must be zero it suggests the RF currents must flow out some others pins.

4.1.2. Near-field disturbances

E component of near field was measured over the middle region of FPGA package at clock frequencies up to 50 MHz for both types of the examined circuits. The electric field over the package increased with the clock frequency to 25 MHz and decreased for higher frequencies what generally corresponds with the observations of conducted disturbances. The radiated spectra were similar for both types of the circuits; some of them are shown as an example in Fig. 5 and Fig. 6.

The number of spectrum components and they amplitudes were slightly larger for the combinational circuits. *E* field components for the combinational circuits were grouped inside the band of about 450 MHz wide, while for the sequential circuits of about 350 MHz.

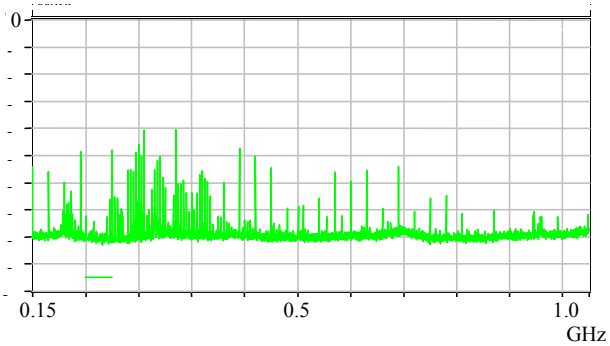


Fig. 5. comb_area circuit spectrum of *E* field over the middle zone of the package for f_C = 25 MHz; 10 dB/division.

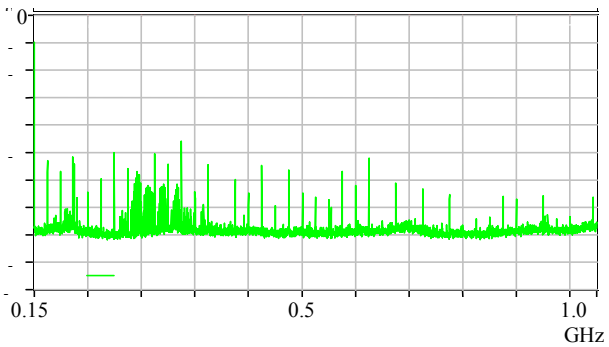


Fig. 6. seq_area circuit spectrum of E field over the middle zone of the package for f_C = 25 MHz; 10 dB/division.

4.2. Disturbances measured in time domain

The change of near field *H* component over the V_{DD} and GND pins and in the middle zone of the integrated circuit package as a function of clock frequency for comb_no_io_speed and seq_area are presented as an example in Fig. 7 and Fig. 8. In the first case fast growth of the H component of the EM field versus the clock rate was observed to approximately to 10 MHz and then above 30 MHz. The maximum value of the *H* field appeared at the clock frequency of about 45 MHz. In the case of comb_no_io_speed circuit the maximum value of *H* over V_{DD} was about 40% greater than the one over the centre of the integrated circuit package. The distinct maximum of the *H* field over the GND pin hadn't been noted. The smaller values of *H* were observed over the centre of the FPGA package - they were about twice smaller than in the case of remaining measuring points.

For the seq_area circuit only certain growth of the *H* field was observed up to the clock frequencies about 5 MHz and again above 30 MHz. The *H* field over the centre of the package reached the greatest value for the clock frequency about 45 MHz. The smallest values of *H* field were obtained over the GND pin and they were about three times smaller than the ones over the centre of the package. For the clock frequencies 5 – 30 MHz the greatest value of

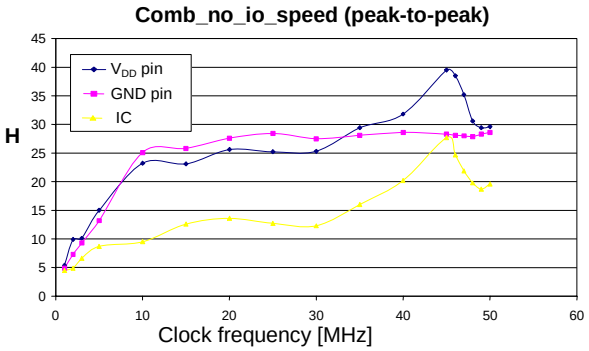


Fig. 7. comb_no_io_speed circuit time domain disturbances as function clock frequency.

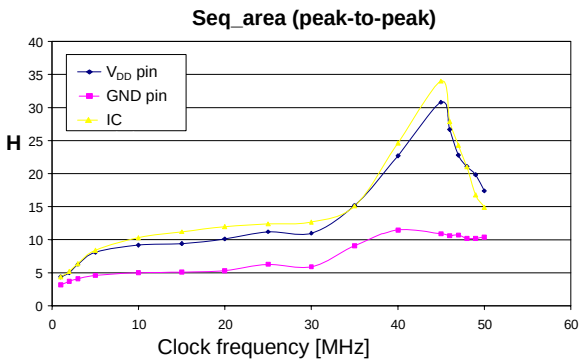


Fig. 8. seq_area circuit time domain disturbances as function clock frequency.

the *H* component were noticed over the centre of the package. It was close to the level of disturbances in the V_{DD} pin and of about 50% higher than in the GND pin. Seq_area circuit produced significantly less disturbances than it was in the case of comb_no_io_speed circuit.

For the remaining combinational and sequential circuits the relations of emissions versus clock frequency were generally different and they depended on the examined circuit. The emissions levels for clock frequencies in the range 5 – 30 MHz were similar but the shape of characteristics was rather different for each case. Maximum of the *H* field appeared at the clock frequency of about 45 MHz for all examined circuits.

It suggests that for this clock frequency, resonances of HF currents flowing through the center of the package and the V_{DD} pin may appear. For currents flowing through the GND pin the resonance hadn't been observed and the characteristics were more or less flat, Fig.7 and Fig.8. The resonance of HF currents in time domain were observed on an oscilloscope as growth of the voltage amplitudes (peak-to-peak), induced in the magnetic probe. These voltages were proportional to the change of *H* field in function of time. Growth of voltage amplitudes was not accompanied by the growth of number of harmonics and their amplitudes within *H* spectrum.

4.3. Power supply currents as a function of clock frequency

Power supply currents as the function of the clock rate were measured for all examined circuits at the V_{DD} terminal (Fig. 9). The values of power supply currents grew up linearly as the function of the clock frequency for all examined circuits. The growth of currents started from 120 mA, and this value was obtained for the clock frequency equal to 0 Hz. It was assumed that 120 mA current was taken by signalling LED diodes and other elements installed on the PCB prepared for testing of FPGA. On the other hand, linearly growing with frequency component of supply current reflects the switching activity of logical gates.

The comb_no_io_speed circuit consumed the greatest supply current among all combinational circuits. The comb_no_io_area circuit consumed a little smaller supply current. These two were the greatest combinational circuits which used 13 448 and 12 552 active logical gates, respectively. Circuits of the smaller number of gates took smaller supply currents.

Similar dependencies of the values of power supply currents on the number of active logical gates were observed in the case of sequential circuits. The greatest values of currents per active logical gate

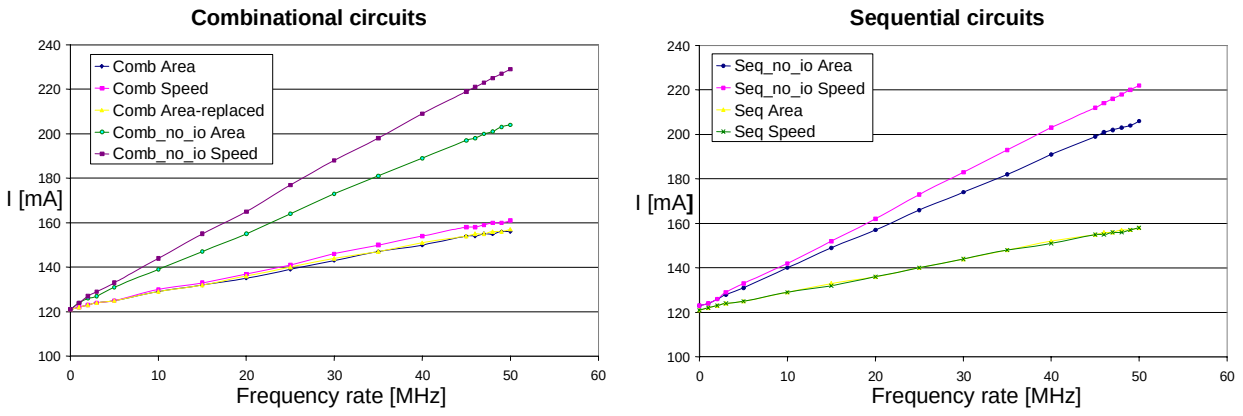


Fig. 9. Power supply currents of combinational and sequential circuits as a function of the clock frequency.

were noticed for seq_no_io_area and seq_no_io_speed circuits, although they contained nearly half of the logical gates used in comb_no_io_area and comb_no_io_speed circuits. The significantly greater values of the current per active logical gate were measured for sequential circuits than for combinational circuits, Table 2.

Table 2. The average value of the power supply current on one logical gate at the clock rate 50 MHz

Circuit	Current/gate [μA]	Number of logical gates	Power supply current [mA]
1	2	3	4
comb_area	3.8	9 453	36
comb_area_replaced	3.9	9 453	37
comb_speed	4.2	9 775	41
comb_no_io_area	6.7	12 552	84
comb_no_io_speed	8.1	13 448	109
seq_area	11.2	3 404	38
seq_speed	11.1	3 423	38
seq_no_io_area	14.2	6 071	86
seq_no_io_speed	14.3	7 145	102

From the above it results that the power supply current grows up along with the number of active logical gates. However, this dependence is not directly proportional, as can be seen from the calculated average values of the current per one active logical gate at 50 MHz, given in column 2 of the Table, as well as from the values of supplying current exceeding 120 mA, given in column 4. The power supply currents were rather related to the manner of the distribution of active gates over the area of FPGA and the multiplication method. It may be supposed that larger number of active logical blocks were simultaneously put into the operation in sequential circuits than in the combinational circuits. For circuits which consumed greater power supply currents the greater level of radiated disturbances were observed. Small amplitude oscillations of power supply currents were appeared for clock frequencies greater than 45 MHz. A little higher amplitudes of the oscillations were measured for circuits consuming smaller supply current than that of greater currents, like comb_no_io_speed and seq_no_io_speed.

5. Discussion

Electronic circuits used for the multiplication of digits with combinational and sequential methods were examined. They were slightly modified and optimized in the process of compilation in respect to the minimization of the number of functional blocks and the speed maximization of the executing multiplication. In this manner, nine different test-circuits were obtained from two basic circuits. They used only small number of logical blocks (1 – 7%) in comparison with the whole number of available blocks in the Xilinx FPGA of Vertex family XCV 800 type. Thanks to this, active gates of the circuits were allocated in FPGA on different manners. The comb_no_io_area and comb_no_io_speed circuits had logical blocks grouped in one place, while the seq_area and seq_speed circuits were scattered over a half of the FPGA area (see Fig. 3). Remaining circuits had one part of logical gates grouped in one place and the other part scattered on the FPGA area. A consequence of differences in the configuration of logical blocks was the difference in the length of the power supply and the ground lines. For circuits with grouped logical blocks the length of connections was relatively smaller than for circuits of scattered logical blocks. For that reason, inductances of the power supply L_{Vdd} and the ground L_{Vss} lines as it is seen in Fig. 10, should be greater for circuits of scattered than of grouped logical blocks.

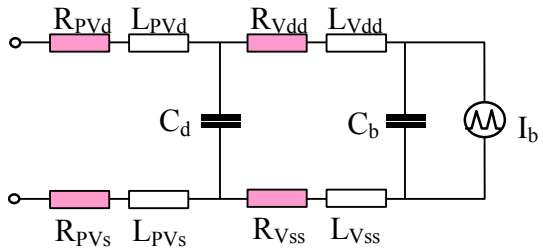


Fig. 10. FPGA power supply schematic circuit. R_{PVdd}, L_{PVdd} – resistance and inductance of external power supply line, R_{PVss}, L_{PVss} – resistance and inductance of external ground line, R_{Vdd}, L_{Vdd} – resistance and inductance of power supply line on IC chip, R_{Vss}, L_{Vss} – resistance and inductance of ground line on IC chip, C_d – capacity between external power supply lines, C_b – capacity between power supply lines on IC chip, I_b – HF current generator.

One could assume that the circuits with greater inductances of inherent connections should generate stronger EM disturbances and exhibit resonances at different frequencies than the other circuits. But it seems that the on-chip inductance was small relative to the inductance of the package, which then determined the measured emissions.

The highest level of the disturbances was obtained for comb_no_io_area, comb_no_io_speed and seq_no_io_speed circuits. They consumed the greatest power supply currents as the function of the clock frequency (Table 2 and Fig. 9). The smallest values of the power supply currents were taken by comb_area and seq_area circuits, which generated also the smallest disturbances. From here a conclusion can be drawn that the level of the emitted (generated) disturbances was proportional to the power supply current.

However, we did not notice the simple relationship between the number of active gates and the values of the power supply current. From Table 2 it results that circuits of the comparable power supply currents as e.g. seq_area and comb_area clearly differ

with the number of used logical gates and the average values of the power supply current per one active logical gate (Table 2, col. 2.) Generally, combinational circuits consumed smaller medium value of supply current per logical gate than it happened for sequential circuits, likely for reason of specific properties of the combinational multiplication algorithm (less number of signal lines).

Circuits having the grouped logical blocks (Fig. 3d–e) and of the greatest power supply currents, generated the greatest disturbances measured in the near field as its and *H* components. However the inductances of their inherent power supply and ground connections were the smallest from all of examined circuits since the shortest connections. Only the circuit seq_no_io_speed generated large disturbances although it included a medium number of logical blocks and only part of them was grouped in one place of FPGA (Fig. 3i). Circuits of scattered logical blocks, which had the relatively greater values of the connection inductances, generated smallest disturbances. Remaining circuits of partly scattered and grouped logical blocks generated disturbances of the medium intensity.

The measurements of investigated circuits showed then, that the inductance of inherent connections had weaker influence on the disturbance levels than it was suggested in work [4]. In our case the influence of strongly coupled internal current loops and possible crosstalk between connection lines as well as the external pins (package) inductance were rather dominated.

6. Conclusion

The performed experiments allow formulate following conclusions regarding the EM emission level of the investigated circuits:

- both conducted and radiated disturbances generated by combinational and sequential multiplicators had similar levels with a little favor of sequential circuit;
- the difference in EM emission levels were mainly related to the specific circuit design – the lowest emission was noted e.g. for seq_area, seq_speed and comb_area circuits while the highest for the circuits marked as no_io in which standard RS 232 interface implemented in FPGA was replaced by logical blocks inside the circuit (provided for transmission and storage data);
- the floorplan was of great importance for the emission level – lower levels were always associated with the scattered arrangement of the used logical blocks
- the values of supplying currents were significantly larger for the circuits which generated stronger disturbances;
- at a certain clock frequency (about 45 MHz) same resonances appeared which manifested themselves as the maxima of RF currents (Fig. 7 and Fig. 8) observed in V_{DD} pins and inside the circuit as well as which caused small fluctuations in supplying currents (Fig. 9 and Fig. 10);
- generated disturbances occupied some frequency bands inside the whole considered frequency range up to 1 GHz.

REFERENCES

1. O. WADA ET AL., *Power Current Model of Digital IC with Internal Impedance for Power Decoupling Simulation*, 4th Europ. Symp. on Electromagnetic Compatibility, Brugge Sept. 11–15, 2000, 315–320.
2. J. F. KOŁODZIEJSKI, J. SZCZĘSNY, *Electromagnetic Emissions of Integrated Circuits and PCBs*, IEEE EMC Newsletter, Spring Issue 2004, 34–39.
3. S. GONG ET AL., *Packaging Impact on Switching Noise in High-Speed Digital Systems*, IEE Proc.-Circuits Devices Syst., 1998, **145**, 6, 446–452.
4. X. DONG, S. DENG, D. BEETNER, T. HUBING, *The Influence of IC Power Bus Design and Floor Planning on High-Frequency Package Current*, sent to IEEE Trans. EMC.
5. J. SZCZĘSNY, J. F. KOŁODZIEJSKI, D. OBRĘBSKI, *Electromagnetic Emissions of Digital Circuits Implemented in Xilinx FPGAs* 4025E and XCV 800. Electron Technol. Internet J. 2004, **36**, 2, 1–6.
6. DataSource CD-ROM rev. 8 Q1-2003.
7. The Programmable Logic Data Book 1999, Xilinx Inc., 1999.