ARCHIVES OF ACOUSTICS
36, 4, 831–849 (2011)

DOI: 10.2478/v10168-011-0055-3

Sampling Jitter in Audio A/D Converters

Zbigniew KULKA

Warsaw University of Technology
Institute of Radioelectronics, Electroacoustics Division
Nowowiejska 15/19, 00-665 Warszawa, Poland
e-mail: z.kulka@ire.pw.edu.pl

(*received June 20, 2011; accepted September 30, 2011*)

This paper provides an overview of the effects of timing jitter in audio sampling analog-to-digital converters (ADCs), i.e. PCM (conventional or Nyquist sampling) ADCs and sigma-delta ($\Sigma\Delta$) ADCs. Jitter in a digital audio is often defined as short-term fluctuations of the sampling instants of a digital signal from their ideal positions in time. The influence of the jitter increases particularly with the improvements in both resolution and sampling rate of today's audio ADCs. At higher frequencies of the input signals the sampling jitter becomes a dominant factor in limiting the ADCs performance in terms of signal-to-noise ratio (SNR) and dynamic range (DR).

Keywords: analog-to-digital converter (ADC), successive approximation register (SAR) ADC, sigma-delta ($\Sigma\Delta$) ADC, sample-and-hold circuit, DT $\Sigma\Delta$ modulator, CT $\Sigma\Delta$ modulator, time jitter, aperture jitter, clock jitter, periodic clock jitter, signal-to-noise ratio (SNR).

1. Introduction

Jitter can affect a digital audio signal mainly in the sampling process and in the digital interface, though it may play a certain role in the storage media and during the processing of this signal. Therefore it is usually classified in digital audio as a sampling jitter and as an interface jitter (this is a rather technical classification). Another, more general, classification of jitter distinguishes two types of jitter: the random jitter and deterministic jitter. Random jitter is caused by factors like thermal noise, thermal vibrations of semiconductor crystal structure and cannot be predicted on a cycle-by-cycle basis. It is not bounded, therefore, a Gaussian distribution best describes random jitter. Random jitter is characterized by its standard deviation (rms) value. Deterministic jitter is created by identifiable interference signals. For example, it is caused by external sources such as power supply noise. It is always bounded in amplitude and

with specific causes, and the bounds can easily be observed and predicted. Deterministic jitter is characterized by its bounded, peak-to-peak, value. Periodic jitter, data-dependent jitter, and duty-cycle dependent jitter are all the types of deterministic jitter.

The term "sampling jitter" indicates the errors in the timing of the sampling processes of an analog-to-digital conversion, a digital-to-analog conversion or a sampling rate conversion. Sampling jitter is always present, but its larger amounts may cause an audible degradation to the audio signal. Sampling jitter is most critical in analog-to-digital converters (ADCs), but there are some differences depending on what type of the converter is taken into consideration. There are two main classes of high-resolution audio ADCs such as successive approximation register (SAR) ADCs, also called conventional or PCM ADCs, and sigma-delta ($\Sigma\Delta$) ADCs, also known as delta-sigma ($\Delta\Sigma$) ADCs (Kulka, 2006).

The mode of operation of the conventional 16- or 18-bits audio SAR ADCs is based on the linear pulse-code modulation (LPCM). In recent designs, the topology of SAR ADCs uses a capacitive redistribution design approach instead of its predecessor architecture, the R-2R ladder with switching current sources topology. The SAR ADC converts a continuous-time signal at its input into a discrete-time signal under the control of an external clock. More precisely, it converts a signal voltage amplitude into a binary code representing a quantized amplitude value, which is the closest to the amplitude of the input. However, the conversion is not instantaneous, and for this reason, a high-performance audio ADC typically includes a sample-and-hold circuit. The block diagram of the conventional (PCM), sampling ADC is shown in Fig. 1.

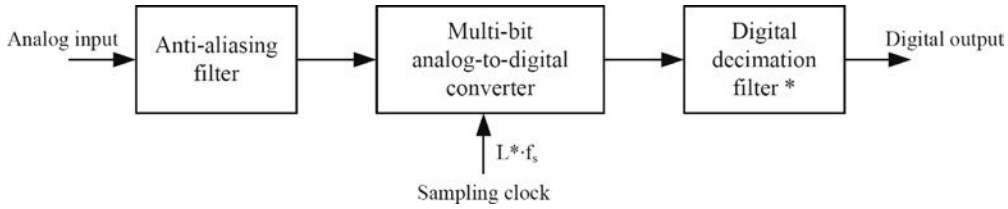


Fig. 1. Block diagram of the conventional ADC (L^* – oversampling ratio, * optional mode).

Today, almost all audio sampled data systems use the so-called sampling ADCs which contain an integral sample-and-hold circuit (without feedback) for uniform sampling, working in sample-and-hold mode or in track-and-hold mode. An external clock is then named as a sampling clock. Modern audio SAR ADCs use an oversampling. This technique with an oversampling ratio L, which is typically 2-, 4- or 8-times higher than the Nyquist rate, gives known benefits related to simplification of an analog anti-aliasing filter before ADC and converter's noise floor reduction.

The acquisition time for the SAR ADC is the time required for the sampling mechanism to capture the input voltage. This time begins after the sample command is given where the hold capacitor charges. Note that a SAR converter with a multibit quantizer samples the input signal once for each conversion.

The mode of operation of the linear 16- to 24-bit audio ΣΔ ADCs are based on sigma-delta modulation (SDM) which is performed by the analog ΣΔ modulators. The basic components of a ΣΔ modulator include a loop filter (even up to 7th order) in the forward loop followed by a low-bit (usually 3 to 6 bits) quantizer, and a low-bit digital-to-analog converter (DAC) in the negative feedback loop. The order of the modulator is equivalent to the number of integrators creating the loop filter. The output of the quantizer feeds forward to a digital decimation filter and back to a DAC. The signal at the inverted output of the DAC is summed with the input signal. The low-bit quantizer has a form of the K-bit flash ADC, i.e. with the K-bit resolution has 2^K-1 voltage comparators connected in parallel with reference voltages set by a resistor-divider network. In practice, there is a set of latched comparators driven by a sampling clock signal. The block diagram of the ΣΔ ADC is shown in Fig. 2.

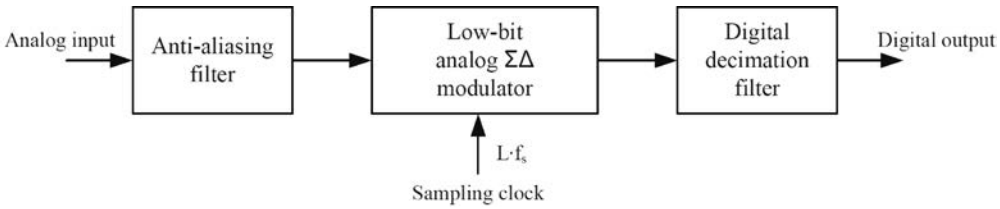


Fig. 2. Block diagram of the ΣΔ ADC (L – oversampling ratio).

The ΣΔ ADC is inherently an oversampling converter and the sampling rate is much higher than the Nyquist frequency, typically 32-, 64-, or 128-times. By using the oversampling operation in conjunction with quantization noise shaping, digital filtering and decimation, it is possible to shape the frequency spectrum of the quantization noise so that the majority of the noise lies above the audio baseband (the band of interest) and only a small portion is left in the baseband. After the noise spectrum is shaped by the ΣΔ modulator, the digital decimation filter can then remove the bulk of the quantization noise energy, and the dynamic range is increased. Such a filter is also used for the reduction of data rate at the ADC output. With contemporary CMOS technology, the integrated ΣΔ ADCs with on-chip digital filters can be built for audio applications.

Note that in the ΣΔ ADCs the separate sample-and-hold circuits are not needed because of the inherent ability of the analog ΣΔ modulators to sampling and tracking the input signal. However, contrary to the SAR ADC, the ΣΔ ADC averages multiple samples for each conversion result. The sampling rate is typically much higher than the output data rate. In other words, the ΣΔ ADC

does not output a code corresponding to a single point. The code that ΣΔ ADCs output is the result of filtering or averaging the input during an interval of time which is equal to the sample period. The averaging performed by the converter usually occurs in the form of a finite impulse response (FIR) digital decimation filter. Consequently, the acquisition time is longer than that with a SAR ADC.

This paper is structured as follows. The components of sampling jitter and corresponding to them the voltage errors as well as their degrading effect on a SNR in conventional (PCM) ADCs are described in Sec. 2. The effect of a random clock jitter on the continuous-time (CT) ΣΔ modulators, in particularly the influence of the clock jitter on the SNR degradation of the CT ΣΔ ADCs is presented in Sec. 3. In Sec. 4 the effect of periodic clock jitter on the generation of the nonlinear distortion in the audio signal is considered.

2. Jitter effects in PCM ADCs

2.1. Aperture time and aperture error

The sample-and-hold amplifier (SHA), usually working in track-and-hold mode, refers to the input sampling circuitry which is integrated with a SAR ADC. A simplified model of the SHA is shown in Fig. 3. It contains an input buffer amplifier, an analog switch (which represents JFET or MOSFET), a hold capacitor, an output buffer amplifier and a switch driver. The circuit is in "track" state when the switch is closed, when the switch is opened the circuit is in "hold" state.

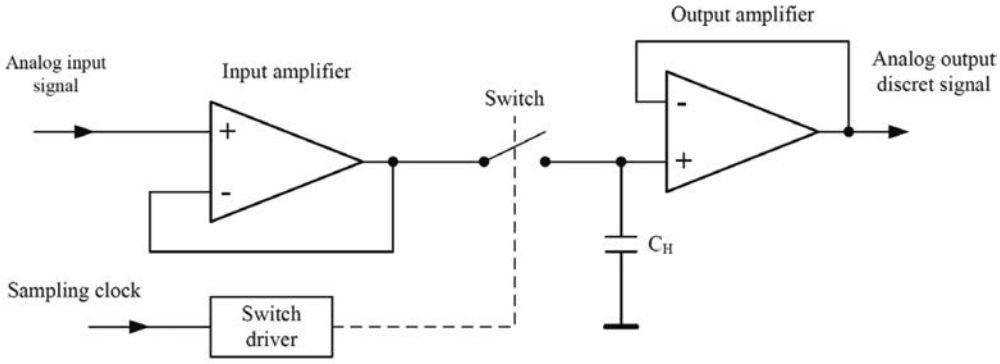


Fig. 3. Simplified model of sample-and-hold amplifier.

When the hold command is applied, the SHA should disconnect instantaneously the hold capacitor from the input buffer amplifier. However, a short time interval is required for this action which is called the aperture time, t_{ap}. The actual value of the voltage that is held at the end of this interval is a function of both the input signal slew rate and the errors introduced by the switching

operation itself. The value that is finally held is a delayed version of the input signal, averaged over the aperture time of the switch. The finite time required for the switch to open (t_{ap}) has two components (Fig. 4).

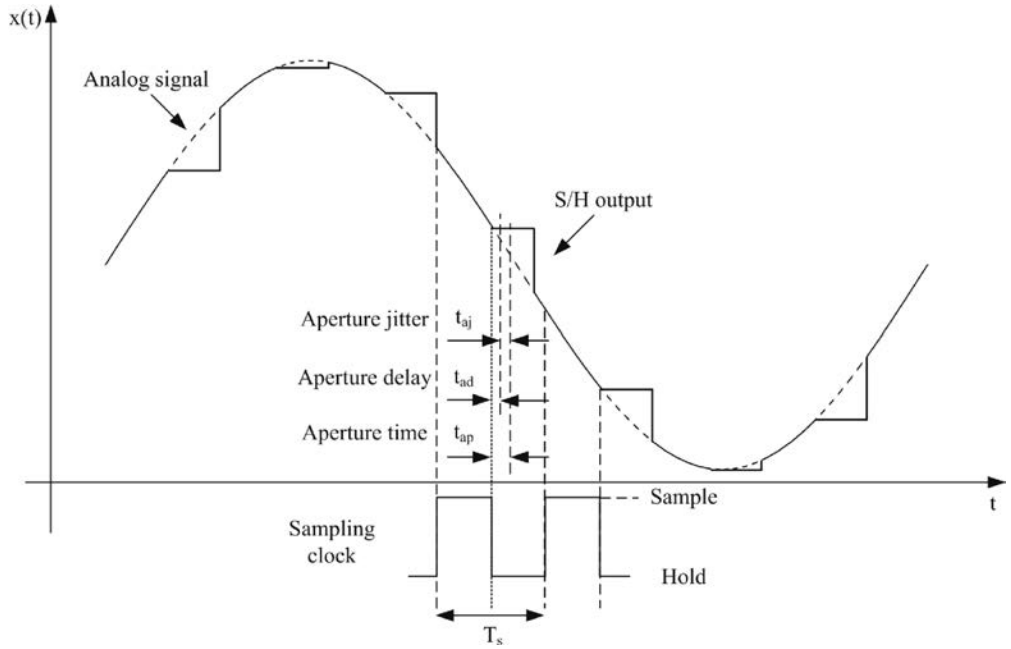


Fig. 4. Relationship of the aperture delay, aperture jitter and aperture time.

The first component is called the aperture delay time or aperture delay, t_{ad}. The aperture delay is constant, and can be measured (KESTER, 2008). It has a positive (usually) or negative value depending on the propagation delay through the input buffer, the delay through the switch driver and the aperture time (the value of $t_{ap}/2$ is taken for calculation). Aperture delay produces no voltage errors (assuming it is relatively short with respect to the hold time), but acts as a fixed delay in either the sampling clock input or the analog input (depending on its sign).

The second component is called aperture uncertainty or aperture jitter (these terms are synonymous), t_{aj}, and is usually measured in rms (root-mean-square) picoseconds. Aperture jitter is caused by sample to sample variation in the aperture delay. This in turn results in an aperture voltage error ε_{aj}, i.e. the effective noise voltage due to the aperture jitter, as shown in Fig. 5.

The value of the aperture error ε_{aj} depends on the value of the aperture jitter t_{aj} and the rate-of-change of the analog input. The error ε_{aj} increases as the frequency f of the input signal $x(t)$ (i.e. slew rate $\mathrm{d}x/\mathrm{d}t$) increases. Typical aperture jitter values are much smaller than those of aperture delay, for example $t_{aj} \approx 5 \div 50$ ps, $t_{ad} \approx 2 \div 10$ ns.

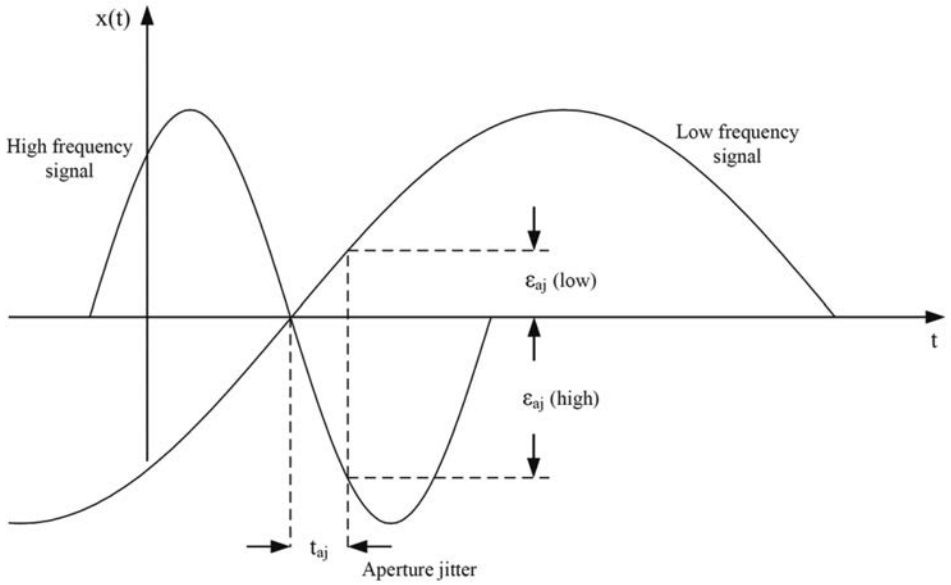


Fig. 5. Voltage error ε_{aj} due to aperture jitter t_{aj}.

From the above discussion it should be clear that the aperture time is not constant but it is changing from sample to sample. The actual value of the input signal that is held and the A/D conversion result of this held voltage depends rather on the averaged value of the input signal voltage over the aperture time than on the instant when the sample of input signal is taken.

2.2. Total sampling jitter and total voltage error

The voltage error ε_{aj} is caused by the aperture jitter t_{aj} even when the sampling clock waveform fed to the sampling ADC is ideal, i.e. it has not sampling clock jitter. However, the sampling clock jitter (fluctuations of sampling period), t_{sj}, is always present in the sampling clock waveform. It is the result of the oscillator phase noise (i.e. oscillator used for sampling clock generation; phase noise in the frequency domain can be converted into jitter in the time domain) and the noise and other disturbances, which are superimposed on the sampling clock signal when it is fed to the sample-hold circuit. The voltage error ε_{sj} corresponding to the sampling clock jitter t_{sj} is the same kind of error as the voltage error ε_{aj}. In a sampling ADC there is a third contributor of jitter, which is the analog input signal jitter, t_{ij}, and its corresponding voltage error ε_{ij}.

Shinagawa, Akazawa and Wakimoto (1990) have proposed a jitter estimation model for a practical sampling system which is shown in Fig. 6. The model consists of three separate total sampling jitter components: the aperture jitter t_{aj}, sampling clock jitter t_{sj}, and the analog input signal jitter t_{ij}. The

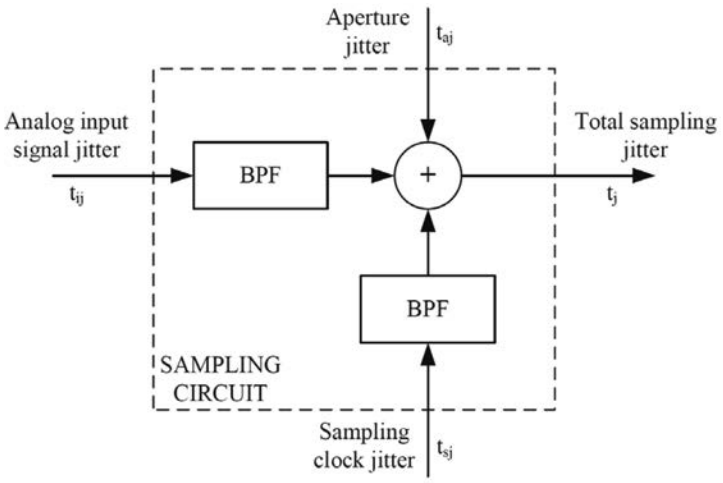


Fig. 6. The total sampling jitter estimation model.

total sampling jitter is given by the sum of these three components. They assumed that two bandpass filters should be used which represent the bandwidth limitation restrictions. These filters are inherent in the sampling circuit and are thus constant and different from each other.

Each jitter component can be assumed to be independent of each other (Shinagawa *et al.*, 1990; Srinivasan *et al.*, 2002) and so the total sampling jitter t_j (total ADC sampling jitter) can be expressed by

$$t_j = \sqrt{t_{aj}^2 + t_{sj}^2 + t_{ij}^2}, \tag{1}$$

where t_{aj} – rms aperture jitter, t_{sj} – rms sampling clock jitter, t_{ij} – rms analog input signal jitter.

The total sampling jitter t_j, similarly to an effective number of bits and a quantization noise, affects the overall precision of the analog-to-digital conversion. As the frequency of the ADC's input signal increases, the effect of jitter t_j becomes more severe. The total voltage error ε_j which arises due to the total sampling jitter t_j when sample-and-hold circuit goes from track state to the hold state, can be specified by summing the three voltage errors ε_{aj}, ε_{sj}, and ε_{ij}, which correspond to the t_{aj}, t_{sj}, and t_{ij}, as

$$\varepsilon_j = \varepsilon_{aj} + \varepsilon_{sj} + \varepsilon_{ij}. \tag{2}$$

The total sampling jitter results in the voltage error proportional to the input signal slope. The effect of the total voltage error ε_j sets a limitation on the maximum frequency of the input sine wave because it defines the maximum slew rate of the signal. Assume an input signal as a sinewave signal

$$x(t) = X_m \sin 2\pi f t. \tag{3}$$

The maximum slew rate occurs at the zero crossing point and can be calculated as

$$\frac{\mathrm{d}x(t)}{\mathrm{d}t} = X_m 2\pi f \cos(2\pi f t), \tag{4}$$

$$\left(\frac{\mathrm{d}x}{\mathrm{d}t}\right)_{\max} = 2\pi f X_m. \tag{5}$$

If the error ε_j does not affect the accuracy of the ADC, it must be less than 1/2 LSB at the point of maximum slew rate. For an N-bit converter therefore

$$\varepsilon_j = t_j \frac{\mathrm{d}x}{\mathrm{d}t} = \frac{1}{2}\,\mathrm{LSB} = \frac{2X_m}{2^{N+1}}, \tag{6}$$

where ε_j is the rms total voltage error for the rms total sampling jitter t_j.

Substituting (5) into (6) gives

$$\frac{2X_m}{2^{N+1}} = 2\pi f X_m t_j. \tag{7}$$

So the maximum frequency is given by

$$f_{\max} = \frac{1}{t_j \pi 2^{N+1}}. \tag{8}$$

For example, using the typical 16-bit ADC with a total sampling jitter of 50 ps, the maximum input signal frequency is $f_{\max} = 48.6$ kHz. This means that the typical total sampling jitter t_j of such ADC only becomes a significant factor when the input signals to it exceed 48.6 kHz and/or the converter resolution greater than 16 bits is desired. In contrary, so to say, for a 20-bit system with a full-scale 20 kHz sinewave and the maximum amplitude error ε_j restricted to 1 LSB, the timing error t_j cannot be more than 3.98 ps rms.

2.3. ADC SNR degradation caused by total sampling jitter

The effect of total sampling jitter on a signal-to-noise ratio (SNR) of the ideal conventional (PCM) ADC can be estimated by the following simple analysis. The noise produced by total sampling jitter is usually modeled as white noise. As before (Eq. (3)), assuming a full-scale sinusoidal input signal $x(t)$ and a Gaussian distribution of the timing jitter, as well as substituting the rms values of total voltage error ε_j and total sampling jitter t_j, the rms value of the input $\mathrm{d}x/\mathrm{d}t$ is given by

$$\left(\frac{\mathrm{d}x}{\mathrm{d}t}\right)_{\mathrm{rms}} = \frac{2\pi f X_m}{\sqrt{2}} = \frac{\varepsilon_j}{t_j}. \tag{9}$$

Solving Eq. (9) for ε_j

$$\varepsilon_j = t_j \frac{2\pi f X_m}{\sqrt{2}}. \tag{10}$$

The rms value of the full-scale input sinewave is $\frac{X_m}{\sqrt{2}}$, therefore the rms signal to rms noise ratio expressed in dB is given by

$$\begin{aligned}\mathrm{SNR}_{t_j(\mathrm{PCM})}\,[\mathrm{dB}] &= 20\log_{10}\left(\frac{X_m/\sqrt{2}}{\varepsilon_j}\right)\\ &= 20\log_{10}\left(\frac{1}{2\pi f t_j}\right) = -20\log_{10}\left(2\pi f t_j\right)\end{aligned} \tag{11}$$

and using oversampling is given by

$$\mathrm{SNR}_{t_j(\mathrm{PCM})}\,[\mathrm{dB}] = -20\log_{10}(2\pi f t_j) + 10\log_{10}(L). \tag{12}$$

The above equations assume an infinite resolution of an ADC where total rms sampling jitter, including aperture jitter and other components, is the only factor in determining the theoretical ADC's SNR. However, there are several factors that limit the SNR of the ADC, such as quantization noise, thermal noise (which limits the SNR at low input frequencies), total sampling jitter, differential nonlinearity and finite resolution. Taking first three factors into consideration, the generalized equation is given below

$$\mathrm{SNR}_{(\mathrm{PCM})}\,[\mathrm{dB}] = -20\log_{10}\sqrt{10^{-\mathrm{SNR}_{qn}/10} + 10^{-\mathrm{SNR}_{tn}/10} + 10^{-\mathrm{SNR}_{t_j}/10}}, \tag{13}$$

where SNR_{qn} – SNR of the ADC degraded only by the quantization noise, SNR_{tn} – SNR of the ADC degraded only by thermal noise, SNR_{t_j} – SNR of the ADC degraded only by total sampling jitter.

This generalized Eq. (13) provides a considerable insight into the noise performance of a conventional ADC.

2.4. Methods for estimating different components of the total sampling jitter

In the last years, the several methods of measuring or estimating basic components of the total sampling jitter were described by different authors. For example, Walden (1999) discovered the aperture jitter as the dominating error effect that limits the achievable ADC SNR. Shinagawa *et al.* (1990) proposed a precision jitter measurement method based on sampled sinewave SNR calculations, Srinivasan *et al.* (2002) described a direct estimating method of the timing jitter present in the sampling clock and the analog input signal by analyzing their phase noise plots, Chiorboli *et al.* (1997) proposed an original procedure for measuring aperture uncertainty, which substantially improves the classical statistical analysis by completely removing the limitations due to quantization noise and ADC nonlinearity, and Kobayashi *et al.* (1999) presented a formula which allows to calculate the SNR in the presence of an aperture jitter. Moreover, the effect of the clock jitter was investigated by Awad (1998).

However, Brannon and Barlow (2006) described a relatively simple method of estimation the aperture jitter of the ADC using the FFT techniques. It can be

estimated by analyzing the degradation of the ADC SNR (without harmonics) as a function of an analog input signal frequency. For a given timing jitter, the SNR degrades with an increase of the signal frequency. Hence a low frequency SNR measurement is made and neglecting the effect of jitter and solving Eq. (13), the total contribution due to thermal and differential nonlinearity noise can be estimated. Once these are known, Eq. (13) can be solved to estimate the aperture jitter component of the total sampling jitter (t_j) for any high frequency analog input signal. This analysis assumes that the DNL noise is independent of the analog input signal frequency.

The modified version the Brannon and Barlow method of determining an ADC aperture jitter that includes the jitter of the sampling clock generator using the FFT technique was proposed by Kester (2008). The block diagram of the aperture jitter measuring setup is shown in Fig. 7.

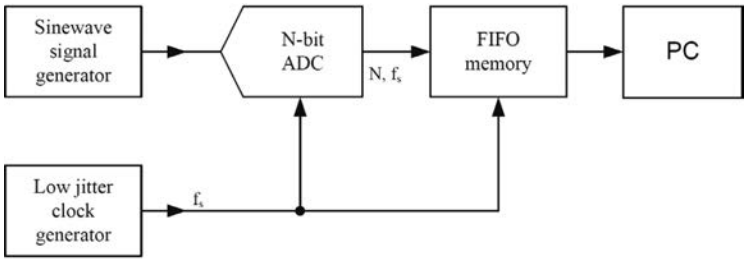


Fig. 7. Aperture jitter measurement setup.

The input sinewave signal generator should be selected with an rms analog input signal jitter (t_{ij}) specification which is several times less than the specified aperture jitter (t_{aj}) of the ADC under test and the sampling clock jitter (t_{sj}). In such a case, the jitter component t_{ij} (Eq. (1)) can be omitted. The sampling rate is generally set for the maximum allowable.

Two SNR measurements are required for the aperture jitter (includes low jitter of the sampling clock generator) calculation. Both utilize a full-scale input sinewave having a low, f_L, and high, f_H, frequency. The first measurement of SNR_L is done at a relatively low frequency, f_L, where the noise is primarily the combination of the ADC input-referred noise and the quantization noise (the effect of aperture jitter is negligible). The second measurement of SNR_H is made using a high frequency input, f_H, where the effects of aperture jitter on the ADC SNR are noticeable. The high frequency should be as high as possible, and usually is chosen as a half of the sampling rate.

According to Eq. (11), the relationship between the SNR due to aperture jitter alone is given as follows:

$$\mathrm{SNR}_A\,[\mathrm{dB}] = 20\log_{10}\left(\frac{1}{2\pi f_H t_{aj}}\right), \tag{14}$$

where SNR_A is the SNR [dB] due to aperture jitter, and f_H is the input frequency.

Solving Eq. (16) for t_{aj} gives

$$t_{aj} = \frac{1}{2\pi f_H} \cdot \frac{1}{10^{\mathrm{SNR}_A/20}}. \tag{15}$$

Next, basing on SNR_L and SNR_H, the SNR_A can be calculated as

$$\frac{1}{10^{\mathrm{SNR}_A/10}} = \frac{1}{10^{\mathrm{SNR}_H/10}} - \frac{1}{10^{\mathrm{SNR}_L/10}}. \tag{16}$$

Substituting Eq. (16) into Eq. (15) yields the following t_{aj} formula

$$t_{aj} = \frac{1}{2\pi f_H} \cdot \sqrt{\frac{1}{10^{\mathrm{SNR}_H/10}} - \frac{1}{10^{\mathrm{SNR}_L/10}}}. \tag{17}$$

Note, that harmonics from the 2nd to 6th as well as the dc components must be removed when making the SNR calculation from the FFT output because this is necessary to get an accurate measure of aperture jitter. Note also, that measuring a rms aperture jitter less than 10 ps is practically very difficult because of the unwanted jitter which may occur on the input signal or the ADC sampling clock, or because of the layout-induced jitter and noise (Kester, 2008).

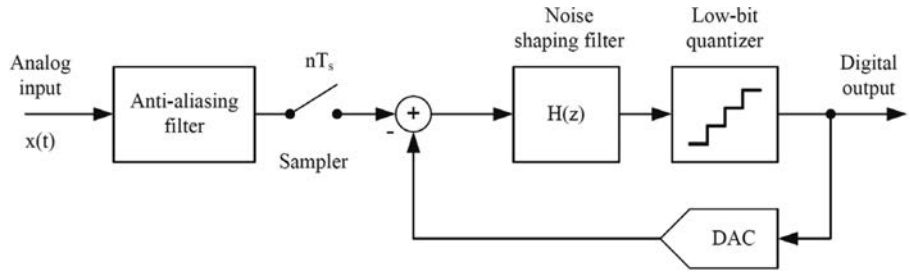
3. Jitter effects in ΣΔ ADCs

3.1. Architectures of ΣΔ modulators

The analog ΣΔ modulators loops of the ΣΔ audio ADCs include noise-shaping filters (loop filters) which are built as discrete-time (DT) or as continuous-time (CT) circuits. The conceptual block diagrams of the single-loop DT and CT ΣΔ modulators are shown in Fig. 8.

The DT ΣΔ modulators are implemented using the switched-capacitor (SC) circuit techniques. The DT (SC) ΣΔ modulators show little sensitivity to clock jitter because the SC noise shaping filters deal with sampled signals (Yang *et al.*, 2007; Chopp, Hamouni, 2009). However, the CT ΣΔ modulators benefit from a number of architectural advantages over their DT counterparts. These include a greater potential for low-power and high-speed operation and an inherent suppression of aliasing and sampling errors (Chopp, Hamouni, 2009). Usually, CT modulators are preferred in comparison of the DT ones, whatever the application. The principal disadvantage of CT ΣΔ modulators is their high sensitivity to clock jitter. The latter can seriously degrade the SNR performances. Generally, increasing the clock frequency higher makes the clock jitter worse. The clock jitter introduces errors into both the forward path (as sampling errors at the quantizer input) and the feedback path (as time-delay errors in the DAC feedback pulses). Sampling errors are subject to the same modulator noise shaping effect as quantization errors, therefore they are insignificant to the overall performance of the ΣΔ ADC. On the contrary, DAC time-delay errors are not

a)



b)

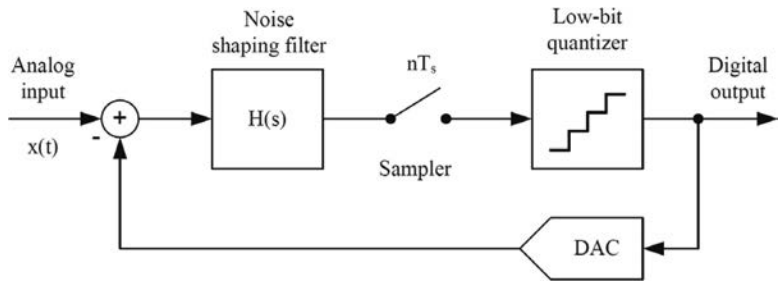


Fig. 8. Simplified block diagrams of the single-loop ΣΔ modulators: DT (a) and CT (b).

suppressed by the ΣΔ loop-filter gain. The jitter error introduced in the DAC is directly added to the input signal, thus it increases the in-band noise power and degrades the modulator performance. Furthermore, the DAC in the feedback path of the CT modulator can also exhibit pulse shapes such as return-to-zero (RZ) or non-return-to-zero (NRZ), depending on the length of the pulse.

The clock jitter in CT ΣΔ modulators has been the object of several studies reported in literature, for example (Shamsi, 2008; Ahmed, Baghel, 2010; Zwan, Dijkmans, 1996; Veldhoven, 2003; Ashry, Aboushady, 2009; Chopp, Hamouni, 2009; Kobayashi *et al.*, 2007; Tortosa *et al.*, 2005; Raikwar, Trivedi, 2009; Strak *et al.*, 2004). Most of them describe ΣΔ modulator architectures with an internal single-bit quantizer and a RZ DAC, others with an internal low-bit quantizer. The combination of 3rd – 4th filter order, single-loop architectures with low-bit (3–6 bit) quantization allows to reduce the oversampling ratio. In addition, low-bit quantization can reduce the sensitivity of CT ΣΔ modulators to clock jitter if the NRZ feedback waveform is used in the DAC.

As shown in Fig. 8, the sampling operation in the CT ΣΔ modulator is realized before quantization instead of the modulator input as done in the case of the DT ΣΔ modulator. So, there are two clocked building blocks which are the cause of a jitter error, i.e. the sampler and the DAC. The error introduced through the sampling operation is reduced by the loop gain and shaped in the same way as the quantization noise. Hence, its effect can be neglected. On the contrary, the jitter error associated to the DAC directly adds to the input signal increasing the in-band noise power. This can limit the modulator SNR performance.

3.2. SNR degradation of CT ΣΔ modulators due to clock jitter

As mentioned above, a major concern in CT ΣΔ modulators is the degradation of the SNR due to clock jitter (also called clock phase noise). Clock jitter is usually defined as a time-fluctuation of the clock transitions with respect to the ideal clock and it can be assumed that it has a Gaussian distribution with a standard deviation σ_j. This approximation results in a clock jitter with a white power spectrum. The clock jitter can be modeled as an additive noise in the feedback path as shown in Fig. 9a. The added jitter noise is defined as the instantaneous difference between the jittered DAC output and the ideal DAC pulse.

DT ΣΔ modulators are relatively insensitive to clock jitter since they utilize SC circuits. The insensitivity is due to the sloping pulse form of the feedback. Since most of the charge transfer in a SC circuit occurs at the beginning of the clock period, clock jitter introduces a minimal amount of error in the charge lost (Fig. 9b). The capacitor is discharged over a switch with very low on-resistance, thus reducing the value of time constant $\tau = \mathrm{RC}$ and causing a fairly steep slope as the DAC discharges. In contrast, CT ΣΔ modulators transfer charge at a constant rate over the clock period (ideally) with RZ-type feedback pulse (Fig. 9c), and thus the charge loss due to a timing error is much greater than for the DT ΣΔ modulator. As can be seen, the clock jitter is translated into a charge error proportional to the shaded areas.

To reduce the degradation of the SNR due to clock jitter, the feedback DAC of the CT ΣΔ modulator can be implemented as a SC feedback circuit. The feedback current in the SC DAC is shown in Fig. 9b. In the SC case, the variation of the amount of charge that is transferred per clock cycle due to the variation in timing (clock jitter) is relatively low. The error charge due to clock jitter depends on the settling-time constant τ of the DAC. It can be assumed that $\sigma_j \ll T_s$, where σ_j is a standard deviation of the clock jitter. As mentioned above, $\tau = \mathrm{RC}$, and R is determined by switch resistance and the equivalent input impedance of the integrator stage.

The degradation of the SNR due to clock jitter was calculated by Zwan and Dijkmans (1996). If the clock jitter causes timing errors t_{sj} with variance σ_j^2 and the DAC output current levels are $\pm I_{\mathrm{DAC}}$, the variance σ_q^2 of the error charge transferred per clock cycle T_s can be calculated by

$$\sigma_q^2 = \sigma_j^2 \cdot I_{\mathrm{DAC}}^2. \tag{18}$$

The maximum signal amplitude at the input of the modulator is -3 dB compared to the DAC current levels, so the maximum variance of the signal charge is

$$\sigma_{\mathrm{signal}}^2 = \frac{I_{\mathrm{DAC}}^2}{4} T_s^2. \tag{19}$$

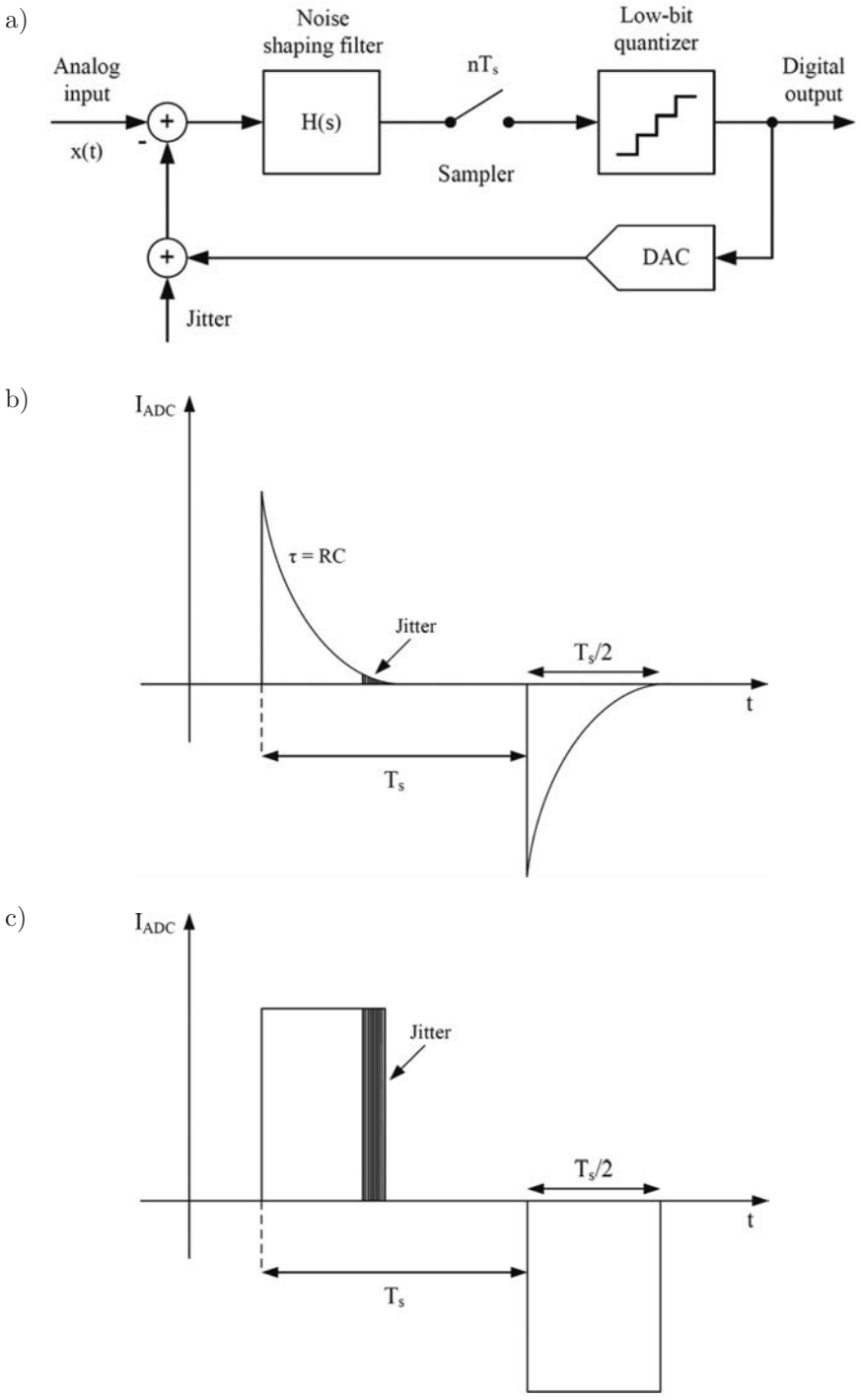


Fig. 9. Modeling of the clock jitter effect as an additive noise (a), clock jitter in DT modulator (b), clock jitter in CT modulator (c).

Assuming that the noise power that is introduced by the time jitter is white, the maximum achievable $\mathrm{SNR}_{(\Sigma\Delta)}$ in dB due to the clock jitter is

$$\mathrm{SNR}_{(\Sigma\Delta)}[\mathrm{dB}] = 10\log_{10}\left(\frac{\sigma^2_{\mathrm{signal}}}{\sigma_q^2}\cdot\frac{Lf_s}{2f_b}\right) = 10\log_{10}\left(\frac{1}{8\sigma_j^2 f_b L f_s}\right), \tag{20}$$

where L is the oversampling ratio and f_s is the Nyquist sampling rate. With $f_s = 2f_b$, the $\mathrm{SNR}_{(\Sigma\Delta)}$ becomes

$$\mathrm{SNR}_{(\Sigma\Delta)}[\mathrm{dB}] = 10\log_{10}\left(\frac{1}{16 L f_b^2 \sigma_j^2}\right). \tag{21}$$

From Eq. (21), it can be seen that the noise caused by jitter is not frequency dependent and that a low L is favorable for low clock jitter sensitivity. As an example, clock jitter with a standard deviation σ_j of 100 ps reduces the $\mathrm{SNR}_{(\Sigma\Delta)}$ (as well as the dynamic range) of a $\Sigma\Delta$ modulator (as well as $\Sigma\Delta$ ADC) with $L = 64$ and $f_b = 20$ kHz to about 83.8 dB compared with $\mathrm{SNR}_{(\mathrm{PCM})}$ of about 98 dB. The last value can be calculated with $f = 20$ kHz and $\sigma_j = 100$ ps using the equation

$$\mathrm{SNR}_{(\mathrm{PCM})}[\mathrm{dB}] = 10\log_{10}\left(\frac{1}{4\pi^2 f^2 \sigma_j^2}\right), \tag{22}$$

which well corresponds to Eq. (12). Equations (21) and (22) show that the value of the $\mathrm{SNR}_{(\Sigma\Delta)}$ is $4L/\pi^2$ (about 14 dB) worse than that of the $\mathrm{SNR}_{(\mathrm{PCM})}$.

It is clear that clock jitter causes an error in the sampling operation, which adds noise to the sampled signal (increases the noise floor). As the result the SNR of the $\Sigma\Delta$ ADC is degraded. Usually, to avoid the SNR degradation, a crystal oscillator is used and than the jitter is low. However, the layout of the clock distribution circuitry should be attentively designed in order not to destroy the low-jitter crystal clock.

3.3. Methods to increase the jitter tolerance of CT $\Sigma\Delta$ modulators

To reduce the effect of clock jitter in CT $\Sigma\Delta$ modulators non-rectangular feedback signals can be used (San Pablo *et al.*, 2005). In particular, a decaying ramp, a decaying exponential signal, and a cosine pulse were considered. The proposed idea to reduce the clock jitter, described in (Ortmanns *et al.*, 2001) is to introduce a modified form of SC feedback into the CT $\Sigma\Delta$ modulator. It uses a so called switched-capacitor–resistor (SC-R) DAC configuration to produce the DAC pulses that are exponentially decaying as shown in Fig. 10.

These pulses are similar to a DT $\Sigma\Delta$ modulator. The sensitivity to clock jitter can be reduced in term of the in-band nosie (IBN) of about 10 dB or even more (depending on the settlin time τ) due to the sloping pulse form of a discharging capacitor. In order to retain the advantages of the CT modulators concerning

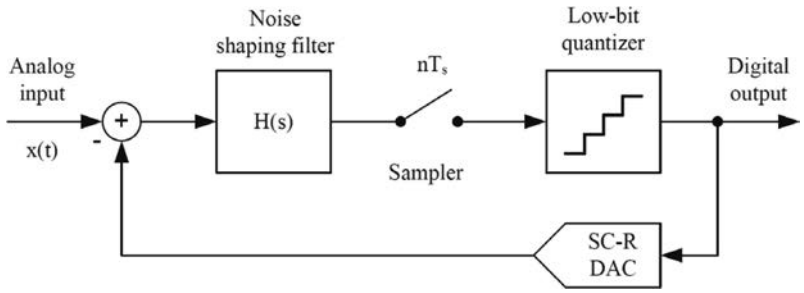


Fig. 10. CT ΣΔ modulator with SC-R DAC feedback.

speed, a resistor was introduced in series to the switched capacitor. So, the shape of the pulse can be chosen to match the jitter requirements.

4. Effect of periodic clock jitter in PCM and ΣΔ ADCs

So far we have considered sampling jitter components modeled in the time-domain (Secs. 2 and 3 of this paper) with the assumption that they are random. But clock jitter can be also analyzed in a frequency-domain. Then it is well described by its spectral characteristics, particularly in the case of periodic (also known as modulated) clock jitter. When analyzed in the frequency domain, the effects of periodic jitter on the sampling clock of an ADC are quite similar to the FM modulation. The simulation results confirmed by the measurements of Harris (Harris, 1990) indicated, that a sinusoidal clock jitter introduces sideband tones equally spaced on both sides of the input component at a distance equal to multiples of the jitter frequency. These sideband tones can introduce nonlinear distortion to the audio signal. As known from previous discussion, the random clock jitter leads to overall elevation of the noise floor level.

Angus (1998) and Dunn (2000) have shown mathematically that there exist a simple relationship between a jitter spectral component, an audio signal spectral component and the resulting jitter modulation product. For a sinewave input signal

$$x(t) = X_m \cos \omega_i t \tag{23}$$

and for a sinusoidal jitter of frequency ω_j and a peak-to-peak amplitude of jitter $t_{j(p-p)}$, the output signal $x'(t)$ is given by the following equation:

$$x'(t) = X_m \cos \omega_i t + X_m \frac{t_{j(p-p)}\omega_i}{4} \cos\left[(\omega_i - \omega_j) \cdot t\right] - X_m \frac{t_{j(p-p)}\omega_i}{4} \cos\left[(\omega_i + \omega_j) \cdot t\right]. \tag{24}$$

The output signal consists of the input signal and two other components at frequencies offset from the input signal frequency by the jitter frequency

(Fig. 11). As can be seen that the input signal is at 10 kHz and the jitter modulation is at 3 kHz. The two components at 3 kHz offset from the input signal are the upper and lower jitter modulation sidebands. The ratio of the signal to each sideband (Dunn, 2000) for sinusoidal jitter components is

$$R_{ssb}[\text{dB}] = 20\log_{10}\left(\frac{t_{j(p-p)}\omega_i}{4}\right). \tag{25}$$

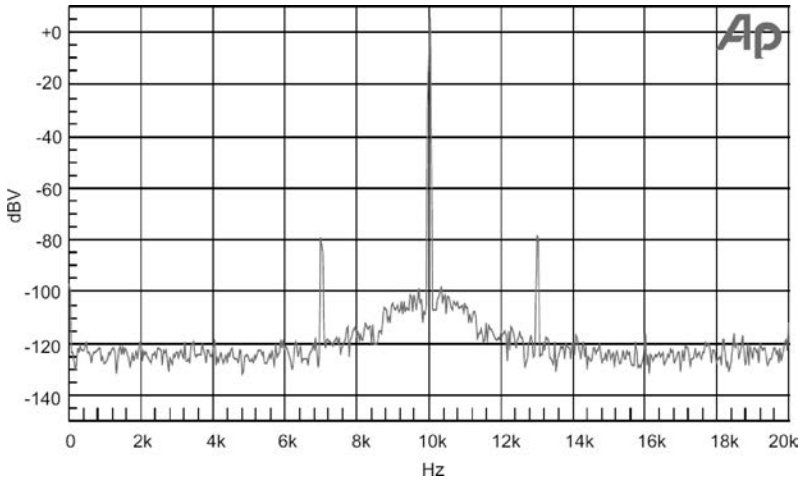


Fig. 11. Jitter-modulated sidebands (Dunn, 2000).

Harris has shown that ΣΔ ADCs are equally susceptible to periodic (sinusoidal) clock jitter as PCM (SAR) ADCs. However, the ΣΔ ADCs are less susceptible to random clock jitter (i.e. white clock jitter) than PCM ADCs because the jitter is extended over the oversampling range and lowpass filtered.

5. Conclusion

In sampling systems like the audio ADCs, the timing jitter is one of the most important factors that limit their signal-to-noise ratio (SNR) as well as the dynamic range (DR). In the case of conventional (PCM) audio ADCs (almost all of them are SAR ADCs), there are three major contributors of jitter: the sampling circuit jitter or aperture jitter, the sampling clock jitter, and the analog input signal jitter. Those three jitter components create the total sampling jitter which results in a voltage error proportional to the input signal slew rate. So, the total sampling jitter is a contributor to the noise floor of an ADC. This can be estimated or measured basing on the degradation in the SNR performance of the converter.

The continuous-time (CT) audio ΣΔ ADCs have some advantages compared to the discrete-time (DT) audio ΣΔ ADCs, such as inherent anti-aliasing filter-

ing, higher sampling rate, lower thermal noise and lower power consumption. The main disadvantage of the CT $\Sigma\Delta$ modulator is its sensitivity to the clock jitter of the feedback DAC which is not shaped with the loop filter. Timing errors due to clock jitter in the feedback loop increases the noise level in the signal band. Clock jitter is mainly caused by the instability of the oscillator which results in sampling time errors in the ADC and thereby degrading the converter's achievable SNR.

It is clear, that the ADC is one of the most critical digital audio components susceptible to jitter. The clock that drives an ADC must be very stable. A random clock jitter as well as periodic clock jitter in the ADC can cause a significant noise and/or distortion which cannot be cancelled out or eliminated at further stages in the audio chain. If it is possible, an ADC should be running from the internal clock, i.e. from a crystal oscillator (XCO or VCXO).

References

1. Ahmed G., Baghel R.K. (2010), *Jitter analysis of continuous-time sigma-delta wideband ADC for software defined radio*, International Journal of Engineering Science and Technology, **2**, 9, 4336–4341.
2. Angus J.A.S. (1998), *A new method for analysing the effects of end-to-end jitter in digital audio systems*, 104th AES Convention, Paper 4716, Amsterdam, May 16–19.
3. Ashry A., Aboushady H. (2009), *Fast and accurate jitter simulation technique for continuous-time sigma-delta modulators*, Electronics Letters, **45**, 24.
4. Awad S.S. (1998), *Analysis of accumulated timing-jitter in the time domain*, IEEE Trans. on Instrumentation and Measurement, **47**, 1, 69–73.
5. Brannon B., Barlow A. (2006), *Aperture uncertainty and ADC system performance*, Analog Devices, Application Note AN-501.
6. Chiorboli G., Fontanili M., Morandi C. (1997), *A new method for estimating the aperture uncertaint of A/D converters*, Proc. of the IEEE Instrumentation and Measurement Technology Conference, Ottawa, May 19–21, pp. 632–635.
7. Chopp P.M., Hamouni A.A. (2009), *Analysis of clock-jitter effects in continuous-time* $\Sigma\Delta$ *modulators using discrete-time models*, IEEE Trans. on Circuits and Systems-I: Regular Papers, **56**, 6, 1134–1149.
8. Dunn J. (2000), *Jitter theory*, Audio Precision, TN-23.
9. Harris S. (1990), *The effects of sampling clock jitter on Nyquist sampling Analog-to-Digital Converters, and on Oversampling Delta-Sigma ADCs*, Journal of the Audio Engineering Society, **38**, 7/8, 537–542.
10. Kester W. (2008), *Aperture time, aperture jitter, aperture delay time – removing the confusion*, Analog Devices, MT-007 Tutorial, Oct.
11. Kobayashi H., Morimura M., Kobayashi K., Onaya Y. (1999), *Aperture jitter effects in wideband ADC system*, Proc. 6th IEEE Int. Conf. on Electronics, Circuits and Systems (ICECS), Pafos, Sept., pp. 1705–1708.

12. Kobayashi D., Takagi S., Fujii N. (2007), *Jitter tolerant continuous-time sigma-delta A-D Converter employing in-loop low-pass filter*, IEEE Trans. Fundamentals, **E90**, 2, 351–357.

13. Kulka Z. (2006), *Analog-to-digital and digital-to-analog converters for high-quality musical sound*, Wydawnictwo Politechniki Białostockiej, Rozprawy naukowe, **134**, I, 269–288.

14. Ortmanns M., Gerfers F., Manoli Y. (2001), *Clock jitter insensitive continuous-time* $\Sigma\Delta$ *modulators*, 8th IEEE Int. Conf. on Electronics, Circuits and Systems, Vol. 2, Malta, 2–5 Sept. 2001, pp. 1049–1052.

15. Raikwar P., Trivedi P. (2009), *Analysis of timing jitters on the performance of bandpass DT-sigma delta ADC for software defined radio receivers*, Int. Journal of Recent Trends in Engineering, **2**, 7, 46–48.

16. San Pablo J., Bisbal D., Quintanilla L., Arias J., Enriquez L., Vicente J., Bafbolla J. (2005), *Jitter effect comparison on continuous-time sigma-delta modulators with different feedback signal shapes*, VLSI Circuits and Systems II, Proc. of the SPIE, **5837**, 83–92.

17. Shamsi H. (2008), *Less jitter sensitive NTF design for NRZ multi-bit continuous-time delta-sigma modulators*, IEICE Electronics Express, **5**, 21, 895–900.

18. Shinagawa M., Akazawa Y., Wakimoto T. (1990), *Jitter analysis of high-speed sampling systems*, IEEE Journal of Solid-State Circuits, **25**, 1, 220–224.

19. Srinivasan V., Islam S.K., Hendrickson G.T. (2002), *A method for the estimation of aperture uncertainty in A-D converters*, The IEEE Int. Symp. on Circuits and Systems (ISCAS), **3**, 125–128.

20. Strak A., Gothenberg A., Tenhunen H. (2004), *Analysis of clock jitter effects in wideband sigma-delta modulators for RF-applications*, Kluwer Academic Publishers, Analog Integrated Circuits and Signal Processing, **41**, 2–3, 223–236.

21. Tortosa R., Rosa J.M., Rodriguez-Vasquez A., Fernandez F.V. (205), *Analysis of clock jitter error in multibit continuous-time* $\Sigma\Delta$ *modulators with NRZ feedback waveform*, Proc. of Int. Symp. on Circuits and Systems, ISCAS, **4**, 3103–3106.

22. Veldhoven R.H.M. (2003), *A triple-mode continuous-time* $\Sigma\Delta$ *modulator with switched-capacitor feedback DAC for a GSM-EDGE/CDMA2000/UMTS receiver*, IEEE Journal of Solid-State Circuits, **38**, 12, 2069–2076.

23. Walden R.H. (1999), *Analog-to-digital converter survey and analysis*, IEEE Journal on Selected Areas in Communications, **JSAC-17**, 4, 539–550.

24. Yang Y., Sculley T., Abraham J. (2007), *A 330 mW 216 kHz 124 dB single die stereo delta-sigma audio analog-to-digital*, 123rd AES Convention, Paper 7289, New York, Oct. 5–8.

25. van der Zwan E.J., Dijkmans E.C. (1996), *A 0.2-mW CMOS* $\Sigma\Delta$ *modulator for speech coding with 80 dB dynamic range*, IEEE Journal of Solid-State Circuits, **31**, 12, 1873–1880.