AN ANALOG LINEAR SVM IMAGE CLASSIFIER

Lelia Festila, Lorant Andras Szolga, Robert Groza, Sorin Hintea and Mihaela Cirlugea

Abstract:

A linear Support Vector machine classifier is proposed in this paper. In such SVM architectures based on multiplying laws the main building blocks are multipliers. We propose in this paper multiplying and weighting cells, developed by using a model consisting of a compound of two inverse non-linear functions. This procedure is suitable for VLSI implementation because it permits the use of simple nonlinearized standard log-domain or DA cells that compensate each other nonlinearities to obtain an extended domain of operation. Current-mode ELIN (externally linear internally nonlinear) design is used for its low voltage, low power and high speed characteristics. The resulted parallel-serial classifier was simulated taking into account real parameters of transistors in BICMOS technology.

Keywords: *Support Vector Machine, analog multipliers, log-domain th domain, square-root domain, image classifier.*

1. Introduction

Support vector machines (SVMs) are a set of related supervised learning methods used for classification and regression [9]. A binary SVM classifier has to decide which of two classes C and $C`$ an object belongs. It classifies positively the object if it belongs to the class C and negatively if it does not [1], [3]. The classifier is trained with positive and negative labeled vectors of features (objects or data points) belonging or not to the given class C. The training results consist of M support vectors (SVs) X_m, $m=1,2...M$, which include relevant features of the training vector set and also Lagrange coefficients am and labels $y_m \in \{-1,1\}$ assigned to each SV. Label y_m is 1 if X_m belongs to class C and -1 if it belongs to $C`$.

A vector X to be classified is given to the already trained classifier characterized by SVs X_m, $m=1,\ldots,M$ and their corresponding Lagrange coefficients and labels.

$$X=\left[X_1, X_2 ... X_N\right]^T \;;\; X_m=\left[X_{m1}, X_{m2} ... X_{mN}\right]^T . \quad (1)$$

The classifier calculates a decision function. Its sign represents the label y to be assigned to the tested vector X, which is positive classified if $y \geq 0$. For example the linear classifier considered in this paper has the decision function based on a multiplying law and the label to be calculated is of the following form [4]:

$$y=sign\left(\sum_{m=1}^{M} y_m \alpha_m X^T X_m + b\right)=sign\left(\sum_{m=1}^{M} y_m \alpha_m \left(\sum_{j=1}^{N} X_{mj} X_j\right)+b\right). \quad (2)$$

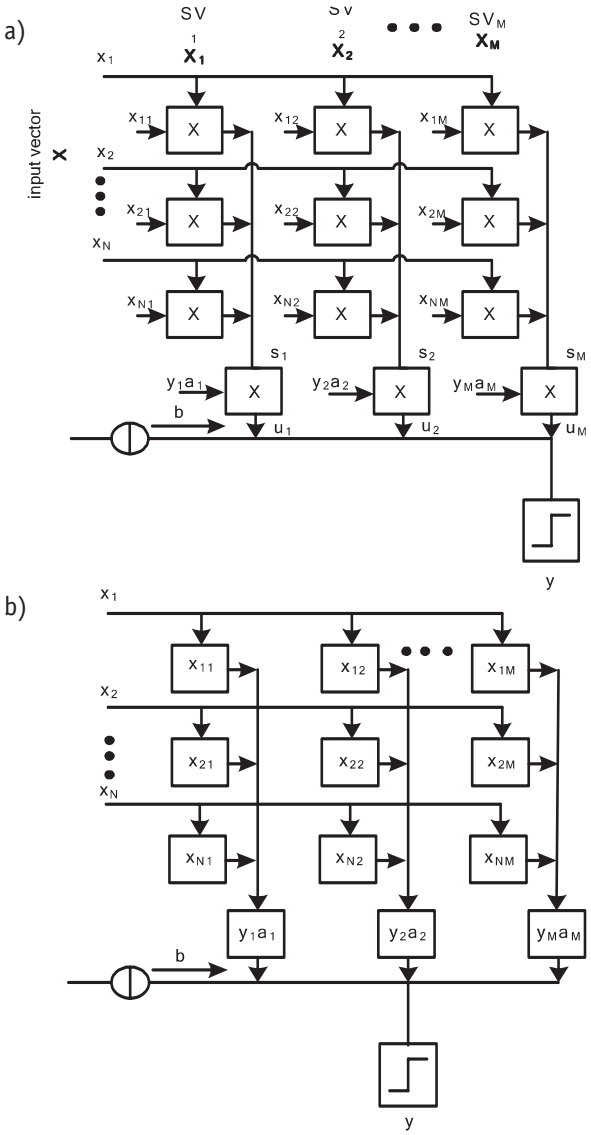


Fig. 1. Block diagram of a cellular parallel SVM classifier with multiplying law: (x_k x_{kj}), k = 1,…,N; j = 1,…,M; N - vector length; M - number of SV; a) with multiplying cells; b) with weighting cells.

Examining relation (2) one can see that to implement such a SVM classifier we need multipliers as basic functional unities. The $X^T X_m$ operation is implemented by a matrix of multiplying cells as Fig. 1a shows. Each product $X^T X_m$ is then multiplied by its corresponding coefficient $a_m y_m$. If the resulted u_m, $m=1,\ldots,M$ signals are currents, they can be summed by simple connections. A constant current b is added then and finally a current comparator delivers the decision function y [5].

If a SVM classifier is dedicated to a specific application, SVs X_m and coefficients could be fixed parameters

set by design and the basic functional unities become simple weighting elements, as Fig. 1b shows.

As SVM classifiers usually require a large amount of calculations, their VLSI implementations need high density, high speed and low power circuits.

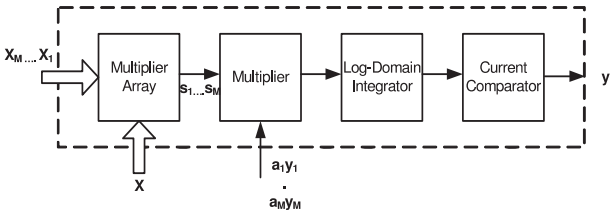


Fig. 2. Proposed Log-Domain SVM classifier block diagram.

Fig. 2 shows the block diagram of the serial-parallel classifier presented in this paper. The multiplier array has the structure of a column in the NxM array in Fig. 1. Support vectors are serially introduced and also coefficients $a_i y_i$. To add continuously each vector product XX_i^T to the partial sum a log-domain integrator is used. The circuit also contains at the output a signal comparator to classify the input vector of data.

Because the main building blocks in the SVM architecture in Fig. 1 and Fig. 2 are multipliers or weighting elements we propose in this paper current-mode multiplying and weighting cells, developed by using a model consisting of a compound of two inverse non-linear functions. This procedure is suitable for VLSI implementation because it permits the use of simple nonlinearized cells that compensate each other nonlinearities to obtain an extended domain of operation - procedure characteristic for ELIN (externally linear-internally nonlinear) circuits [2].

We will also present the other component circuits for the SVM parallel classifier proposed in this paper and then the simulation results for an image recognition table.

2. Multiplier current-mode models and schematics based on F-F^{-1} functions

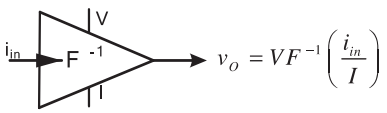
2.1. Multiplying F-F^{-1} models

Let define an invertible function $F: x \to y$, where variables x and y are nondimensional, expressed by normalized voltages and currents respectively:

$$\frac{i}{I} = F\left(\frac{v}{V}\right) \qquad and \qquad \frac{v}{V} = F^{-1}\left(\frac{i}{I}\right). \tag{3}$$

Consider that the above functions can be implemented by two basic building blocks F, a nonlinear transconductor, and F^{-1}, a nonlinear transresistor represented in Fig. 1.

a)



b)

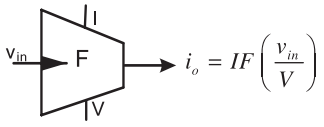
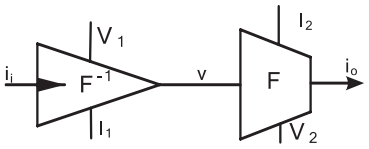


Fig. 3. F^{-1} (Fig. 1a) and F (Fig. 1b) building block symbols.

One connects two F and F^{-1} blocks as in Fig. 3. If the requirement $V_1 = V_2 = V$ may be fulfilled, a current-mode weighting cell or a multiplier can be realized (Fig. 4):



if $V_2 = V_1 = V \Rightarrow i_o = \frac{I_2}{I_1} i_i$

Fig. 4. Current-mode weighting cell or multiplier.

If currents I_1 and I_2 can be set independently of voltages V_1 and V_2, respectively, multipliers result. The type of the multiplier depends on the input port type. The input signal may admit one or two directions, respectively, but scaling currents I or voltages V are usually one-directional in the basic building blocks. Therefore, by using the block diagrams from Fig. 3, 1-Q or 2-Q multipliers result. For a four-quadrant multiplier an extra current source is needed, as Fig.5 shows as an example.

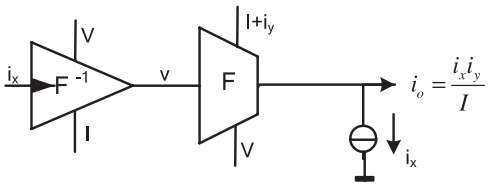
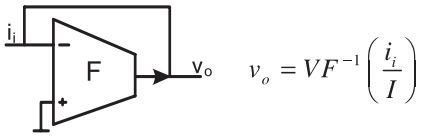


Fig. 5. Basic 4-Q current mode multiplier model: i_x and i_x are bi-directional input signals.

Fig. 6a and 6b show some variants for implementing block F^{-1} with an inverting nonlinear block F.

a)



if $F(-x) = -F(x)$

b)

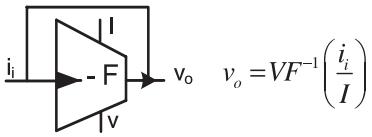


Fig. 6. Implementation of function F^{-1} with: a) a differential F block; b) an inverting F block.

In the following we analyze examples of multipliers based of the above-proposed F-F^{-1} models in log-domain, or hyperbolic-domain. In square-root domain the model leads to an uncontrollable gain.

2.2. A Log Domain 4Q Multiplier

Based on models given in Fig. 3-6, we developed in [5] log-domain multipliers with ln-exp building blocks. In this case F and F^{-1} functions are:

$$F: \frac{i_o}{I} = exp^{\frac{v_i}{V_T}} \quad ; \quad F^{-1}: \frac{v_o}{2V_T} = \ln\frac{i_i}{I} \tag{4}$$

The basic circuits and their symbols are shown in Fig. 7. Input I_x in Ln block is onedirectional so the multiplier having the structure from Fig. 3 is a $1Q$ one.

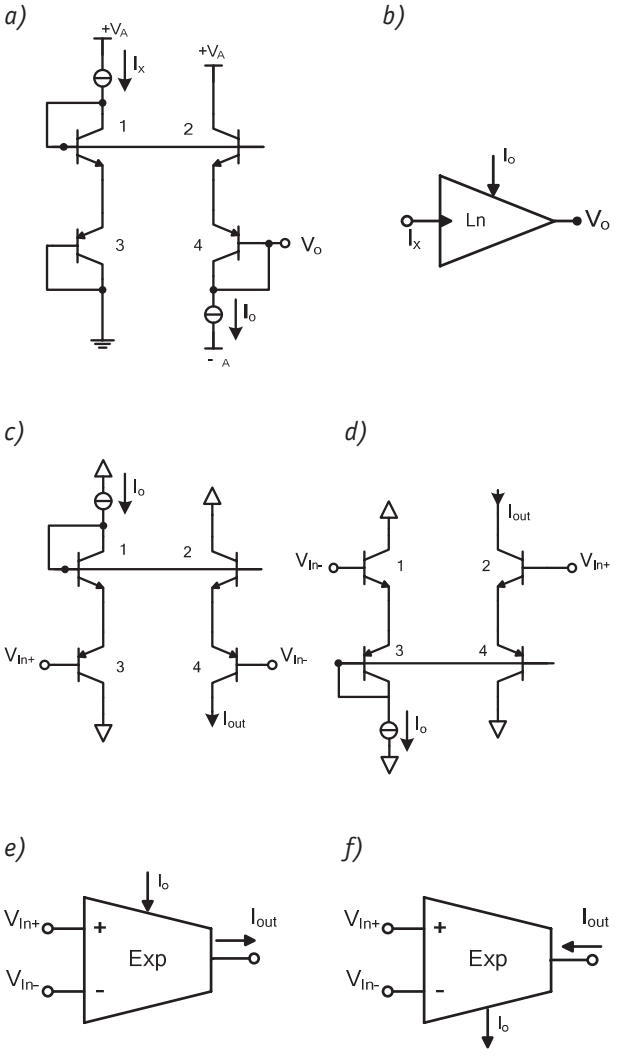


Fig. 7. Log-Exp building blocks: a) ln circuit; b) symbol of ln block; c),d) exp circuits; e), f) symbol of exp circuits.

The $4Q$ multiplier based on the model in Fig. 3 is presented in Fig. 8a. The input-output characteristics for $i_1 \in \{-[-9uA, 9uA]$ having i_2 as parameter [-9uA,-5uA,-1uA,1uA,5uA,9uA] are given in Fig. 8b.

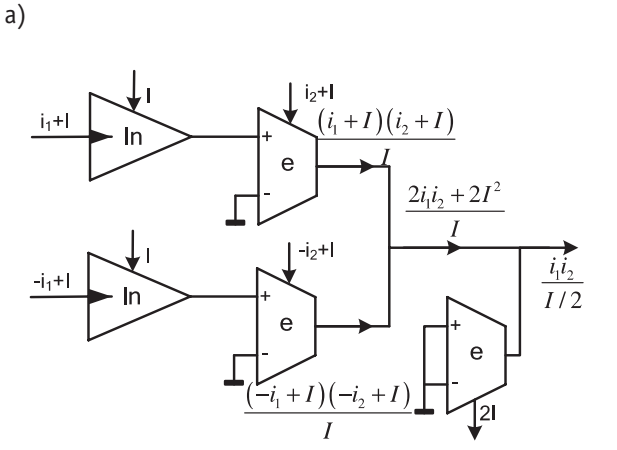
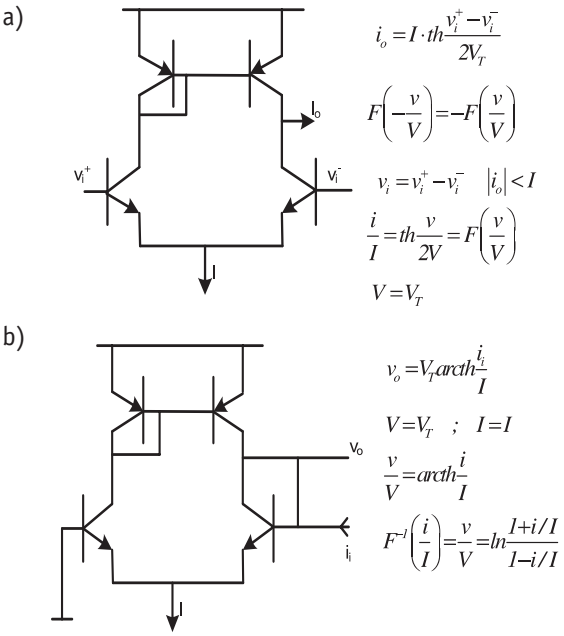


Fig. 8. $4Q$ log-domain multiplier: a) block diagram; b) DC sweep simulation results.

The relation between in/out signals and the linearity of the characteristics proves the validity of models.

2.3. Multiplying cell realized with bipolar DAs



$$i_o = I \cdot th\frac{v_i^+ - v_i^-}{2V_T}$$

$$F\left(-\frac{v}{V}\right) = -F\left(\frac{v}{V}\right)$$

$$v_i = v_i^+ - v_i^- \quad |i_o| < I$$

$$\frac{i}{I} = th\frac{v}{2V} = F\left(\frac{v}{V}\right)$$

$$V = V_T$$

$$v_o = V_T arcth\frac{i_i}{I}$$

$$V = V_T \;;\; I = I$$

$$\frac{v}{V} = arcth\frac{i}{I}$$

$$F^{-1}\left(\frac{i}{I}\right) = \frac{v}{V} = ln\frac{1+i/I}{1-i/I}$$

Fig. 9. Bipolar differential amplifier used in the large signal domain a) F block: th cell; b) F^{-1} block: arcth cell.

The large signal model of a DA in bipolar technology is described by a hyperbolic tangent function as Fig. 9a shows. In Fig. 9b the connection implementing F^{-1} function is given. The input signal in the F cell is $v_i = v_i^+ - v_i^-$.

One can see that the requirement $V_1 = V_1 = V_T$ is fulfilled and a $2Q$ current mode multiplier may be realized using the model from Fig. 3. Fig. 10 shows the schematic of such a $2Q$ multiplier and $i_{out} = f(i_x)$ characteristics for $I_y = ct$ as a parameter. In Fig. 11a $4Q$ multiplier is shown considering the model from Fig. 4. Simulations have proved the validity of the models and also the linearity on the whole domain $|i_x|, |i_y| < I$.

The same conclusions result if schematics from Figs 9-10 are realized with MOS transistors in weak inversion, because functions F-F^{-1} remain of the same type.

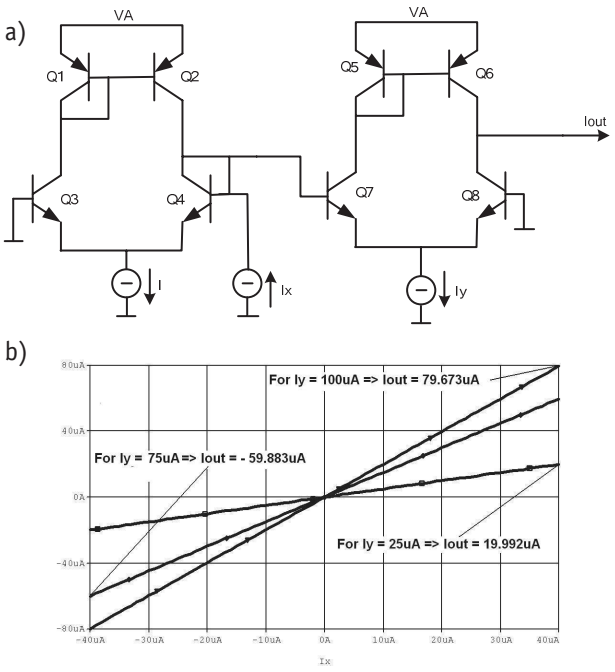


Fig. 10. 2Q multiplier a) schematics; b) in-out characteristics for I_y= ct and I=50μA.

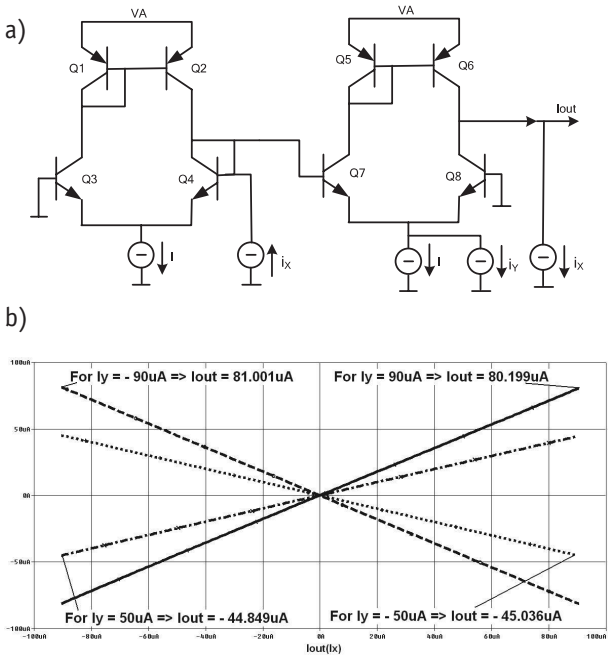
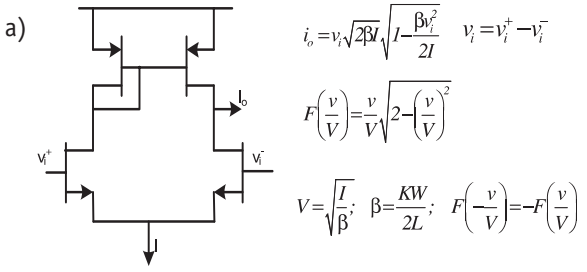


Fig. 11. 4Q multiplier for I_y= ct and I_x=100μA a) schematic; b) in-out characteristics.

Weighting cells with MOSFETs saturated in strong inversion

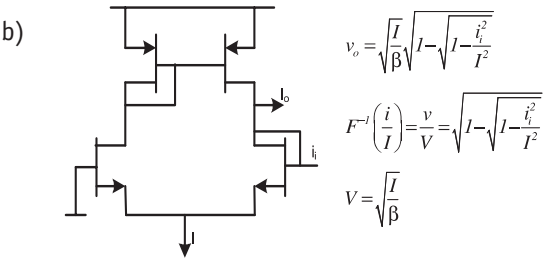
Figures 12a and 12b present both F and F^{-1} functions implemented by simple differential amplifiers (DAs) with saturated MOS transistors in strong inversion.



$$i_o = v_i\sqrt{2\beta I}\sqrt{1-\frac{\beta v_i^2}{2I}} \qquad v_i = v_i^+ - v_i^-$$

$$F\left(\frac{v}{V}\right) = \frac{v}{V}\sqrt{2-\left(\frac{v}{V}\right)^2}$$

$$V = \sqrt{\frac{I}{\beta}}; \quad \beta = \frac{KW}{2L}; \quad F\left(-\frac{v}{V}\right) = -F\left(\frac{v}{V}\right)$$



$$v_o = \sqrt{\frac{I}{\beta}}\sqrt{1-\sqrt{1-\frac{i_i^2}{I^2}}}$$

$$F^{-1}\left(\frac{i}{I}\right) = \frac{v}{V} = \sqrt{1-\sqrt{1-\frac{i_i^2}{I^2}}}$$

$$V = \sqrt{\frac{I}{\beta}}$$

Fig. 12. Square-root F and F^{-1} cells a) F cell ; b) F^{-1} cell.

In the same figures the functions F and F^{-1} are deduced on the base of the input output relations $i_O = f_1\left(v_i^+ - v_i^-\right)$ Fig. 11a and $v_O = f_2\left(i_i\right)$ Fig. 12b. The circuit having the model in Fig. 3 is shown in Fig. 13.

In this case considering Fig. 3, relation $V_1 = V_2$ has to be fulfilled, that is:

$$\frac{I_1}{\beta_1} = \frac{I_2}{\beta_2} \quad \Rightarrow \quad i_o = \frac{I_2}{I_1} i_i = A_i i_i \; ; \; A_i = \frac{W_2/L_2}{W_1/L_1}. \tag{4}$$

One can see that the current gain A_i cannot be controlled. Therefore the current amplifier from Fig. 13 could only be used to realize weighted signals with fixed weights.

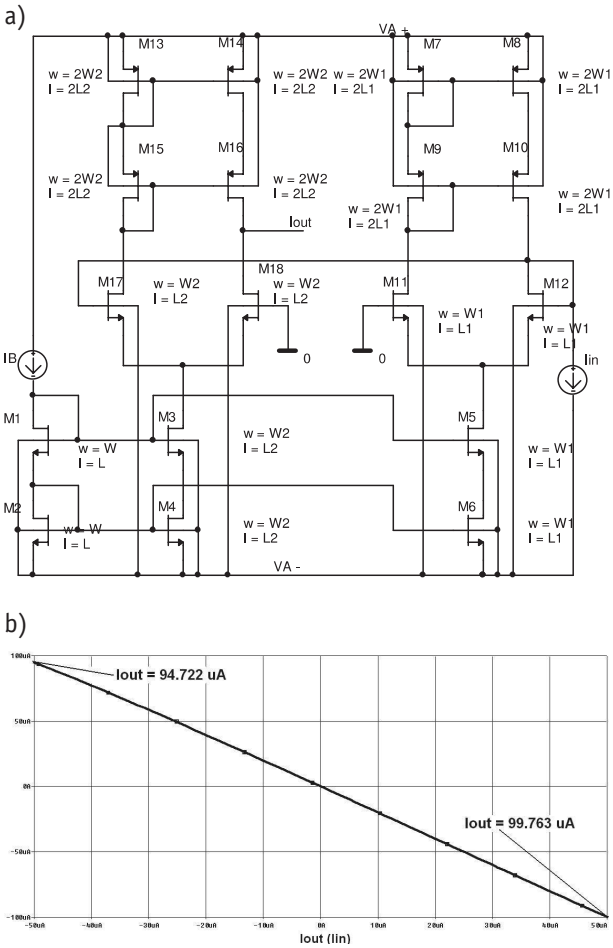


*Fig. 13. Current amplifier for W_2/L_2 = 2*W_1/L_1 a) schematics; b) in-out characteristic.*

3. SVM classifier components

A SVM parallel-serial classifier having the architecture shown in Fig. 2 is proposed in BICMOS technology. The basic building blocks are: multiplying cells, integrator and comparator.

The variant proposed in this paper contains log-domain multipliers shown in Fig. 8 based on $\underline{e}$ and $\underline{ln}$ modules from Fig. 7. Because one has to sum sequential signals resulted by multiplying test vector X with each support vector X_m a log-domain integrator was used as Fig. 14 shows [6].

The final result y is given by a current comparator [11] in Fig. 15.

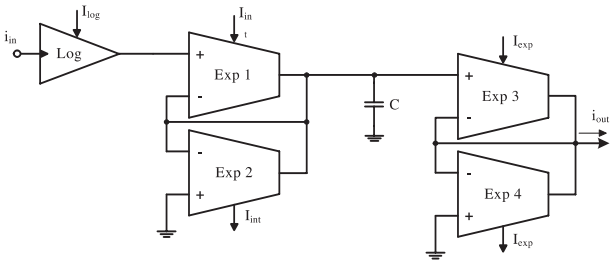


Fig. 14. Log-Domain Integrator.

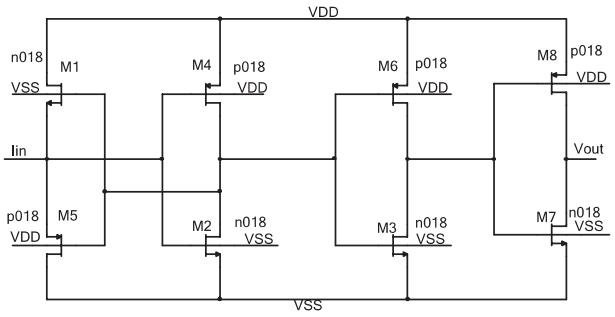


Fig. 15. Current comparator circuit.

4. Simulation Results

Simulations have been performed taking into account applications in image classifications. For example a SVM was trained by software to identify the letter F in a 6x7 image. A number of 16 positive and 16 negative examples were considered in the training. The results are 16 SV's as Fig. 16 shows and also coefficients $a_i y_i$, $i=1,2\ldots6$ given in Table1.

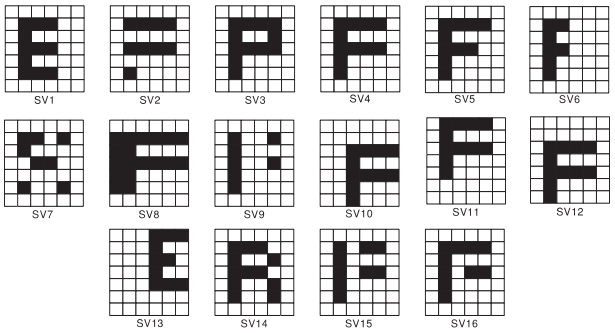


Fig. 16. SV's resulted after the training process.

Table 1. Support Vector Coefficients.

Support Vector	$a_i y_i$	Support Vector	$a_i y_i$
SV1	-0.700	SV9	-1.493
SV2	0.067	SV10	0.187
SV3	-0.410	SV11	0.098
SV4	0.038	SV12	0.025
SV5	0.213	SV13	-0.199
SV6	0.989	SV14	-0.200
SV7	-0.113	SV15	1.382
SV8	-0.070	SV16	0.187

The images to be tested are given in Fig. 17. The resulting output currents of the integrator corresponding to each tested image are shown in Table 2.

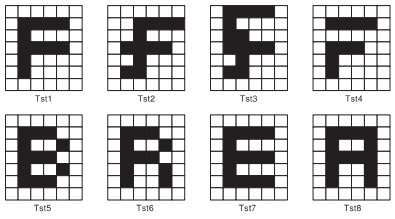


Fig. 17. Test images.

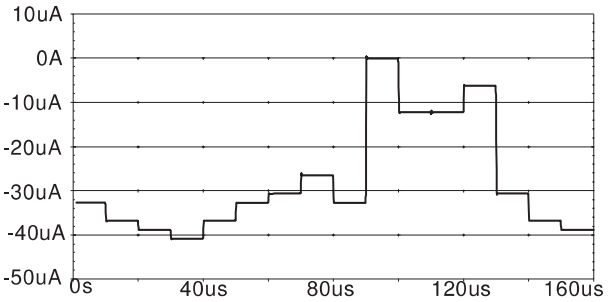
Table 2.

Test Image	Iout_integ	Classified	Test Image	Iout_integ	Classified
Tst1	1.34u	+	Tst5	-2.47u	-
Tst2	0.45u	+	Tst6	-1.95u	-
Tst3	-3.51u	-	Tst7	-0.4u	-
Tst4	-4.85u	-	Tst8	-0.42u	-

The input current for a black pixel was considered -1 μA and the value for the white one +1 μA; the bias current b is 4 μA. At the output of the inverting current comparator, the positive values of the decision function indicate the images close to the given reference image, in our case letter F.

In Fig. 18 we present the signals from the outputs of the main building blocks, for a given test image, in this case, Tst1 from the Fig. 18. The following output signals are considered: the output current of the multiplier array, a), the output current from the second multiplier block, which performs the product between the first signal and the SV's coefficients presented in Table 1; b), the resulting current at the current summator log-domain block, c) and finally the output voltage of the current comparator d). The time necessary to realize the classification operation with the given number of SV's was 160 μs.

a)



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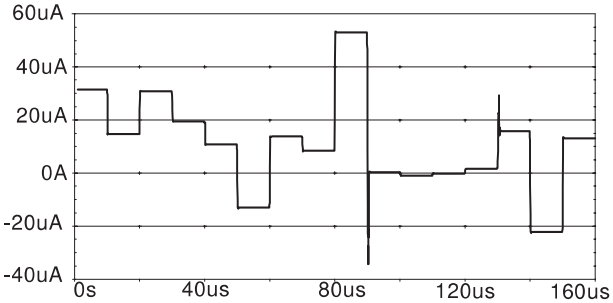

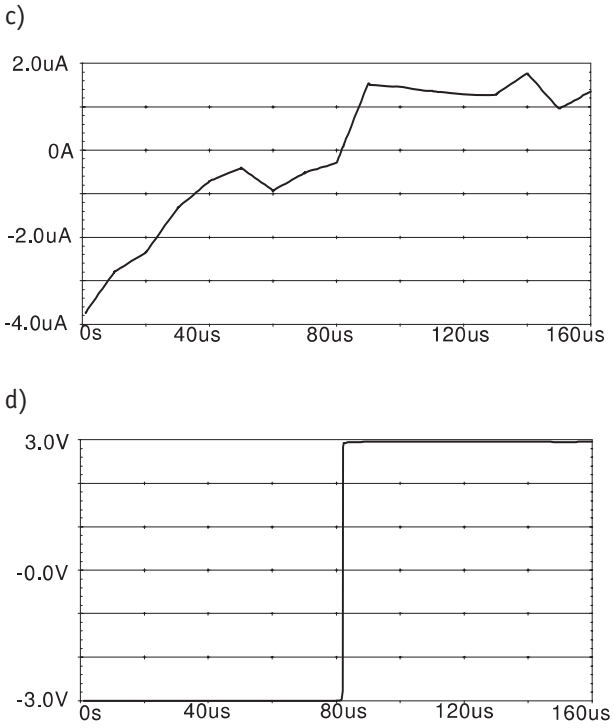

Fig. 18. Simulation results: a) output signal from the multiplier array; b) output signal of the second multiplier; c) output signal from the log-domain current summator; d) output signal from the current comparator.

5. Conclusion

Modularity, current programmability of the parallel-serial SVM classifier proposed in this paper recommend it for standard cell design and real time operation in image classification tasks. ELIN design was extended in this paper to modular nonlinear circuits like multipliers.

The general modular multiplier models use simple nonlinear F-F^{-1} cells that compensate each other nonlinearities. In this manner the large signal domain can be used extending the linear behavior of input-output characteristics. Replacing the F modules by simple nonlinearized bipolar or CMOS building blocks very simple multiplying/weighting cells may result. They are suitable to be used in VLSI neuron-like networks in particular SVM classifiers because of their simplicity, efficiency and good performance for a large domain of signal variations.

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