A Highly Linear Low Pass Filter for Low Voltage Reconfigurable Wireless Applications

Gabor Csipkes, Sorin Hintea, Doris Csipkes, Cristian Rus, Lelia Festila, Hernando Fernández-Canque

Abstract:

This paper presents a reconfigurable and programmable analogue low pass filter for low voltage wireless applications. The proposed filter may be used for channel or band selection in multi-mode receiver front ends employing direct frequency conversion. The circuit has been synthesized using state variables and leapfrog OTA-C techniques, features programmable order, digitally variable frequency parameters and wide linear range. The fundamental OTA cell has been implemented with fully balanced second-generation current conveyors, suitable for operating with low supply voltages. Transistor level simulations based on a 180 nm digital CMOS technology have demonstrated the functionality of the design.

Keywords: *software radio, reconfigurable filters, state variable synthesis, current conveyors, dynamic bias currents.*

1. Introduction

The widespread of mobile communication systems have led to an unprecedented diversity of functions that the radio access interfaces must integrate. Each of these functions may be associated with a particular communication standard, defined by a precise set of specifications, including channel bandwidth and spacing, carrier frequency, data modulation, analog-digital signal processing and hardware requirements.

The ultimate goal of the industry is the development of the software defined radio (SDR) technology that gives the context for the implementation of different analogue and digital reconfigurable building blocks. In the first acceptance the software defined radio has been envisioned as a signal processing chain in which the data converters are placed directly in the vicinity of the antenna, allowing all the specific radio functions to be realized in the digital domain. In spite of the advantages offered by the ideal architecture, the technology induced limitations concerning the consumption of a data converter capable of sampling the signal at the carrier frequency with sufficiently high dynamic range, may render a real implementation impossible. Therefore, the ideal model must be extended in order to include some analogue interface circuitry [1]. One of the most widely used radio interfaces, considered mainly due to its simplicity and well-understood behaviour, is the so-called zero-IF or direct conversion architecture shown in Fig. 1. Its simplicity makes the direct conversion architecture a good candidate for the implementation of reconfigurable radio interfaces [2].

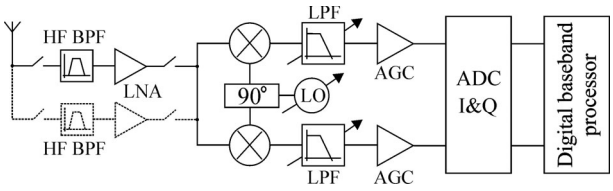

Fig. 1. Typical reconfigurable direct conversion receiver architecture.

In a direct conversion receiver the radio frequency signal is converted directly to the base band by multiplication with a complex local oscillator signal having the same frequency with the RF carrier. The LO signal is generated in quadrature to suppress image components and to allow the correct demodulation of the wanted signal. The advantages of the direct conversion approach over the classical heterodyne architecture are straightforward: there is no need for multiple frequency translations, amplifying and filtering stages, while the channel selection is simply done by means of low pass filters.

A survey of the existing literature shows that the reconfigurable circuits, specifically channel or band select filters within the analogue interface, are key building blocks of a practically feasible SDR transceiver. Although filter design is a very well known area of VLSI circuit development, only few theoretical studies have been published on low voltage reconfigurable filters [3],[4]. The remainder of this paper describes a modular and easily scalable approach to reconfigurable and programmable analogue filter design. The proposed low pass filter is intended for SDR built upon zero-IF analogue interfaces and operates from a single 3 V supply voltage, compatible with modern digital CMOS fabrication technologies.

2. Reconfigurable state variable OTA-C filters

State variable filters stand out among analogue filter architectures due to their low sensitivity performance, inherited from their doubly terminated passive LC prototypes. The implementation based on operational transconductance amplifiers (OTA-s), connected in open loop configurations, allows the operation at high frequencies [9]. Furthermore, the modular structure creates the premise for easy topological reconfiguration, a prerequisite for the design of fully reconfigurable filters.

The versatility in operation is achieved by creating a fundamental module that can be simply cascaded in order to implement higher order filters. The modular structure is based on the circuit template that implements the signal flow graph associated with a generalized LC ladder prototype. The graph corresponding to

a generalized passive LC ladder is shown in Fig. 2. The block diagram has been obtained by writing Kirchoff's theorems and Ohm's law for the nodes and branches of the LC ladder. The dummy resistance R, usually sized to be equal to the termination resistances of the ladder, transforms branch currents into voltages allowing voltage only state variables [5].

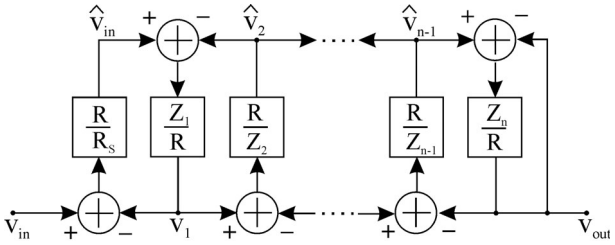

Fig. 2. The signal flow graph corresponding to a generalized LC ladder filter.

Filters designed for communications systems exhibit mainly a low pass or band pass frequency response. In particular, when the imposed operating frequencies are not prohibitive and quadrature signal paths are available, band pass filters may also suppress the image signal in the intermediate frequency stage. In these cases the band pass response is obtained from the low pass transfer function by performing a linear frequency transformation. Therefore, the impedances in the generalized ladder should be particularized in order to accommodate first of all with a low pass response. In this case the odd order transversal components are capacitances and the even order longitudinal components are inductances as shown on the passive low pass prototype in Fig. 3.

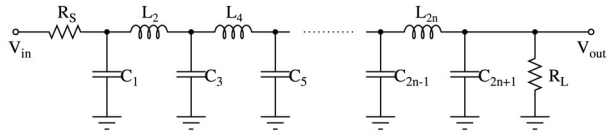

Fig. 3. An odd order doubly terminated low pass ladder filter.

The resulting implementation of the low pass OTA-C filter for an arbitrary odd order n is shown in Fig. 4 [5]. The even order filter can be derived through a similar procedure.

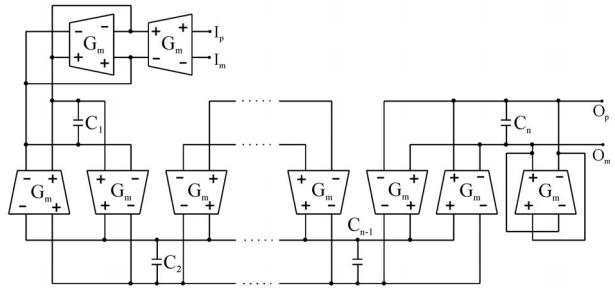

Fig. 4. Schematic of a fully balanced odd order OTA-C filter.

The values of the inductances and capacitances can be calculated after denormalization and impedance scaling. If the characteristic resistance of the ladder is $R=R_S=R_L=1/G_m$ and f_t is the desired corner frequency, the capacitances in the active implementation may be calculated according to the equations (1) [5]. From the sizing equations it can be seen that the corner frequency may be adjusted without modifying the shape of the frequency response by changing G_m. Furthermore, the adjustment of the corner frequency is independent on the filter order.

$$\begin{cases} C_{odd} = \dfrac{C_{2k+1(n)} \cdot G_m}{2\pi \cdot f_t} \\ C_{even} = \dfrac{L_{2k(n)} \cdot G_m}{2\pi \cdot f_t} \end{cases} \tag{1}$$

where $C_{2k+1(n)}$ *and* $L_{2k(n)}$ are the normalized transversal capacitances and longitudinal inductances of the passive low pass prototype.

The complete reconfiguration of the low pass filter implies freely changing the frequency parameters, the filter order and the approximation while dynamically adjusting the current consumption. A careful examination of the filter topology for two consecutive orders may be done when considering the corresponding termination networks for odd and even order implementations shown in Fig. 5. The purpose of the comparison is the identification of a reconfigurable module, simply cascaded in order to obtain a generalized, variable order filter.

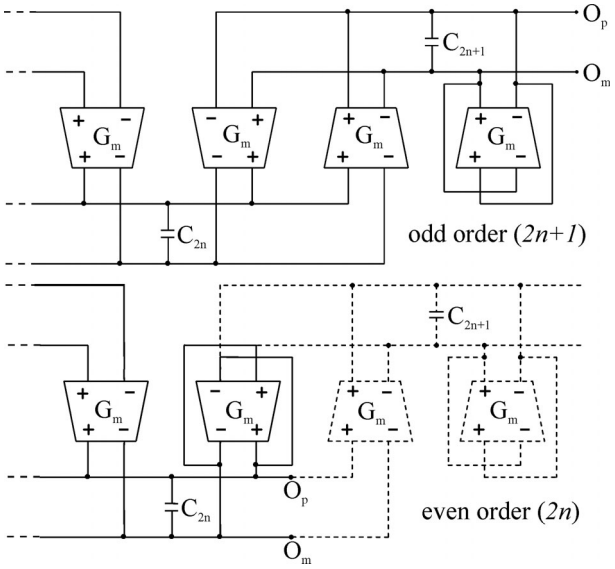

Fig. 5. A comparison between odd and even order termination networks.

The comparison shows that the fundamental module can be implemented around two transconductor cells with switches that connect or disconnect the given module depending on its position in the cascade. Additionally, the negative feedback created around the second OTA in every cell effectively implements an active resistance. The last module in the cascade will have the feedback path activated corresponding the load resistance R_L of the ladder [6]. The resulting reconfigurable module is illustrated in Fig. 6.

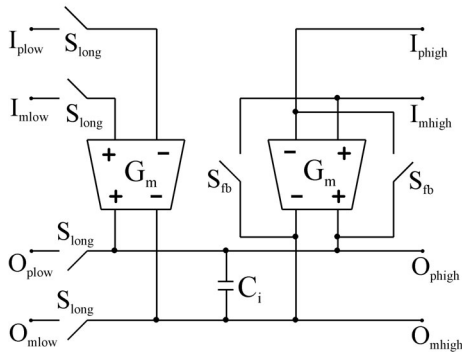

Fig. 6. The reconfigurable filter module.

A simple cascade connection of identical modules, as many as required by the highest desired filter order, controlled by a decode logic, leads to a fully reconfigurable low pass filter implementation. The typical interconnection of several modules in a cascade configuration is shown in Fig. 7.

3. The Transconductance Amplifier

The most important high frequency analogue filter implementation techniques encountered in the literature are based on OTA-C structures. However, transconductance amplifiers are known to exhibit a limited range for the transconductance parameter, low-to-average linear range and relatively high current consumption. Classical linearization methods make use of the non-linear transistor equations and various circuit topologies in order to effectively cancel odd order non-linearities, while even order harmonics may be reduced by fully balanced designs [9]. The circuit described in this work is an alternative to a wide linear range, fully balanced OTA, built around second-generation current conveyors.

Current conveyors play the same role in current mode signal processing as opamps in voltage mode circuits, namely they hold virtual ground for the wanted signal. Their versatility in applications is mainly defined by the configuration of the terminals. A classical method to

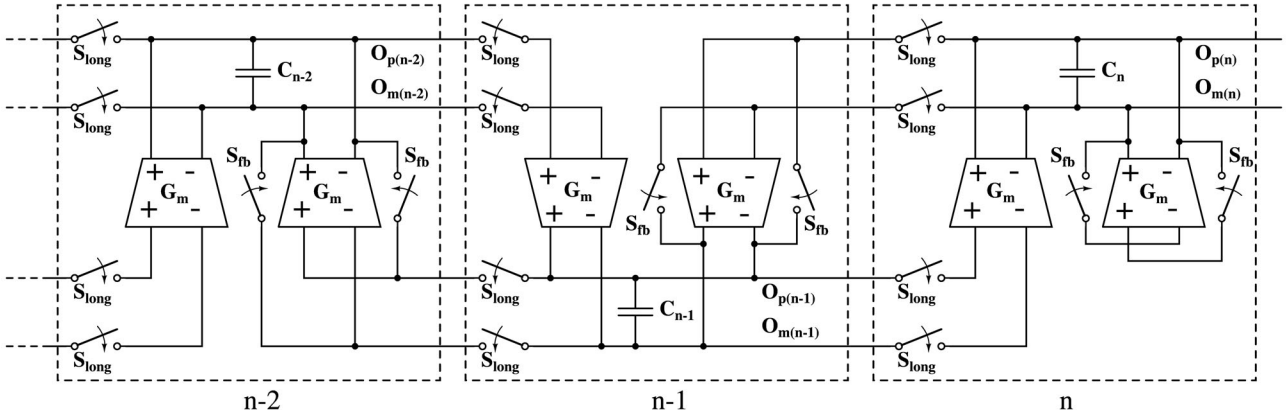

Fig. 7. A cascade of several identical modules to form a filter with variable order.

When the filter order is decreased by one, the longitudinal switches S_{long} in the n^{th} module of the cascade are turned OFF separating the unit from the rest of the ladder. Meanwhile, the switches S_{fb} are also turned OFF and the disconnected OTA cells are forced in a power-down state. The new outputs of the filter will be $O_{p(n-1)}$ and $O_{m(n-1)}$ of the previous module. Additionally, the switches S_{fb} of the termination module n-1 must be turned ON in order to shift the load resistance to the output of the lower order filter. The position of the switches for a filter with consecutive orders n-2, n-1 and n is given in Tab. 1.

Table 1. Switch states for three consecutive filter orders n-1, n-2 and n.

Order	Switch	Module n-2	Module n-1	Module n
n-2	S_{long} S_{fb}	ON ON	OFF OFF	OFF OFF
n-1	S_{long} S_{fb}	ON OFF	ON ON	OFF OFF
n	S_{long} S_{fb}	ON OFF	ON OFF	ON ON

build a transconductance amplifier with a CCII cell is to use the Y terminal as a voltage input. The input voltage is then copied to the X terminal. The voltage V_X determines a current through a resistor connected between the X terminal and the ground. This current is then copied to the Z terminal, used as current output [7]. Mirroring the circuit and connecting a resistor between the X terminals leads to the OTA block diagram shown in Fig. 8.

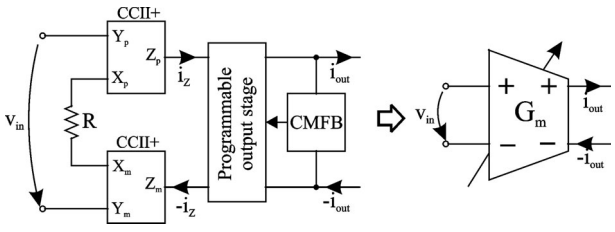

Fig. 8. Block diagram of the programmable transconductance OTA.

The overall transconductance of the circuit will be equal to the reciprocal of the passive resistance R. The programmable output stage is essentially a weighted gain current amplifier permitting the adjustment of the transconductance and of the filter corner frequency. The fully balanced implementation requires a common mode control circuit (CMFB) that sets the DC voltages at the high impedance output terminals [10].

In the ideal case the equivalent transconductance G_m is $1/R$. However, real current conveyors exhibit non-zero parasitic resistances of the X terminal, which must be added twice to the passive resistance R when calculating the transconductance [7]. Furthermore, R_X is often frequency dependent and highly non-linear.

The solution that reduces the relatively high parasitic resistance is to use negative feedback. There are various low input resistance conveyor implementations proposed in the literature. In order minimize the number of stacked transistors between supply rails and allow low voltage operation, the majority of these circuits are using a differential amplifier on the negative feedback path [7]. The filter design presented in this paper is built around Liu's conveyor [8]. Liu's CCII is essentially an unbuffered opamp with Miller compensation, whose second gain stage is used as a current mirror for copying the X terminal current to the Z output. Its main advantages are the simple structure, low current consumption and the potential to operate at supply voltages as low as 1.2 V. The latter option makes the designs compatible with modern, deep submicron CMOS technologies. A special care must be taken of the opamp stability through an adequate compensation. The lead-lag type of compensation, implemented with the resistor R_C in series with the capacitor C_C, yields good results in insuring the stability and in extending the range of the conveyor operating frequencies [7]. The schematic of Liu's CCII is shown in Fig. 9.

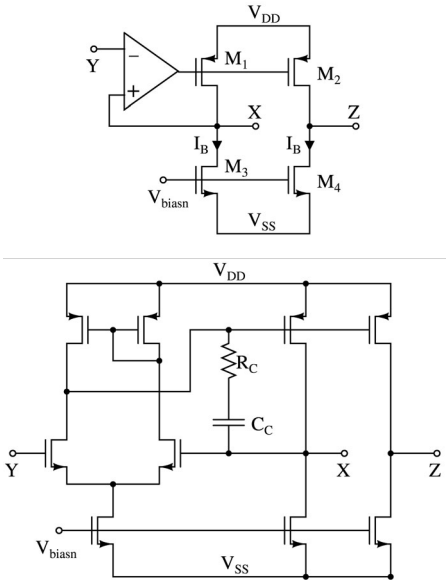

Fig. 9. Simplified schematic of Liu's current conveyor.

The X terminal resistance may be determined from the small signal model of the input stage, illustrated in Fig. 10.

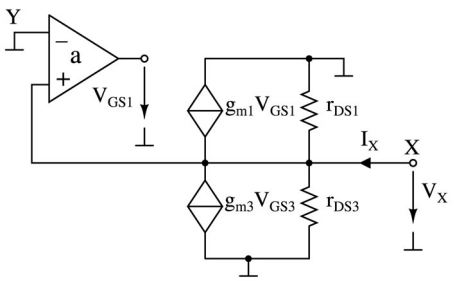

Fig. 10. The small signal model used to calculate R_X.

The calculations yield

$$R_X = \frac{V_X}{I_X} = \frac{r_{DS1} \,\|\, r_{DS3}}{a\, g_{m1}\left(r_{DS1} \,\|\, r_{DS3}\right)+1} \cong \frac{1}{a\, g_{m1}} \tag{2}$$

The calculations show that the negative feedback helps reducing the small signal R_X to hundreds or even tens of Ω-s. However, the non-linear expression of R_X becomes increasingly important when considering the large signal behaviour. It can be demonstrated that the incremental current flowing through the X terminal exhibits a parabolic dependence on the voltage at the X terminal, according to (3), where a is the gain of the differential amplifier, β_p is the intrinsic transconductance of the p-channel transistor M_1 and I_B is the bias current of the X terminal input stage [7].

$$I_X = 2a\sqrt{\beta_p I_B}\cdot V_X - \beta_p a^2 V_X^2 \tag{3}$$

This equation shows that the non-linear R_X introduces even order harmonics and it may be considered the main source of nonlinearity in CCII based circuits. Using fully balanced circuit architectures effectively cancel even order non-linearities. Therefore, when the differential signal paths are matched, the OTA has the potential for very linear operation along with relatively low current consumption. The Z terminal output resistance may also be enhanced by using cascoded transistors. The structure of the fully balanced OTA is presented in Fig. 11.

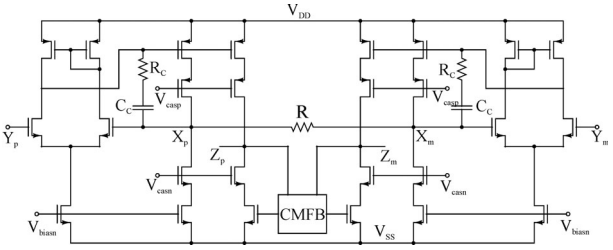

Fig. 11. The fully balanced OTA with cascode output stage.

4. Simulation Results

The simulations performed on the filter at transistor level have the main goal to demonstrate the functionality of the circuit in the presence of the inherent non-idealities, compared to the concept level implementation in [6]. The main emphasis here lays on the performance indicators concerning frequency and order variability, non-linearity and a dynamically adjustable current consumption.

The corner frequency programming strategy implies changing the transconductances through a binary weighted current amplifier in the CCII output stage according to (4). In this equation 4 MHz is the lowest achievable corner frequency, R is the termination resistance of the network and b_i are the programming bits of the weighted current amplifier.

$$f_t = 4MHz \cdot \frac{\sum_{i=1}^{4} b_i \cdot 2^i}{R} \tag{4}$$

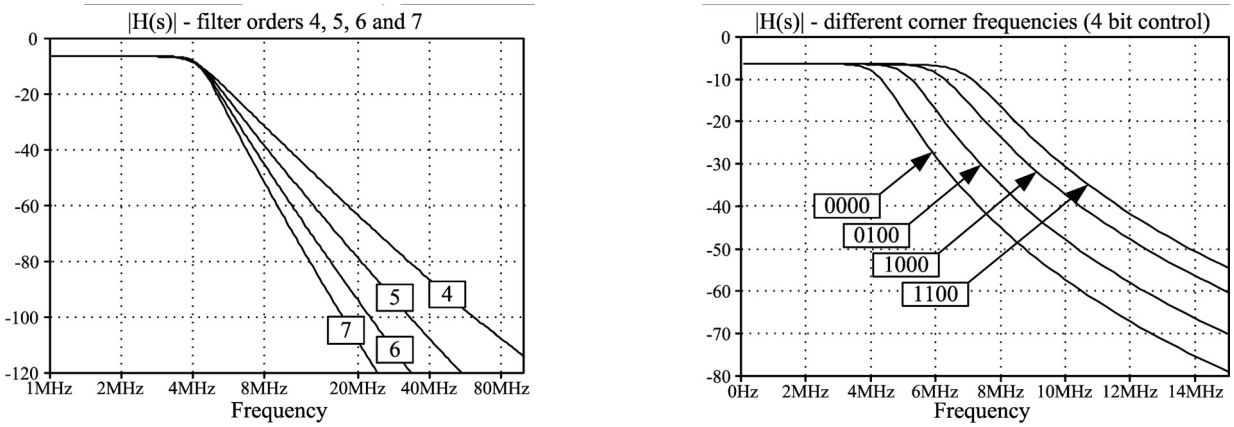

Fig. 12. The filter magnitude response for different orders and corner frequencies.

Fig. 12 shows the magnitude response of the filter, designed for the lowest possible corner frequency equal to 4 MHz, standard Butterworth approximation, orders 4, 5, 6 and 7, various programming codes and corner frequencies.

The linearity of the filter has been extensively simulated for all the corner frequency-order combinations. The frequency of the input signal has been chosen 250 kHz, such that the lowest ten harmonics lay in the filter pass band. The worst-case total harmonic distortion was approximately – 53 dB for a 1 V peak-to-peak differential input sine wave. Fig. 13 shows the typical output spectrum of the filter and the higher order harmonics for the 6th order configuration.

The built in power down algorithm allows the dynamical reduction of the filter consumption when the order is lowered. The complete 4th order filter draws 8.4 mA from a single 3 V supply, while the 7th order configuration draws 13.6 mA. The consumption has been measured for the highest possible corner frequency, when all the branches of the programmable output stage are functional and correctly biased.

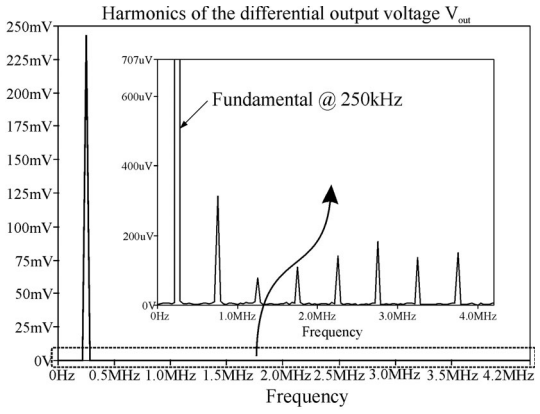

Fig. 13. Distortion measurement of the 6th order filter – 1V peak-to-peak input at 250 kHz.

5. Conclusions

The reconfigurable low pass filter described in this paper is suitable for integration into multi-mode receiver front-ends that employ a form of direct conversion architecture. The modular design is easily scalable, allowing the extension to higher orders and wider programming range of the corner frequency by simple replication of the fundamental reconfigurable module. Furthermore, the circuit can be extended to implement a polyphase band pass response, adapting the transfer function to the needs of other receiver configurations, such as the low-IF architecture. The simulations performed at transistor level have proven the functionality of the reconfiguration concept. The filter achieves good performances in terms of linearity and features dynamically adjustable current consumption. In all the cases the consumption is lower compared to classical OTA-C implementations with similar linear range.

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