SPECIAL ISSUE SECTION

AH/EHW - the State of the Art and the Prospectus for Future Development

Editors:

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Editorial

Special issue section on

AH/EHW - the State of the Art and the Prospectus for Future Development

With great pleasure, we would like to welcome you to this Guest Invited Issue of the *JAMRIS - Journal of Automation, Mobile Robotics & Intelligent Systems*. The motivation of its selected topic - *AH/EHW - the State of the Art and the Prospectus for Future Development* is deeply justified. Bio-Inspired Computing Technologies led to the spectacular progress of the Computational Intelligence (CI) nowadays and to its implementations in form of the Hybrid Intelligent Systems (HIS). Evolvable Hardware (EHW) has emerged as a novel and highly diversified technology and paradigm supporting the design, analysis and deployment of the high performance intelligent systems. The intellectual landscape of EHW is enormously rich. The discipline of EHW brings together hardware implementation of the main technologies of CI including fuzzy sets, neural networks, and evolutionary optimisation. But EHW systems use more than just the three broad areas mentioned above. They also cover novel areas as Artificial Immune Systems and DNA computing. The strength of EHW hinges on the synergy between these technologies supported by the advanced analogue and digital programmable circuits. This synergy helps exploit the advantages of the contributing technologies while reducing their possible limitations. The advanced programmable circuits confer the suitable hardware environment for a CI implementation from day to day more close to the intelligence of a human being.

Nevertheless, it is hardware implementation of the most benefit for the society and indeed most revolutionizing application of E*volutionary* C*omputation* (EC) by leading to the so-called E*volvable* H*ardware* (EHW). These new EC based methodologies make possible the hardware implementation of both genetic encoding and artificial evolution, having a new brand of machines as a result. This type of machines is evolved to attain a desired behaviour that means they have a *behavioural computational intelligence*. There is no more difference between adaptation and design concerning these machines, these two concepts representing no longer opposite concepts. A dream of technology far years ago currently became reality: adaptation transfer from software to hardware is possible by the end. Much more, the electronics engineering as a profession was radically changed: the most based on soldering assembling manufacturing technologies are largely replaced now by programming circuitry-based technologies, including EHW technologies.

EHW is a special case of the adaptive hardware, namely being strongly related to the Adaptive Systems (AS) and the Adaptive Hardware (AH). The progress in EHW is rapid. The individual technologies evolve quite quickly paving a way to new interesting and truly amazing applications. In the heart of all of those is the principle of hybridisation. EHW is suitable for the dramatic changes that happen in the relation between hardware and the application environment. This is in the case of malicious fault/defects and need for new emergent functions that claim for in-situ synthesis of a totally new hardware configuration. It is not surprising at all witnessing a lot of activities and achievements within this realm included on the agenda of high tech organizations as NASA or ESA.

The application developer may meet different design tasks to be evolved. As the case, the design to be evolved could be: a program, a model of hardware or the hardware itself. Algorithms that run outside the reconfigurable hardware, mainly feature the actual EHW state of the art, but also some chip level attempts were done. It is important to understand that *evolutionary circuit design* and *evolvable hardware* (EHW) are two different and distinct approaches. *Evolutionary circuit design* performs the evolution (the design) of a single circuit. The aim is typically to design novel implementations that are better (in terms of area, speed, power consumption) than conventional deigns and/or to design circuits with additional features such as fault-tolerance, testability, polymorphic behaviour, that are difficult to design by conventional methods. E*volvable* h*ardware* (EHW) involves an EC responsible for continual adaptation. EHW is applied to high-performance and adaptive systems in which the problem specification is unknown beforehand and can vary in time.

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In the first paper, Oltean, Hintea, Sipos are focussed on new a method for analogue circuit design optimisation. Design objectives can be expressed in a flexible manner by using fuzzy sets. Neuro-fuzzy systems (universal approximators) are used to model the complex multi-variable and non-linear circuit performances. The exploration of the large, multidimensional solution space in quest for the optimal solution is done by an efficient and robust genetic algorithm avoiding local minima. This was tested and validated by application to the design optimisation of a CMOS amplifier.

The second paper by Negoita, Sekanina, and Stoica is an overview on the Evolvable Hardware (EHW) the exciting and rapidly expanding industrial application area of the Evolutionary Computing (EC), of the Genetic Algorithms especially. An overview is made on the outstanding technological support making possible the implementation of system adaptation in hardware. Different kind of programmable circuits arrays are introduced. The most known EC based methods for the EHW implementation are described. A main part of this paper deals with some concrete elements of the EHW design, including the current limits in evolutionary design of digital circuits. Practical concluding remarks for the practitioners with regard to future perspectives of the area are an integrant part of this paper.

Csipkes G, Hintea, Csipkes D, Rus, Festila and Fernandez-Canque deal with a reconfigurable and programmable analog low pass filter for low voltage wireless applications. The proposed filter may be used for channel or band selection in multi-mode receiver front ends employing direct frequency conversion. The circuit has been synthesized using state variables and leapfrog OTA-C techniques, features programmable order, digitally variable frequency parameters and wide linear range. The fundamental OTA cell has been implemented with fully balanced second-generation current conveyors, suitable for operating with low supply voltages. The functionality of the design has been demonstrated by transistor level simulations based on an 180 nm digital CMOS technology.

A linear Support Vector machine classifier is proposed in this paper. In SVM linear classifiers architectures based on multiplying laws the main building blocks are multipliers. Festila, Szolga, Groza, Hintea, Cirlugea treat this approach. Using a model consisting of a compound of two inverse non-linear functions develops the multiplying and weighting cells. The procedure is fitting the VLSI implementation by use of simple nonlinearized standard log-domain or DA cells that compensate each other nonlinearities to obtain an extended domain of operation. Current-mode ELIN (externally linear internally nonlinear) design is used for its low voltage, low power and high speed characteristics. The resulted parallel-serial classifier was simulated taking into account real parameters of transistors in BICMOS technology.

In the fifth paper, Kirei, Topa, Neag, Onet are focused on some aspects regarding the design process of the low-IF receivers. They present an I/Q imbalance image interference - compensation algorithm based on neural networks that is suitable for low-IF receivers.

The standard solution using a complex LMS adaptive filter, which separates the desired, and image signals is limited in that the recovered signal remains affected by the I/Q imbalance, a drawback that is corrected by the proposed method. The functionality, convergence and stability of the neural network based filter are demonstrated through extensive computer simulations.

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