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# Designing high speed FPGA systems with close relation to physical domain

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**Abstract**

In real system design, when FPGA technology is used for high performance DSP computing, to short design time and prohibit any critical error in hardware prototype there is the need to explore system level approach and detail physical level verification at the same time. In this article author presents a design environment built to design some kind of radar systems. Characteristic in this approach is great care given to guarantee possessing from and generating signals to the real environment.

**Keywords**: FPGA, DSP, RF systems.

## Projektowanie systemów FPGA przetwarzania szybkich sygnałów w ścisłym powiązaniu z warstwą fizyczną

**Streszczenie**

Projektowanie systemów technicznych, przetwarzających sygnały szybkie (częstotliwości radiowe) jest zadaniem trudnym i wymagającym złożonego onarzędziowania. Użycie reprogramowalnych tablic logicznych FPGA w roli wysokowydajnych elementów cyfrowego przetwarzania sygnałów staje się obecnie standardem. Aby skrócić cykl projektowy i wyeliminować ryzyko zaistnienia krytycznych błędów prototypu potrzebne jest zastosowanie projektowania na poziomie systemu, z koniecznością jednoczesnej, szczegółowej i w pełni wiarygodnej weryfikacji na poziomie warstwy fizycznej. Przedstawiony w publikacji zestaw narzędzi programowych i przyrządów pomiarowych, zdaniem autora, daje możliwość spełnienia wyżej zarysowanego postulatu. Postulat ten sam w sobie nie wydaje się wszakże oryginalny, zwarzywszy jednak na postęp technologiczny, pewne istotne tendencje z tym związane warte są omówienia. Przedstawiony, jako przyczyna dyskusji, zestaw stanowiska badawczo-rozwojowego przewidziany jest do realizacji badań przemysłowych oraz prac rozwojowych w zakresie konstruowania określonej klasy radarów.

**Słowa kluczowe**: rekonfigurowalne tablice logiczne, cyfrowe przetwarzanie sygnałów, systemy radiowe.

## 1. Introduction

Historically, in science and engineering, the reductionism was used as general methodology. Scientific or design problem of any complexity was always decomposed into smaller components and those subcomponents where investigated/developed individually, apart from each other. After that process all subcomponents were integrated into original complexity scale. It was satisfied methodology at the era of Newton or Descartes (16/17 century), but at 40's of 20$^{th}$ century it was obvious that decomposition as the methodology is, however intuitive, but no longer useful [1]. And, only holistic approach is acceptable where all system components are evaluated simultaneously and trade-off decisions, concerning any individual subsystem, are correlated with all other subsystems current specification continuously. This methodology is known as System Engineering [2], has been defined, developed and used for over 60 years. First effective step into direction of this kind of thinking can be illustrated by the appearance of British radar system of 1940 (there was a symmetry on the German side at the same time, but details are less known). Professor of Manchester University P.M.S. Blachett formed a team of army officer, basic physics specialist, 2 of mathematical physics, and 6 of other specializations members (mathematics, physiology, and earth science), covering very wide spectrum of specializations. All under demand of air defense criticized the problem. It is assumed that it was the moment of operational research methodology appearing.

System Engineering (SE), as methodology, was not very popular to support science effort or even engineering. Even now there are misunderstandings on that field. Probably, the reason is that SE is characteristic for big companies of aviation and/or military and usually overloaded by formal procedures of Project Management techniques. Industry brunches of this kind are most methodologically and technologically advanced for obvious reasons and are rather hermetic. From high education point of view it depends on what is the industrial level in a country. Scientists in education are willing to make copies of their self rather than prepare engineers for the industry.

Originally, SE was the domain of mechanics and electro-technology so; some standards in thinking and tooling were made before era of microelectronics and computing technology. The example: co-design as the problem was recognized about 1985 [3], but this way of thinking was obvious long before in SE. In other words, co-design was introduced rather late, and the source of inspiration was derived from embedded system development bottlenecks observations, not from SE. Conclusion may be; that a lot of time and money has been lost until the holistic methodology was re-invented in form of co-design in emerging brunch of microprocessor based embedded technology.

In the electronic industry last 10 years have been characteristic of system level approach, known as Electronic System Level (ESL) [4]. ESL is recognized of higher abstraction levels than it was used for software or hardware design separately. In fact, this higher abstraction level it is a way to postpone for later hard effort to resolve critical, detailed design dilemmas of lower abstraction levels during a design process. Especially, Transaction Level Modeling (TLM) allows escaping from details of inter-modular communication protocols [5]. However, ESL simplifies and makes much more easy simulation and verification and cuts design time, compared to the previous methods, also thanks to encapsulation of functional components into hardware/software independent modules, in many times ready to use IPs (Intellectual Property, like processing cores, I/O units etc.). All modules and their interconnection standards may be described using C-like languages (SystemC, as example), even more simplifying tooling aspects of ESL methodology (however does not guarantee useful results).

C-like languages make ESL approach mentally friendly for traditional, procedural programmers and easer to be accepted for new generations of them. So, it looks so easy to build any electronic system of any complexity without knowing much more than programming in "C". It is also promising for the industry; it is much cheaper to employ a programmer than the experienced hardware specialist. But, mentioned before postponing of detailed problems will appear sooner or later. The knowledge of detailed issues of physical layer eventually have to be used, in other case system will stay virtual forever, no satisfied speed, power consumption, cost, reliability etc., would be ever achieved without co-verification of the physical domain during design steps.

Creating co-design methodology we wanted to cover the gap between programmers and hardware designers, but creating ESL we can generate much greater gap where more abstractive thinking programmers of new generations would be much more far from hardware designers than ever before.

In this paper there is a solution presented for the real problem solving for the industry – some kind of radar technology. There is no room for many attempts because the real product must be introduced on time to the market (EU Structural Funds in Poland). Proposed solution is conservative enough to relay on proven methods and tools, but also, innovative at the same time to get profits of using the latest and most advanced technology. Matlab/Simulink is used as design entry and modeling ESL platform, well known and verified toolset (for wireless and software defined radio [6, 9], radar technology [7] and generally, for DSP applications [8]). FPGA technology is used for any logic and computing functions, at the development stage and in final product application.

General consideration introduced here serves as the background for more detailed description (section 2) about tool and measurement devices used in R&D project referenced in this paper. In section 3 methodological aspects and the design flow is discussed. Finally, section 4 concludes all aspects mentioned through all the work.

## 2. Tools and measurement devices

Figure 1 presents the general view of the RF-system-in-FPGA research and developments stand. For real signals observation of the physical domain (PHY) Digital Spectrometer Analyzer was used, (DSA) of RSA3000B series from Tektronix. This device is able to capture and visualize RF signals both: in frequency and time domains. This feature is extremely useful for Ultra Wide Band (UWB) technology, for example. Thanks to advanced DSP computing embedded, the spectrometer is able to extract and correlate particular features of a signal. Periods of signals can be stored internally and then off-line processed out of the device; there is dedicated software tooling available.

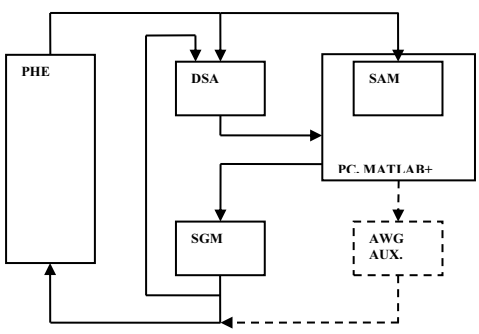


Fig. 1. Block diagram of the RF-system-in-FPGA R&D stand. Where: DSA – Digital Signal Analyzer, SAM – Signal Acquisition Module, SGM – Signal Generation Module, AWG AUX. Auxiliary Arbitrary Waveform Generator, PHE. - Physical Environment, PC and MATLAB+ are standard PC with Matlab/Simulink and other appropriate software packages

Rys. 1. Schemat blokowy stanowiska badawczo-rozwojowego dla systemów radiowych implementowanych w FPGA. Oznaczenia skrótów: DSA – cyfrowy analizator sygnałów, SAM – moduł pozyskiwania sygnałów, SGM – moduł generowania sygnałów, AWG AUX – dodatkowy generator przebiegu zadanego, PHE – komponenty otoczenia fizycznego, PC oraz MATLAB+ to standardowy komputer klasy PC wraz z oprogramowaniem Matlab/Simulink i innymi, współpracującymi pakietami oprogramowania

In the presented scheme it is very important that those data blocks of intervals of selected signals acquired by the spectrometer are then transferred into Matlab environment. Thanks to that link abstract Matlab models may be stimulated directly with information derived from signals of the real world.

The second device (Signal Acquisition Module – SAM), also capable to acquire real signals, it is PCIe expansion board, type X5-400M from Innovation Integration Inc. This board, being controlled by a standard PC, can sample signals with 500MHz frequency and 16-bit resolution. It is based on the Virtex-5 FPGA chip from Xilinx Inc. and is supported with dedicated library module integrated with Matlab environment. Data acquired by the board can also be used to stimulate Matlab models.

Based on reconfigurable FPGA, board can not be used to acquire data only, but any DSP computing (limited by resources) can be executed there during prototyping. Dedicated DSP functions are eventually implemented using Xilinx ISE synthesis tools preceded with Xilinx AccelDSP Synthesis Tool, System Generator and FPGA Matlab modeling for synthesis (complete tooling chain it is MATLAB+ on the Figure 1).

Another Virtex-5 board (type: Virtex-5 FPGA ML506 Edition) is used as Signal Generation Module (SGM), radar signals are generated this way. Signals are modeled and appropriate hardware modules are prepared also in Matlab environment. But, the verification loop of generated signals is not limited to the loop closed inside Matlab environment only. Verification of generated signals can be done any time by connecting SGM output directly to the input of DSA. Thanks to that signals can be observed as real in frequency and time domains, can also directly stimulate Matlab models of FPGA blocks of SAM.

On Figure 1 there is also showed Arbitrary Signal Generator (AWG), of AWG7000B series (Tektronix). This device is an option, not yet used because of project cost limitations. This option, however, would be very valuable because AWG can be programmed directly from Matlab and signal waveforms are available immediately on its output. Now, these signals have to be generated in SAM, it consumes more time of preparation and limits the flexibility. Positive aspect of the situation is, that only these signals which are possible to generate in FPGA can be evaluated, as required for the final product implementation.

## 3. Methodology and design flow

The design flow starts with test pattern generation model built in Matlab environment (Figure 2). Signals of the test pattern can be, and should be, verified with the use of DSA before real components of PHE may be included. Internal verification loop processed in Matlab environment uses abstract models of PHE components. After positive verification of abstract models, physical components of PHE may be connected. Test pattern generation model is then synthesized and down-loaded into FPGA based SGM (or AWG, alternatively can be used before prototyping). Radio frequency signals generated in SGM are available on its power amplifier output (extra added to the original board). These signals are led to PHE components (up-converters, antennas, etc.). SGM with DSA connection creates the external (out of Matlab) loop of the physical verification. So, abstract models of the test pattern generation can be analyzed for the physical implementation correctness. SGM-DSA-MATLAB+ loop can be used until investigation results are satisfied and the pattern generated follows assumed constraints.

Multi-loop simulation and physical verification before real PHE components are used, is critical because eliminates as much as possible uncertain assumptions about physical properties of PHE. Abstract models of PHY are usually not accurate enough and some properties may by missed or mismatched. So, external verification loop with PHE components serves also for verification of research hypothesis. Eventually, the abstract model of PHE will be refined and precise enough to continue development on simulation bases.

Having evaluated acceptable model of PHE and verified some physical properties of SGM implementation, on the way to build physical prototype, there is the need to add SAM into the development process. In fact, SAM implements selected functions available already in DSA, but in embedded form and with ability of automatic recognition predefined signal patterns in time. This observation was the base of the presented configuration of R&D stand. SAM with its tooling environment offers great flexibility of evaluation implementation attends. First, Matlab abstract models are evaluated for SAM, similarly as for SGM before, and then these models are implemented in FPGA on board to be verified in the physical domain.

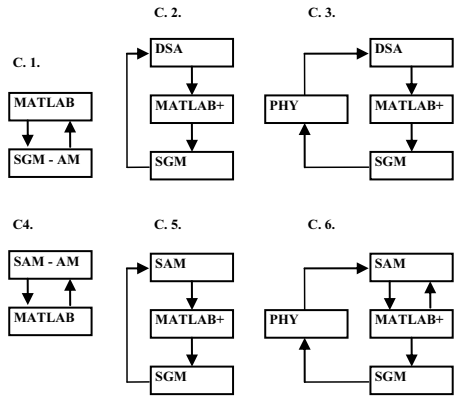


Fig. 2. Design flow block diagram. Where: C.1. Internal simulation loop for SGM abstract models (AM) evaluation, C.2. SGM models synthesized and externally verified with the use of DSA, C.3. Components of PHY models final refinement external loop, C.4. Internal simulation loop for SAM abstract models, C.5. SAM models synthesized and externally verified with the use of SGM, C.6. Final refinement external loop of SAM synthesized models completed with PHY components

Rys. 2. Schemat blokowy procesu projektowania. Oznaczenia: C.1. Pętla symulacyjna abstrakcyjnych modeli (AM) SGM realizowana wewnątrz środowiska Matlab, C.2. Zewnętrzna pętla weryfikacji syntezowanych modeli SGM z użyciem SAM, C.3. Pętla zewnętrzna ostatecznej weryfikacji ulepszanych modeli PHY, C.4. Wewnętrzna pętla symulacyjna modeli abstrakcyjnych SAM, C.5. Zewnętrzna pętla weryfikacji syntezowanych modeli SAM przy użyciu SGM, C.6. Zewnętrzna pętla ostatecznej weryfikacji syntezowanych modeli SAM uzupełniona elementami PHY

## 4. Conclusion

The history tells us that in spite of so great recourses of knowledge available there are important obstacles of gaining enough synergy of scientific/technological brunches differentiations. Most probable reasons are: overwhelming volume of knowledge and specialization tendency as the result of ever growing competition. Other reasons may be: directed and constrained by the higher education background and terminology or specific methods and tooling applied for a brunch. The last worth to mention reason it is the human mentality; it is extremely difficult to work-out unified, interdisciplinary approach for science or/and engineering by a person being already involved in strictly scheduled professional activities.

When a real system is developed there is no way to avoid interdisciplinary R&D problems. If it is innovative project there always can be found quite a lot of scientific aspects. It is characteristic, regardless of how big is an organization responsible for that, it may be corporation or SME (Small Medium Enterprise). For bigger organizations and big projects (airplanes, cars) it is the problem of building a team (or corporation of teams, or structure of organizations) of specialists of different brunches, and complete it with someone who is able to interdisciplinary coordinate a project. For smaller organizations individual persons of interdisciplinary knowledge and skills have to be found, and it is much more difficult.

However, EDA with ESL methodology may play similar role as some time ago FPGA technology appearance; in fact, removing ASICs as economical barrier for SME. The significant methodological gap (economically dictated) between big and small companies can be buried gradually with the EDA progress. Smaller teams or even single specialists being armed with automated, interdisciplinary methodology and tooling can do the same as big teams with great money, before. It may be smaller scale, but with complete spectrum of scientific/technological differentiations.

In this paper the author presents results of the initial phase of "EU Structural Funds in Poland" type project, started in January 2009. Having limited resources of funding and professionals available (SME) there was the must to use in R&D process most advanced tooling and methods of a moderate cost. As it was mentioned before, radar technology was created in the II World War by the interdisciplinary team and the must of survival paradigm. Next decades proved that radar technology was domain of big industries with good financial condition, having rather long R&D phases. If described project succeeds it would be the exception of this rule, in spite of crisis surrounding at this moment (some kind of "must of survival"), and thesis of this paper would be proved this way.

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