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Multi-core Audio Decoding System Based on Networks on Chip Architecture

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Abstract

A heuristic core mapping dedicated to multi-path routing algorithm for mesh Network on Chip dedicated to popular stream-based audio decoder algorithms is proposed. The processing units performing stages of a number of decoders are mapped into 2D mesh nodes in order to balance and minimize the bandwidths of the structure links. The experimental results confirming the benefits of the proposed approach are provided.

Keywords: Network on Chip, multi-path routing algorithms, core mapping techniques.

Wielordzeniowe dekodowanie strumieni dźwiękowych opartych o architekturę sieci wewnątrzukładowych

Streszczenie

W artykule przedstawiono heurystyczny algorytm odwzorowywania aplikacji zdominowanych przez dane do struktury dwuwymiarowej sieci wewnątrzukładowej. Jednostki przetwarzające są odwzorowywane do sieci NoC w sposób zmniejszający i wyrównujący przepustowości magistral wewnątrzukładowych. Do wyznaczania tras użyto wielościeżkowego algorytmu routingu. Badania eksperymentalne potwierdzają zasadność proponowanego podejścia.

Słowa kluczowe: Sieci wewnątrzukładowe, wielościeżkowe algorytmy routingu, techniki odwzorowywania rdzeni.

1. Introduction

One of the promising candidates for future generation of chips implementing streaming multimedia applications are Multi-Processor Systems on Chips (MPSoCs) [1]. However, nowadays popular MPSoCs realizations, based on buses or point-to-point connections (P2P) are reported to scale badly with the growth of the number of intellectual property (IP) cores in a single chip [5]. It is one of the motivations of introducing the Network-on-Chip (NoC) approach, where the IP cores are connected each other by means of a network resembling the well-know, macroscopic computer networks. It has been demonstrated in [4] that the NoC contention level is lower than in the realizations with a bus and only slightly worse in comparison with the P2P connections. However, the target chip area while using the P2P approach is much higher.

For one important class of algorithm the typical NoC-based chip architecture synthesis is of worse performance [3]. Multimedia streaming applications do not adapt to the temporary data-flow and even two data-flows transmitted by a single link result in contention. The transferred streams are fixed for relatively long time and thus it is impossible to make up for the delay cased by the contention in the subsequent stages [6].

The contention level, however, may be decreased while the algorithm stages are mapped into the NoC mesh using certain permutations. Thus we decided to develop a heuristic that would generate a mapping permutation of stages for a given set of audio decoder algorithms. The heuristics is meant to generate the core permutations which, after mapping into a mesh structure, would balance the transfers between the cores and decrease the overall bandwidth of the links in the structure.

In this paper, the proposed approach is applied to an MPSoC realizing more than one streaming algorithms at once. Such multi-algorithm chips are increasingly popular due to, e.g., the numerous audio/video standards existing in many end-user applications. We decided to test our approach with an NoC-based MPSoC realizing three audio decoders (AAC, MP3 and OGG).

2. Routing Issues

The motivation of our work has arisen when we tried to utilize NoC routing algorithm, so called tapeworm, introduced in [2], to various video streaming codecs and obtained promising results in terms of minimal bandwidth, links utilization balance and routing efficiency [3]. So, we decided to apply our multi-route algorithms for audio decoders so as to obtain a multi-cores chip model that realizes a number of popular audio decoding tasks at once. In the tapeworm routing algorithm a package body is split into segments that are comprised of a number of smaller units of constant length, named flits (flow control units). The algorithm is to be applied after the mapping stage, i.e., when all the IP cores have been mapped into a NoC structure.

In order to determine the appropriate core mapping, i.e., the mapping of the nodes from flow networks realizing subsequent stages of the algorithm that leads to the minimal value of the transfers between cores while using the tapeworm algorithm, it is possible to use an exact algorithm. Due to the computational complexity $O(n!\cdot n^2)$, it can be reasonable applied only to the NoC mesh of the size up to 3x3 cores. So it is practically impossible to apply this approach to a model implementing more than one decoder.

The simplest approach for mapping a set of IP cores, the dividing and conquer method, when the cores are mapped independently for each algorithm and then placed next to each other, as presented in Fig. 2a does not lead to the promising results, as it is presented in the next section. This is caused with the fact that in the tapeworm routing it is important to create as many paths as possible between nodes transferring large portion of data to each other, whereas the distance between these nodes is of lower importance. In Fig. 1 we propose a heuristics that, according to our experimental results, leads to quite promising core mappings while applied to the NoC utilizing the tapeworm routing scheme. We start our algorithm with a generating a population of random core permutations to be mapped into the mesh structure.

The algorithm is iteratively run as long as the maximum number of generations has not been met, or the resulting transfers are constant for a specific number of iterations.

```
1. select randomly an item from NoC transfers table between src and dest
2. d0 ← calculate Manhattan distance between src and dest cores
4. (d1, d2, d3, d4) ← calculate Manhattan distance
                                between src and all neighbors of dest
5. if(min(d0, d1, d2, d3, d4) ≠ d0)
6.          nmin ← neighbor with the lowest distance
7.          swap (dest, nmin)
```

Fig. 1. Pseudo-code of mapping algorithm
Rys. 1. Pseudokod algorytmu odwzorowania rdzeni

3. Experimental Results

In Fig. 3 three histograms, for AAC, MP3 and OGG codecs, are presented. These histograms inform about the instance of the proposed iterative algorithm where the minimal value of the bandwidth has been obtained. In all cases, the optimal value has been reached in a relatively early stage. The outstanding graph for AAC means that this algorithm the most suitable for our technique due to the linear structure of its flow graph; the flow graph of the remaining two decoders include a number of additional branches. As a result, the mapping of these two algorithms into a regular 2D-mesh is more sophisticated and requires more iterations. However, in all three benchmarks the results were quite promising: in the first 50 iterations the minimal bandwidth has been obtained in 33%, 41% and 99% for OGG, MP3, AAC, respectively.

Next, we combined these three audio decoders in a single 4x4 NoC mesh. Having executed the algorithm provided in Fig. 1, the locally minimal result have been obtained for the mapping presented in Fig 2b, where the cores of the AAC, MP3 and OGG decoders, with indices: 0-5, 6-11, and 12-15, respectively. In comparison, we provided an example of the regular core structure in Fig 2a. The link bandwidth of the regular structure mapping is equal to 58334 bps, whereas the mapping generated with the proposed technique equals 48837 bps, which is 16 per cent lower.

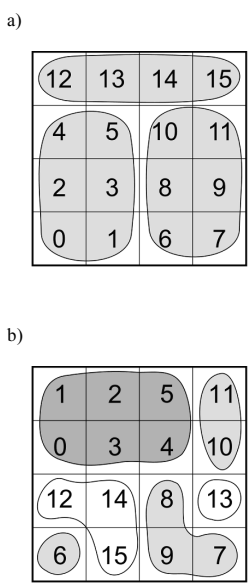

Fig. 2. Example of core mapping for three decoders (AAC, MP3, OGG) unsuitable (a) and suitable for the proposed routing algorithm (b)
Rys. 2. Przykłady odwzorowania rdzeni dekoderów (AAC, MP3, OGG) o większej (a) i mniejszej (b) przepustowości przy zastosowaniu algorytmu routingu

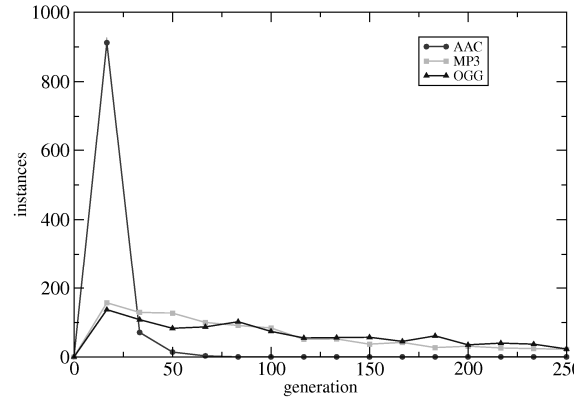

Fig. 3. Indices of generations with minimal transfers for considered decoders
Rys. 3. Numery generacji, w których osiągnięto minimalną przepływność rozpatrywanych dekoderów

4. Conclusion

In this paper, we have presented an approach for mapping data-dominated algorithms, such as audio decoders, into a 2-D mesh NoC architecture. We have demonstrated that the multi-path routing scheme with the proposed mapping heuristic algorithm is more suitable for this kind of algorithms than the intuitive regular distribution of the processing cores of different decoders.

The proposed heuristics leads to minimal results in relatively early iteration – in the first 100 iterations we obtained the minimal solutions in 76% average cases for the considered audio decoders. The obtained results confirm the advantage of the proposed routing and mapping techniques in the NoC domain.

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