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Log signals simulation

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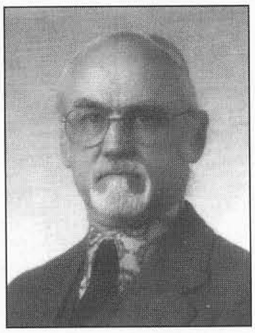

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Abstract

Log simulators (log – a device for measuring speed in marine navigation) should possess a pulse output – a given number of pulses per nautical mile. These are digital to frequency converters, in the form of digitally programmable frequency dividers, which are widely known, but in this applications they are required to achieve rather special features. Due to a hyperbolic relationship between the pulse repetition period and speed they should be able to generate a wide range of periods (e.g. 0.09 s – 360 s and further to ∞ with resolution up to $9\cdot10^{-5}$ s) and should achieve a fast and undisturbed change of period at simulated speed manoeuvres and simulated speed errors. In this paper equations for design parameters are derived and the solution of period change problem is provided.

Streszczenie

Symulatory logów (urządzeń mierzących prędkość w nawigacji morskiej), które używane są do testowania oraz szkolenia operatorów radarów i systemów antykolizyjnych, powinny posiadać również wyjście impulsowe, które w logu rzeczywistym pochodzi z licznika przebytej drogi, w postaci zadanej liczby impulsów na milę morską. Urządzenie takie to przetwornik cyfrowo-częstotliwościowy w formie programowanego cyfrowo dzielnika częstotliwości. Przetworniki takie są powszechnie znane jednak w tym zastosowaniu spełniać muszą dość specjalne wymagania. Ze względu na hiperboliczną zależność okresu impulsów od symulowanej prędkości muszą generować okresy powtarzania impulsów w szerokim zakresie (np. 0,09 s – 360 s i dalej do ∞ z rozdzielczością do $9\cdot10^{-5}$ s) oraz zapewniać szybką i niezakłóconą zmianę okresu przy manewrach prędkością symulowaną oraz symulacji błędów tej prędkości. W artykule wyprowadzono zależności na parametry projektowe symulatora oraz przedstawiono sposób korygowania okresu powtarzania impulsów.

Keywords: digital to frequency converters, marine navigation, marine simulators
Słowa kluczowe: przetworniki cyfrowo-częstotliwościowe, nawigacja morska, symulatory morskie

1. Introduction

Contemporary logs provide a digital output for external devices in NMEA standard but, from times of electromechanical logs, an output from log's distance counter in the form of k (e.g. 100, 200, 400) pulses per nautical mile is also commonly used.

The log simulators, as a part of radar simulators, are used for testing or training purposes of radars and ARPA systems (an acronym from Automatic Radar Plotting Aid), and should provide both capabilities. This paper is aimed towards the pulse part of the log simulator, which seems to be simpler but in fact is more difficult in realization as it will be shown.

2. Derivation of equations for frequency and period of pulses

K pulses per nautical miles means k·V pulses per hour
- where: V – speed [knots = n.m./h]
therefore

$$f = \frac{kV}{3600} \tag{1}$$

where: f – frequency of pulses [1/s = Hz]
whereas

$$T = \frac{1}{f} = \frac{3600}{kV} \tag{2}$$

where: T – pulse repetition period (prp) [s].

3. Design requirements

The log simulator is a microprocessor controlled digital device and it looks like a classical digital to frequency converter, but there exist some design difficulties.

Each log simulator should have assumed required performance parameters such as:
- V_{min}, V_{max} – minimum and maximum simulated speed,
- ΔV – speed resolution,
- k_{min}, k_{max} – range of k factors.

From equation (1)

$$f_{max} = \frac{k_{max} V_{max}}{3600} \tag{3}$$

$$f_{min} = \frac{k_{min} V_{min}}{3600} \tag{4}$$

A digital to frequency converter can be in this application a digitally programmable frequency divider, which divides a generator frequency f_{gen} by a divisor loaded from a controlling microprocessor to a memory register and to a counter (Figure 1). The counter counts generator pulses down to zero; a decoder detects this state and generates a pulse, which also reloads the counter from the memory register.

A divisor C is calculated from equation

$$C = \frac{f_{gen}}{f} \tag{5}$$

and after substitution equation (1)

$$C = \frac{3600 \cdot f_{gen}}{kV} \tag{6}$$

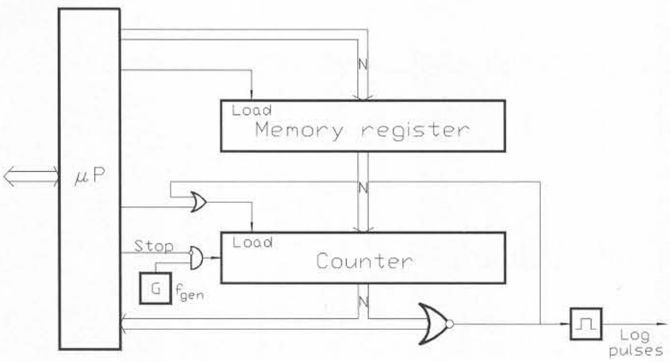

Fig. 1. Logic diagram of log simulator
Rys. 1. Schemat logiczny symulatora logu

This converter has to be able to generate a resolution in T prp related to V_{max} and $V_{max} - \Delta V$ speeds given by

$$\Delta T = \frac{3600}{k_{max}(V_{max} - \Delta V)} - \frac{3600}{k_{max}V_{max}} = \frac{3600 \cdot \Delta V}{k_{max}V_{max}(V_{max} - \Delta V)} \tag{7}$$

thus a minimum frequency of the generator is

$$f_{genmin} = \frac{1}{\Delta T} = \frac{k_{max}V_{max}(V_{max} - \Delta V)}{3600 \cdot \Delta V} \tag{8}$$

Taking into account that the longest T prp yields equation

$$T_{max} = \frac{1}{f_{min}} = \frac{3600}{k_{min}V_{min}} \tag{9}$$

than the minimum length of the binary counter, which has to simulate the longest T prp (which has to hold the biggest divisor) is obtained from

$$2^{N_{min}} - 1 = \frac{T_{max}}{\Delta T} = T_{max} f_{genmin} = \frac{k_{max}V_{max}(V_{max} - \Delta V)}{k_{min}V_{min}\Delta V} \tag{10}$$

and finally

$$N_{min} = \log_2\left(\frac{k_{max}V_{max}(V_{max} - \Delta V)}{k_{min}V_{min}\Delta V} + 1\right) \tag{11}$$

4. Exemplary log simulator

Let's assume performance requirements for an exemplary digital to frequency converter as a part of log simulator:

V_{max} = 100 knots
V_{min} = 0 knots
ΔV = 0.1 knot
k_{min} = 100
k_{max} = 400

From equation (3) f_{max} = 11.1 (1) Hz
From equation (4) f_{min} = 0 Hz
f_{min} = 0 means that no pulses are generated but the lowest frequency generated will be for V=ΔV. Hence f_{min} = 0.0027 (7) Hz
From equation (7) ΔT = 0,00009009 s = 90.09 μs
From equation (8) $f_{gen\ min}$ = 11100 Hz
From equation (9) T_{max} = 360 s
From equation (11) N_{min} = 22 bits

It should be appreciated that such a digital to frequency converter is rather special. It should generate frequency from 0, thus it should have a capability to stop generator pulses, and 22 bits dividing counter is rather very long. This is caused by a hyperbolic relationship between T prp and V speed (equation 2) and a required high resolution at high speeds in association with a very long T prp at low speeds.

5. Speed changes simulation

The simulation of speed changes is necessary for simulation of speed manoeuvres as well as the simulation of random log errors in ARPA accuracy tests.

A digital to frequency converter in log simulator is an autonomous device i.e. it receives, through a memory register, a counter contents according to equation (6) as f_{gen} frequency divisor and generates respective T prp up to time of receiving a new value.

There exist at least four solutions to change this value:

- a new value is loaded to the memory register – a new prp will be generated when the current T prp will be finished but it has to be emphasized that at low speeds a new prp will be generated even after T_{max} i.e. e.g. 6 minutes what rather cannot be tolerable,
- a new value is loaded to the memory register, and the counter is cleared – the converter generates a pulse at once at random T prp (shorter than correct), and the next one will be correct. It should be appreciated, however, that an ARPA, or another device, measures received T prp and reconstructs a speed from equation

$$V = \frac{3600}{kT} \tag{12}$$

A random T prp means random V speed, always higher than correct,

- a new value is loaded to the memory register and to the counter – the current T prp will be random (rather longer than correct) and the next one will be correct. Results as above,
- a new value is loaded to the memory register and a corrected value to the counter – the correction is done according to equations

$$C_{corr} = C_n - (C_p - C_c) \tag{13}$$

$$C_{corr} = C_{corr} \text{ if } C_{corr} > 0 \tag{14}$$

$$C_{corr} = 0 \quad \text{ if } C_{corr} \le 0 \tag{15}$$

where: C_n – value of C for a new speed,
C_p – value of C for a previous speed,
C_c – current contents of the counter.

The part in parenthesis in equation (13) represents time from the last pulse generated. The current T prp is corrected "on the fly" to a new value and the next one will also be correct. This correction can also be corrected any number of times, without random pulses, and the current T prp and the next one are always according to a new speed.

The last solution is the only proper solution but it requires access to the current value of the counter, which is not standard in typical digital to frequency converters.

It can be recommended for users of any log simulator to check which solution is used in their simulators for speed changes. Moreover the same refers to real logs which use digital to frequency converters.

6. Conclusions

It has been pointed out that the proper design of log simulators with pulse output, which seems to be very simple, requires careful attention to solve expected and unexpected problems. Ready to use equations for design parameters and for undisturbed changes of pulse repetition period as well as exemplary calculations have been provided.

Tytuł: Symulacja sygnałów logu

Artykuł recenzowany