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Stabilization of multi DC bus link voltages of multilevel NPC VSI. Application to double stator induction motors

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Voltage source multilevel inverters have become very attractive for power industries in power electronics applications during last years. The main purposes of studying multilevel inverters are the generation of output voltage signals with low harmonic distortion and reduction of switching frequency. An important issue of the multilevel inverter is the capacitor voltage-balancing problem. The unbalance of different DC voltage sources of multilevel neutral point clamped (NPC) voltage source inverter (VSI) constitutes the major limitation for the use of this new power converter. In this paper, we present study on the stability problem of the input DC voltages of the three-level Neutral Point Clamping (NPC) voltage source inverter (VSI). This inverter is useful for application in high voltage and high power area. In the first part, we remind the model of double stator induction motors (DSIM). Then, we develop control models of this inverter using the connection functions of the semi-conductors. We propose a Pulse Width Modulation (PWM) strategy to control this converter. The inverter is fed by constant input DC voltages. In the last part, we study the stability problem of the input DC voltages of the inverter. A cascade constituted by two three-level PWM rectifiers - two three-level NPC VSI - DSIM is discussed. The results obtained show that the input DC voltages of the inverters are not stable. To solve this problem, we propose to use a half clamping bridge. This solution is very promising in order to stabilize the input DC voltages of this converters.

Key words: multilevel, VSI, NPC, PWM, rectifier, clamping bridge

1. Introduction

Multilevel inverter structures provide an attractive solution for high power and high voltage applications. The multilevel topology allows application of cheaper devices in higher technology, however, the link multi DC voltage balancing problem is a serious drawback which limits the applicability of multilevel topology for motor drives. One of the major limitations of the multilevel inverters is instability of the input multi DC voltages [1]. Newly developed power components which operate in the opened and closed

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states have led to the conception of new and fast converters for high power applications. In the first part of the paper, we propose a new cascade structure for high voltage and great power applications. In the first part, we remind the model of the double stator induction motors (DSIM) [2] [3] [4]. Then, we elaborate the working model of this inverter, with no control [2] [3] [4]. In the second part, we develop the space vector modulation strategy to control the inverter [3] [4] [5]. The inverter is assumed to be fed by constant input DC voltages. In the last part, we study the stability problem of the input DC voltages of the inverter. The problem concerns the cascade structure which is constituted by two three-level PWM rectifiers - two three-level NPC VSI - DSIM [4]. The results show that the input DC voltages of the inverter are not stable. To improve the performances of the proposed cascade and stabilize the input DC voltages, we propose to uses a half clamping bridge. The results obtained confirm expected improvement.

2. DSIM model

The model of double stator induction machines (DSIM) is shown in Fig. 1.

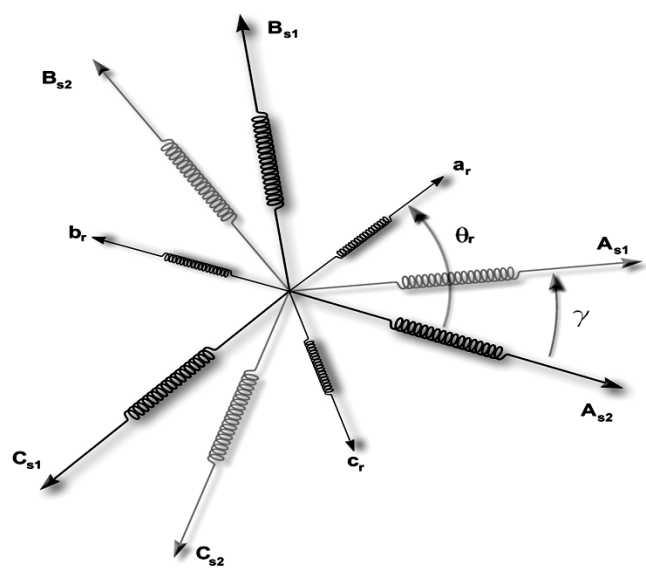

Figure 1. DSIM scheme.

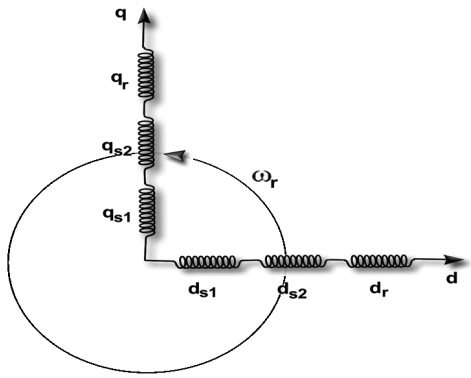

Figure 2. Representation of DSIM in the Park frame.

Park model of the double stator induction machines, with P pairs of poles, is defined by the following equations:

$$\begin{cases} V_{sd1} = r_{s1} i_{sd1} + \dfrac{d\varphi_{sd1}}{dt} - \omega\varphi_{sq1} \\ V_{sq1} = r_{s1} i_{sq1} + \dfrac{d\varphi_{sq1}}{dt} + \omega\varphi_{sd1} \\ V_{sd2} = r_{s2} i_{sd2} + \dfrac{d\varphi_{sd2}}{dt} - \omega\varphi_{sq2} \\ V_{sq2} = r_{s2} i_{sq2} + \dfrac{d\varphi_{sq2}}{dt} + \omega\varphi_{sd2} \\ V_{rd} = r_r i_{rd} + \dfrac{d\varphi_{rd}}{dt} - \omega_{gl}\varphi_{rq} \\ V_{rq} = r_r i_{rq} + \dfrac{d\varphi_{rq}}{dt} + \omega_{gl}\varphi_{rd} \end{cases} \tag{1}$$

The electromagnetic torque is given by the following expression:

$$C_{em} = p\frac{L_m}{L_m + L_r}\left[\phi_{rd}\left(i_{sq1} + i_{sq2}\right) - \phi_{rq}\left(i_{sd1} + i_{sd2}\right)\right] \tag{2}$$

The model of the DSIM in the Park frame is shown in Fig. 2.

3. Modeling of the three-level NPC VSI

3.1. Three-level NPC VSI structure

Three-phase three-level NPC VSI is a new conversion structure used to feed the high power alternating current machines with variable frequency and voltage. Several structures are possible for three-level inverters [6] [7] [8]. In this paper, we study the

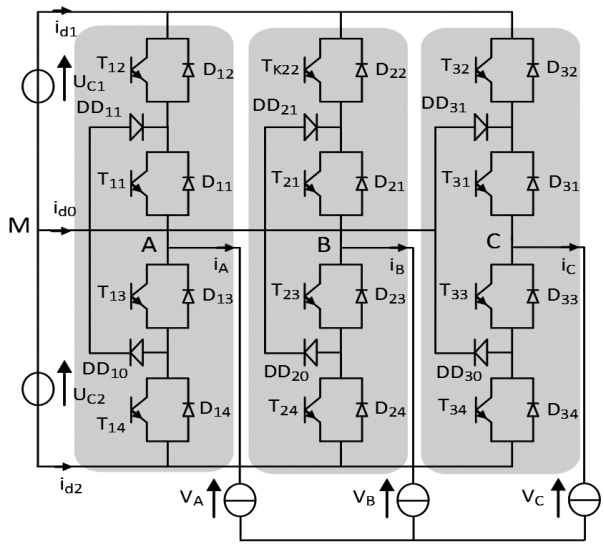

Figure 3. The three-level NPC inverter.

neutral point clamping (NPC) structure (Fig. 3). This converter is constituted by three arms and two DC voltage sources. Every arm has four bi-directional switches in series and two diodes [5].

3.2. Knowledge model

The switch connection function F_{ks} indicates the opened or closed state of the switch TD_{ks}. We define as well a half arm connection function F^b_{km} with k being the arm number.

$$m = \begin{cases} 0 & \text{for the left half arm} \\ 1 & \text{for the right half arm} \end{cases}$$

For the arm k of the three-phase three-level NPC VSI, several complementary laws controls are possible. The control law which lets an optimal control of this inverter is [4]:

$$\begin{cases} B_{k4} = \bar{B}_{k1} \\ B_{k3} = \bar{B}_{k2} \end{cases} \tag{3}$$

where B_{ks} represents the gate control of the switch T_{ks}. We define the half arm connection function F^b_{i1} and F^b_{i0} associated with the upper and lower half arms respectively. Subscript i means arm number ($i = 1, 2, 3$).

$$\begin{cases} F_{11}^b = F_{11}F_{12} \\ F_{10}^b = F_{13}F_{14} \end{cases} \quad \begin{cases} F_{21}^b = F_{21}F_{22} \\ F_{20}^b = F_{23}F_{24} \end{cases} \quad \begin{cases} F_{31}^b = F_{31}F_{32} \\ F_{30}^b = F_{33}F_{34} \end{cases} \tag{4}$$

The output voltages of the inverter relatively to the middle point M are defined as follows:

$$\begin{bmatrix} V_{AM} \\ V_{BM} \\ V_{CM} \end{bmatrix} = \begin{bmatrix} F_{11}^b \\ F_{21}^b \\ F_{31}^b \end{bmatrix} U_{C1} - \begin{bmatrix} F_{10}^b \\ F_{20}^b \\ F_{30}^b \end{bmatrix} U_{C2} \tag{5}$$

The system (5) shows that the three-level NPC VSI can be considered as two two-level voltage source inverters in series. The input currents of the inverter are as follows:

$$\begin{cases} i_{d1} = F_{11}^b i_A + F_{21}^b i_B + F_{31}^b i_C \\ i_{d2} = F_{10}^b i_A + F_{20}^b i_B + F_{30}^b i_C \end{cases} \tag{6}$$

The current i_{d0} is defined by the following relation:

$$i_{d0} = (i_A + i_B + i_C) - (i_{d1} + i_{d2}) \tag{7}$$

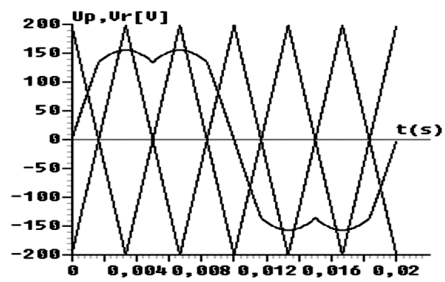

Figure 4. Space vector modulation strategy ($m = 6$, $r = 0.8$).

3.3. PWM strategy for the three-level NPC VSI

The inverter is controlled by the space vector modulation strategy which uses two bipolar carriers. This strategy is characterized by two parameters [4] [5] [8] [9]:

- modulation index m defined as ratio between the carrier frequency f_p and the reference voltage frequency $\left[m = \frac{f_p}{f}\right]$.
- modulation rate r, which is the ratio between the magnitude V_m of the reference voltage and the carriers magnitude U_{pm} $\left[r = \frac{V_m}{U_{pm}}\right]$.

Fig. 4 shows the signals of this strategy. Fig. 5 represents the simple output voltage of the three-level NPC inverter controlled by the proposed PWM strategy.

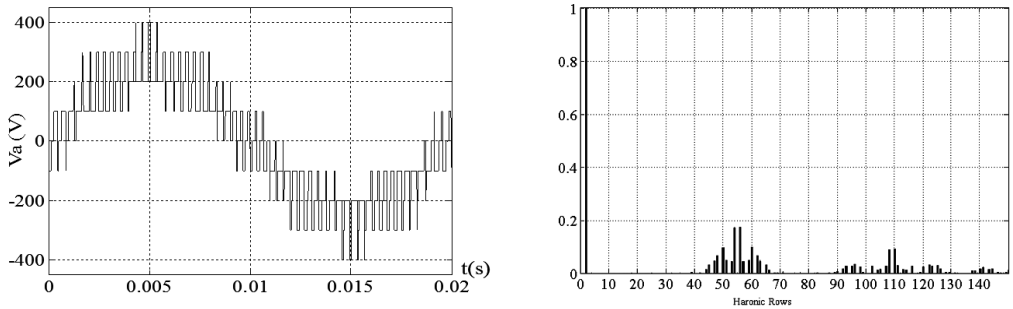

Figure 5. Simple voltage of the inverter and its spectrum $(m = 27)$.

For even values of m, the output voltages present symmetry relatively to the quarter of the period. Then, only odd harmonics exist. These harmonics are gathered as family centered around frequencies multiple of $2mf$. The first family centered around frequency $2mf$ is the most important in view of its magnitude (Fig. 5).

4. Two three-level PWM rectifiers-filter and two three-level NPC VSI-DSIM cascade

Until now, we have supposed the input DC voltages of the three-level NPC VSI constant. In this section, we study generation input DC voltages technique [3]. We propose a cascade constituted by two three -level PWM rectifiers-filter-two three-level NPC VSI which feeds DSIM (Fig. 6). This cascade lets to absorb, in network, sinusoidal input currents with unity power factor.

All control strategies used for the two-level inverter can be used for the two-level PWM rectifier [10] [11]. In this paper, they use the current hysteresis strategy to control this rectifier.

4.1. Modeling of the intermediate filter

The model of the intermediate filter is defined by the following system:

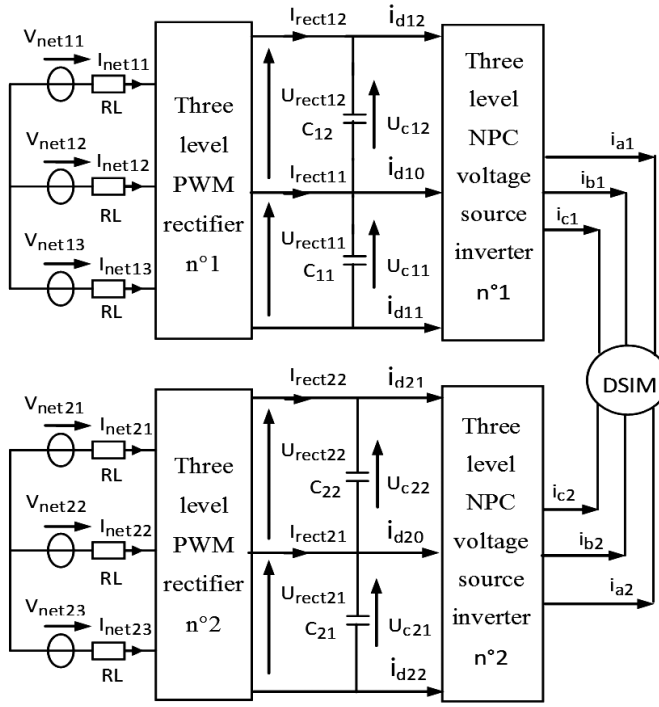

Figure 6. Two three-level PWM rectifiers-filter-two three-level NPC VSI-DSIM cascade.

$$\begin{cases} C_{11}\dfrac{dU_{c11}}{dt} = I_{rect11} + i_{d11} \\ C_{12}\dfrac{dU_{c12}}{dt} = I_{rect12} - i_{d12} \\ C_{21}\dfrac{dU_{c21}}{dt} = I_{rect21} + i_{d22} \\ C_{22}\dfrac{dU_{c22}}{dt} = I_{rect22} - i_{d21} \end{cases} \tag{8}$$

Note, that

$$\begin{cases} U_{rect1} = U_{rect11} + U_{rect12} \\ U_{rect2} = U_{rect21} + U_{rect22} \end{cases}$$

4.2. Simulation results

The parameters of the intermediate filter are: $C_{11} = C_{12} = C_{21} = C_{22} = 10$mF. The battery voltage is initialized at $U_{c11} = U_{c12} = U_{c21} = U_{c22} = 200$V. The different input voltages of the VSI are not stable and they differ (Fig. 7). The output voltages of the two three-level rectifiers decrease continuously (Fig. 8).

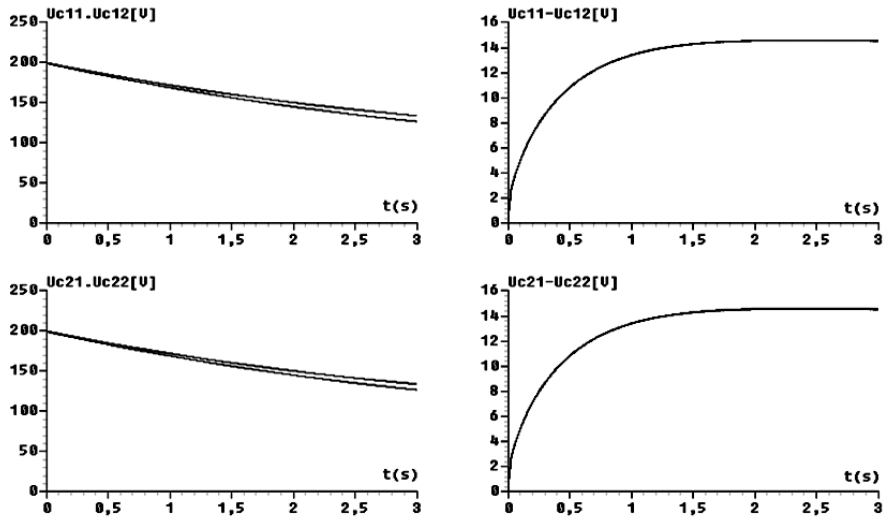

Figure 7. Input DC voltages of the three-level NPC VSI.

5. The half clamping bridge

To improve the input voltages of the three-level NPC inverter, we propose to use a half clamping bridge, constituted by a transistor and a resistor [4] [10] [11]. The transistors are controlled to maintain the different input DC voltages of the inverter equal (Fig. 9).

5.1. Modeling of the intermediate filter

Fig. 10 shows the structure of the intermediate filter of the studied cascade.

The model of the half clamping bridge-filter set is defined by the following equation:

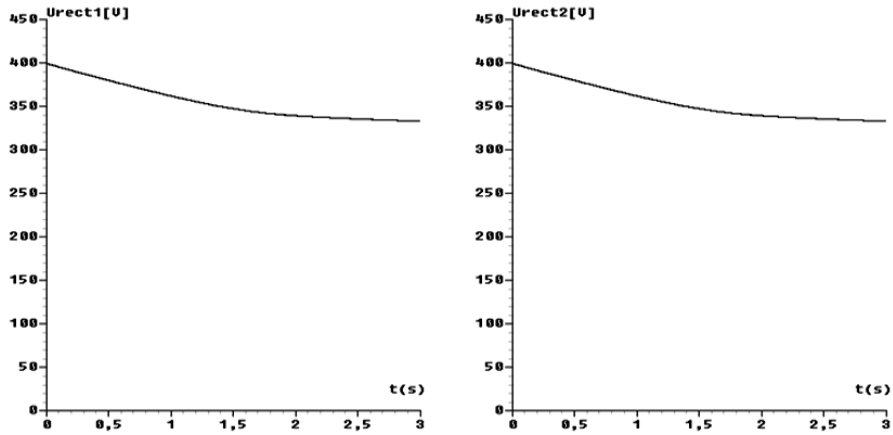

Figure 8. Input DC voltages of the three-level NPC VSI.

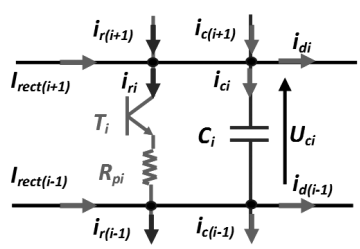

Figure 9. Clamping bridge cell.

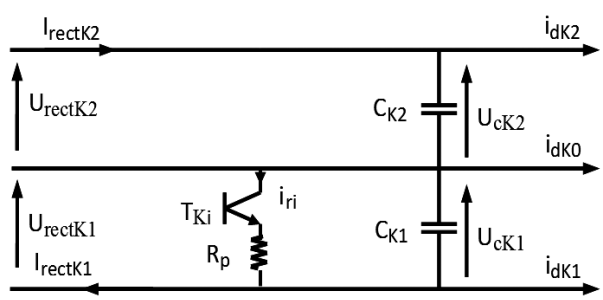

Figure 10. Structure of the intermediate filter of the of the half clamping bridge cascade.

$$\begin{cases} C_{k1}\dfrac{dU_{Ck1}}{dt} = I_{rectk} - I_{dk1} - I_{ri} \\ C_{k2}\dfrac{dU_{Ck2}}{dt} = I_{rectk} - I_{dk2} \end{cases} \tag{9}$$

where

$$I_{ri} = \frac{U_{Ck1}}{Rp} \tag{10}$$

and $i = 1$ for the first filter, $i = 2$ for the second filter.

The control algorithm of the resistive clamping circuits can be summarized as follows:

$$\text{If} \quad U_{Ck1} > U_{rect\,k1} \;\Rightarrow\; (T_{k1} = 1)\; and\; (T_{k2} = 0)$$

5.2. Simulation results

Figures 11, 12, 13, 14 and 15 show the simulation results when using the resistive clamping circuits. The parameters of the intermediate filter are: $C_{11} = C_{12} = C_{21} = C_{22} =$ 10mF and $R_p = 48\Omega$.

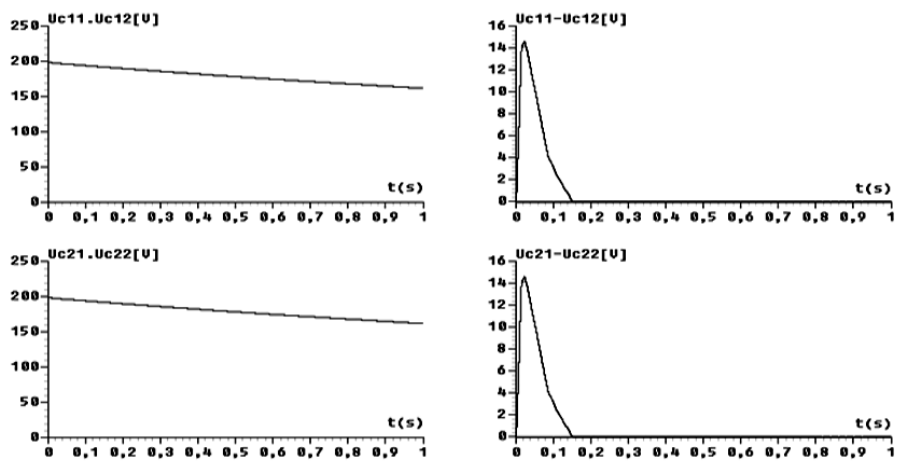

Figure 11. Clamping bridge voltage and their differences.

Note that the input voltage of two three-level NPC VSI (U_{c11}, U_{c12}, U_{c21}) and U_{c22}) become practically equal in bench regime and their differences are decreased to have a value practically null in steady state (Fig. 11). The output voltage of the two three-level are lightly increased (Fig. 12). The currents i_{d11} and i_{d21} are respectively the opposite of the currents i_{d12} and i_{d22}. The currents i_{d10} and i_{d20} have a mean value practically null

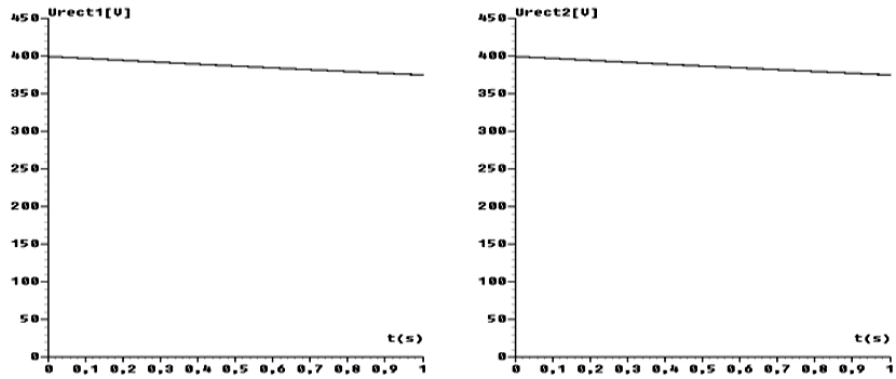

Figure 12. Input voltage of the clamping bridge.

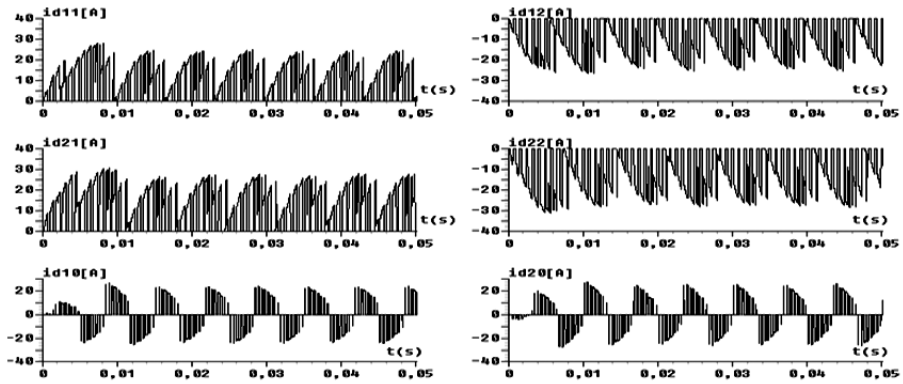

Figure 13. Input currents of the three-level inverter.

(Fig. 13). The rectifier currents I_{rect11}, I_{rect12}, I_{rect21} and I_{rect22} are practically equal (Fig. 14). The performance of the speed control algorithm of the DSIM shows that the current of the machine is nearly sinusoidal. The speed is not affected by an application of a load torque (Fig. 15).

6. Conclusion

In this paper, we have studied the stability problem of the input voltages of the three-level NPC VSI. The modeling of the three-level inverter shows that it is equivalent to

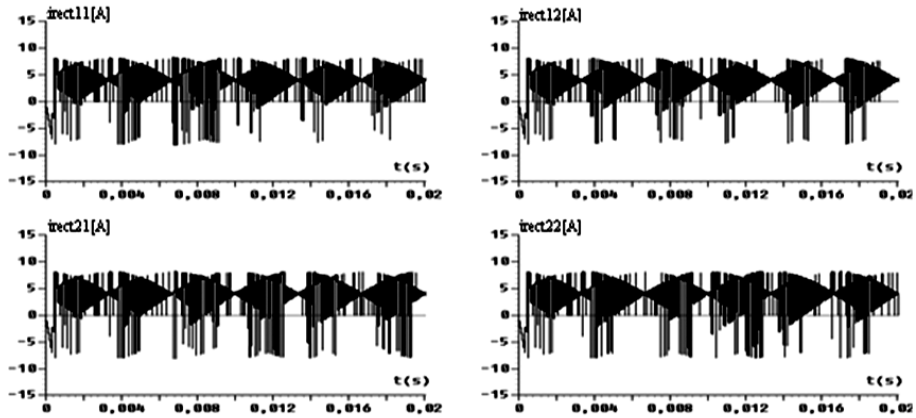

Figure 14. Output rectifier currents.

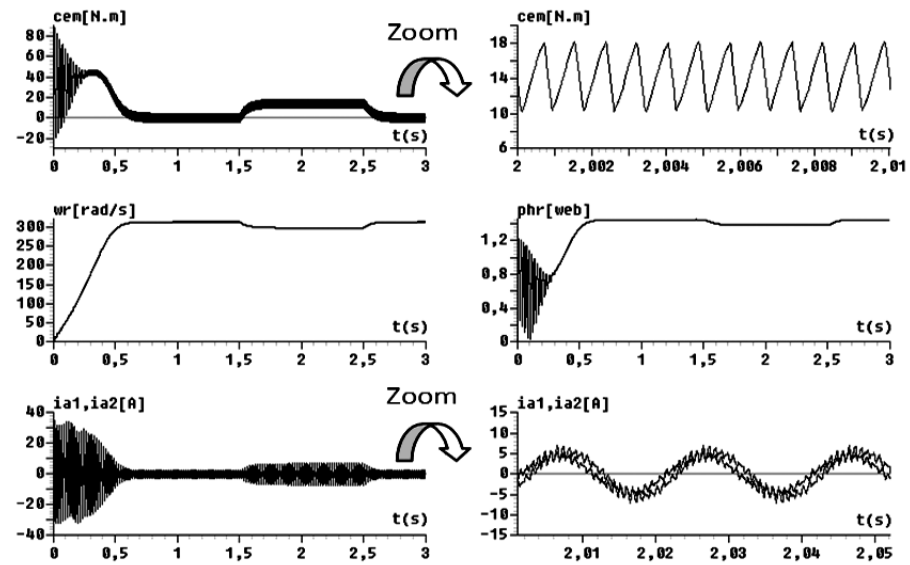

Figure 15. DSIM performances.

two two-level inverters in series. This characteristic lets us to extrapolate the strategies used for the two-level inverter to the three-level NPC inverter.

The study of the stability problem of the input voltages of three-level shows that the different input voltages of this VSI are not stable and their differences are not to be neglected. To solve this problem, we have proposed the use a half clamping bridge. This

solution allowed us to equalize the different input DC voltages of the inverter. Then, we showed that the input voltages of the VSI are practically equal by pairs and their differences are decreased to zero in steady state. The results obtained with this solution are promising to be used to stabilize the input DC voltages of the inverter in an opened loop.

Appendix

r_s, r_r – are the stator and rotor resistors respectively,
φ_{sd}, φ_{rd} – are the stator and rotors flux respectively,
i_{sd}, i_{rd} – are the stator and rotors current respectively,
V_{sd}, V_{rd} – are the stator and rotor voltages respectively,
L_s, L_r – are the stator and rotor inductances respectively,
L_m – is the mutual inductance,
g – is the slip of the rotor relative to the stator rotating field,
ω – is the angular speed,
ω_r – is the angular speed of the axes (d,q) relatively to the rotor,
p – pairs of poles,
d – direct axes,
q – quadrature axes,
C_{em} – is the electromagnetic torque,
k – is the arm number,
B_{ks} – is the gate control of the switch T_{ks},
F_{i1}^b, F_{i0}^b – is the half arm connection function associated to the upper and lower half arms respectively,
NPC – neutral point clamped,
VSI – voltage source inverter,
DSIM – double stator induction motors,
DC – Direct current,
m – is the modulation index,
f_p – is the carrier frequency,
f – is the reference voltage frequency,
r – is the modulation rate,
V_{AM}, V_{BM}, V_{CM} – are the output voltage of each arm of the inverter with respect to the middle point M,
U_{C1}, U_{C2} – are the input voltage of the three level inverter,
U_{rect} – is the rectifier voltages,
i_{d1}, i_{d2}, i_{d0} – are the input currents of the three level inverter,
i_A, i_B, i_C – are the load currents,
i_{rect} – is the rectifier current,
R_p – is the resistor of clamping bridge.

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