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SOFT FAULT CLUSTERING IN ANALOG ELECTRONIC CIRCUITS WITH THE USE OF SELF ORGANIZING NEURAL NETWORK

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Abstract

The paper presents a methodology for parametric fault clustering in analog electronic circuits with the use of a self-organizing artificial neural network. The method proposed here allows fast and efficient circuit diagnosis on the basis of time and/or frequency response which may lead to higher production yield. A self-organizing map (SOM) has been applied in order to cluster all circuit states into possible separate groups. So, it works as a feature selector and classifier. SOM can be fed by raw data (data comes from the time or frequency response) or some pre-processing is done at first. The author proposes conversion of a circuit response with the use of e.g. gradient and differentiation. The main goal of the SOM is to distribute all single faults on a two-dimensional map without state overlapping. The method is aimed for the development stage because the tolerances of elements are not taken into account, however single but parametric faults are considered. Efficiency analyses of fault clustering have been made on several examples e.g. a Sallen-Key BPF and an ECG amplifier. Testing procedure is performed in time and frequency domains for the Sallen-Key BPF with limited number of test points i.e. it is assumed that only input and output pins are available. A similar procedure has been applied to a real ECG amplifier in the frequency domain. Results prove a high efficiency in acceptable time which makes the method very convenient (easy and quick) as a first test in the development stage.

Keywords: fault detection, parametric faults, analogue electronic circuits, self-organizing neural network.

1. Introduction

Test and diagnosis of analog electronic circuits (AEC) is a difficult problem, which even in the face of the expansion of digital circuits cannot be neglected. The obvious link between the outside world (which is analog by its nature) and input interface for signal processing leads to the use of analog input circuits. The first block in many electronic devices is always analog. The next block in the signal processing pipeline is an analog-to-digital converter where the analog world becomes a digital one. As the result of such an approach, digital signal processing methods can be applied because they are much simpler to implement and control (compared with analog signal processing). Turning to the problem of diagnosis and testing, we can see a clear disproportion between the methods dedicated to digital and analog circuits [1-4]. Standards set for digital circuits are used for many years, while every AEC requires a specific, dedicated approach for diagnostic purposes [5]. In case of digital testing, the IEEE1149.1 standard is well described and commonly used. For analog systems, there is lack of standards. The researchers have proposed a mixed signal boundary path IEEE1149.4 [1] however for relatively small circuits it occupies an unacceptably large area on the chip. For that reason many methods for testing analog electronic circuits have been proposed including e.g. heuristic methods.

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One of the major problems in the area of diagnosis is design for testability [6], where a test point selection [7-10] and an input source function [11-13] are optimized. For test point optimization an entropy measure is proposed in [10] and the same problem with use of a genetic algorithm is described in [7]. Comparison of the results of both approaches gives acceptable results (optimal) but the method described in [10] is faster and it is deterministic. The input source optimization can be divided into two domains. An piecewise linear (PWL) function can be designed [14, 15] in case of time domain and a multitone signal (sum of a limited number of sinewaves) is created in the AC domain [12, 13]. A heuristic algorithm of simulated annealing is proposed in [12] for optimal multitone selection. In the case of time domain, the output responses are acquired and classification is based on selected features (delay time, rise time, etc) [15]. The problem of analog fault diagnosis is very complex due to tolerances of elements, and the mainly continuous domain of circuit specification. Other well-known problems come from the size of the analog part which occupies a much greater area than digital components. For a mixed IC, it is estimated that only 10% of the substrate consists of the analog part but the diagnosis cost exceeds 80% of the whole validation process (both analog and digital tests). Typically, the analog part consists of less than 100 elements and is responsible for acquiring information from the surrounding world (e.g. MEMS) or/and performing pre-processing operations on the analog signal (e.g. antialiasing filter) [1, 3, 6]. The circuit responses are measured for the selected test nodes in the predefined domain. A DC analog fault dictionary determination is proposed in [16]. In order to enhance the accuracy of classification, a number of soft computing algorithms can be applied [17-19]. Another reason for applying fuzzy logic is the masking effect of analog elements which leads to ambiguity regions [1, 20]. Historically, the ambiguity region equals 0.7 V for DC domain circuits, which means if the voltage in a particular node for at least two circuit states is less than 0.7 then the states are not separable. Nowadays, researchers apply the Monte Carlo analysis [21] more frequently in order to determine an ambiguity region for a test point [12, 15]. Diagnosis of multiple catastrophic faults with the use of linear programming has been presented in [22]. The advantage of the method is components tolerance consideration. A very interesting approach to fault diagnosis with the use of sigma-delta modulation and an oscillation test has been proposed in [23].

There are a number of artificial intelligence (AI) classification methods [1, 17-19] which provide significantly better classification results compared with the classical methods [16]. Application of wavelet transform is another interesting approach [1, 23]. The wavelet pre-processing results in better diagnosability of the electronic systems. A wavelet-neural network for soft parametric faults has been described in [24-26]. More, a neural network is designated for the purpose of diagnosis of a single [1] and global parametric [27] faults. Another technique for fault diagnosis has been proposed in [28], where measurements are transformed in multi-dimensional space. An algorithm for multiple fault diagnosis has been described in [29], the method is based on the very precise measurements at test points.

A specification driven test (SDT) for field programmable analogue array (FPAA) is proposed in [30]. The authors present a diagnosis method with the use of the internal structure of the hardware. Hardware implementation of the built-in type test is proposed in [31]. Classification of nonlinearity and evaluation of the total harmonic distortion (THD) of the signal under test, without expensive automatic test equipment is presented in [32].The tester is based on a sigma-delta modulator located on a board and artificial neural networks implemented in an attached personal computer. The SVM algorithm [33] is applied to soft and hard faults diagnosis in analog electronic circuits. In this article, the time domain response for unit step excitation as well as soft- and hard-fault injection are considered.

The main disadvantage of AI algorithms is non-deterministic behavior, which often leads to unacceptable deviation of results (the AI algorithm for exactly the same data creates two

different, but almost always good results). Multilayer perceptron (MLP) and feed-forward neural network (FF-NN) applications [34] to analog fault diagnosis are not enthusiastically invited by test engineers because of the aforementioned problem. Moreover, FF-NN and MLP are inefficient for a significant number of data and the first step should reduce this number to an acceptable value. Such chosen values within the circuit under test (CUT) response is named a feature. There are numbers of methods for features optimization but the PCA analysis seems to have results good enough [35]. Nevertheless, the first stage brief test should consider the whole response of the CUT and indicate if there is a possibility for fault detection and/or localization. For that purpose a special neural network has been investigated in this paper, called Kohonen or self-organizing map (SOM). However, there are known Kohonen neural network approaches to hard-fault diagnosis of analog circuits based on the observation of the power supply current [36, 37]. Another application of SOM has been described in [38] where it tries to diagnose ambiguity groups after classification performed by MLP. Proposition of circuit diagnosis with the use of multiple frequencies and SOM is shown in [39]. Unfortunately, none of the applications introduces initial pre-processing and the possibility of detecting soft faults in both time and frequency domains, however the first attempt to diagnose an ECG amplifier has been published in [40]. In the next paragraphs the application of the self-organizing map (SOM) to analog fault diagnosis is presented. Next, two examples of different size are evaluated and compared with a radial basis function neural network (RBF-NN), and feed forward neural network (FF-NN).

2. Testing Procedure

Obviously, there are several stages for test application in analog and mixed electronic circuits. The development stage is the first place where a test can be applied. New product construction (package or chip) is a challenging task even if an assembly or package (final) test is not considered at this level. However, design for testability should be taken into account. In order to evaluate the project when a single fault occurs, a SOM is proposed as a fast and convenient tool for fault isolation on the basis of circuit response. The overall approach for diagnosis with the use of SOM is presented in Fig. 1.

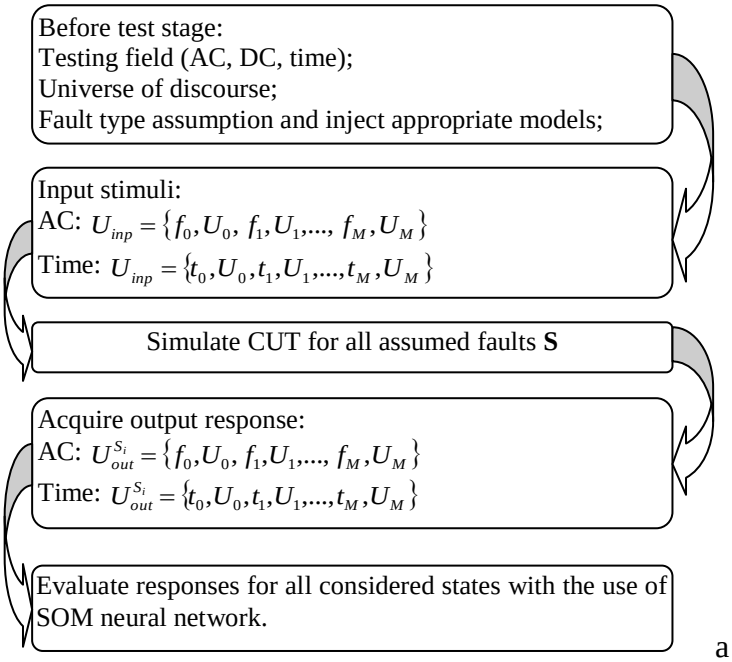

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Fig. 1. Testing procedure.

It has been assumed that input stimulus and the output response are composed of equal number of points. In the following next two subsections the before-test stage and SOM are described.

2.1. Before-Test Stage

Let us assume a CUT with *N* parameters which have to be considered (very often it is *N* elements). The number of all states in the circuit with respect to upper and lower deviation of each parameter is *2N+1* which leads to circuit state set:
$\mathbf{S} = \{S_0, S_1, S_2, ..., S_{2N}\}$, where S_0 is the healthy state.
The main goal of the method is to isolate S_0 and then all other states under the following assumptions:

- upper and lower deviations are to be assumed by the test engineer and can be defined for parametric or catastrophic faults, i.e.

$$\begin{aligned} E_k^{lower} &= \left(1 - dev^{lower}\right) E_k^n \\ E_k^{upper} &= \left(1 + dev^{upper}\right) E_k^n \end{aligned}, \tag{1}$$

  where E_k^n is the nominal value of k^{th} element,
  dev^{lower} and dev^{upper} – depends on fault type, i.e. commonly for a parametric fault it is within the range <0.1;0.6> but for catastrophic faults $dev^{lower}=0.999$ and $dev^{upper}=1E6$.
- Only a single fault occurs at a time,
- Healthy parameters may vary within the tolerance range. The tolerance value depends on circuit functionality and the technological process.

The main goals for the evaluation algorithm are:

- The output results should be obtained relatively fast, however the method belongs to SBT techniques and the time consumption is not crucial at the before-test stage.
- Output data should be analyzed without any pre-processing, i.e. lack of feature extraction block from the CUT is an advantage. The step of feature extraction is not a trivial task but it must be very often introduced in order to reduce input data. In other words, if an algorithm takes all data and reduces it into lower dimension then feature extraction is pointless.
- There must be a measure (or graphical visualization) which indicates clusters (circuit states) close to other circuit states. Such measure helps the test engineer to pay attention to neighbor states. The visualisation should help in assessing a circuit state, may cause a problem during the final test on a production assembly line.

Hence, the method should be independent of field testing, i.e. it allows for testing in the time-, AC, and DC domains. One of artificial intelligence methods which can be applied in the area of analogue fault diagnosis is the Kohonen neural network. The application of such a network and interpretation of results will be given in the next paragraph.

2.2. Self-Organizing Map

A self-organizing map (SOM) is a type of neural network which is trained without an output pattern (called unsupervised learning). The learning algorithm was proposed by Kohonen in 1981 [41, 42]. The purpose of these networks is to group or classify input data, where similar inputs should be classified as belonging to the same category. These categories are determined by the same network based on the correlation of the input. An important feature of SOM is transformation of a large amount of input data into low-dimension map (typically two-dimensional) at the output.

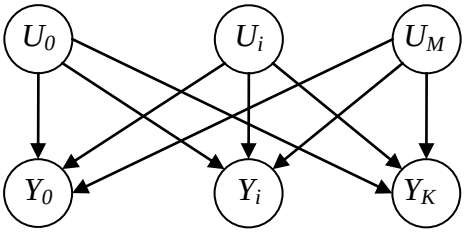

Fig. 2. SOM architecture.

A SOM is built with neurons in the form of a matrix and all of them are excited by the input signal. An important part of the network is a mechanism that for each neuron determines the degree of similarity between its weights to the input signal and calculates the neuron with the best match – the winner. Finally, the network has the ability to adapt to the winner neuron and its neighbors in order to carry out self-organization. So, the network topology depends on strength with which it responded to the input data. Then it can be assumed that the network is arranged, if the topological relationships between input signals and their images are the same. As aforementioned before, SOM has ability for reducing (converting) a large number of input data into a lower number of output data (clusters) which leads to a network architecture of two layers: input and output. Input units are fully connected with weights to output units which have been illustrated in Fig. 2.

The learning algorithm is based on feature presentation (e.g. signals) at the input of the SOM and it can be found in [42-45] and may be briefly cited in the following way:

- Select the topology for the output layer (initialize the current neighborhood distance, *G(0)* to a positive value. The output map dimension is the first important parameter describing the SOM structure. The neural network map must have enough space in order to distribute all states uniformly, i.e. the number of neurons must not be smaller than the number of states. Based on author's experiments, the number of a map should not exceed 10 times more clusters then states.
- Initialize weights from inputs to outputs to small random values;
- Let *n=1 (iteration variable – discrete time index)*
- *While (computational bounds are not exceeded) do*
  1. Select an input sample **u** to the network, where $\mathbf{u} = \{u_1, u_2, ..., u_l\}$
  2. Compute the square of the Euclidean distance of **u** from the weight vector ($\mathbf{w}_j$) associated with each output node.
  3. Select the output node N_{j*} with minimum value from pt. 2. Choose the winning neuron which fits the input vector the best [40] with an appropriate distance metric.
  4. Update weights to all nodes within a topological distance of *G(n)* from N_{j*}, using the update rule:
  $$\mathbf{w}_j(n+1) = \mathbf{w}_j(n) + \alpha_j(n) G(j,\mathbf{u})\left(\mathbf{u}(n) - \mathbf{w}_j(n)\right) \tag{2}$$
  where α is the learning rate (coefficient) generally decreases with time *n* (in our approach linearly, but it can be decreased exponentially):
  $$0 < \alpha_j(n) \le \alpha_j(n-1) \le 1 \tag{3}$$
  where *n=1,2,…no_epochs; j=1,…, no_features l=1,…, no_states;*
  and *G(j,***u***)* is neighborhood function of the j^{th} neuron.
  5. Increment *n*
- *Endwhile*

The neighbor function *G(j,***u***)* is defined as a Gaussian function:

$$G(j,\mathbf{u}) = \exp\left(-\frac{\left\|j - j^*\right\|^2}{\sigma^2(n)}\right) \tag{4}$$

where $\left\|j - j^*\right\|$ is the Euclidean distance between the weight vector of j^{th} neuron and winner j^*, σ is the neighborhood parameter, decreasing in time.
The main goal of SOM is to distribute all states evenly in the predefined map.

3. Time domain testing

For the purpose of correct interpretation of a SOM network let us consider the BPF from Fig. 3. The CUT is driven by a unit step function and time domain responses are gathered at the *out* point. The response consists of 101 data points distributed evenly over the range (0;1ms]:
$U_{out}^{S_i} = \{t_0, U_0, t_1, U_1, ..., t_{100}, U_{100}\}$ for all circuit states **S**={S_0,S_1,…,S_{14}}={Healthy, R_1(-), R_2(-), R_3(-), R_4(-), R_5(-), C_1(-), C_2(-), R_1(+), R_2(+), R_3(+), R_4(+), R_5(+), C_1(+), C_2(+)}, where (-) indicates the value of the element for dev^{lower}=0.1 and (+) means dev^{upper}=0.1 according to eq. (1). All responses are presented in Fig. 4. Each response has been transformed with the use of the following formulas:

1. Gradient: $\nabla U_{out}^{S_i}(t) = \dfrac{\partial U_{out}^{S_i}(t)}{\partial t}$
2. Laplacian: $l^{S_i} = \dfrac{\nabla^2 u_{out}^{S_i}(t)}{4}$
3. Differentiate: $Diff^{S_i} = u_{out}^{S_i}(t_{n+1}) - u_{out}^{S_i}(t_n)$

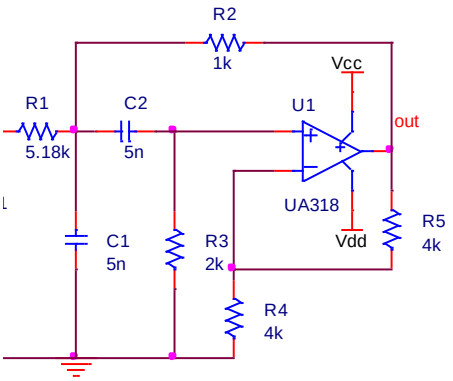

Fig. 3. Sallen-Key band pass filter.

Hence, correlations between the healthy state and fault responses have been calculated. It has been done for clarification of the method and better understanding of the SOM outputs, however this step is not mandatory and can be neglected.

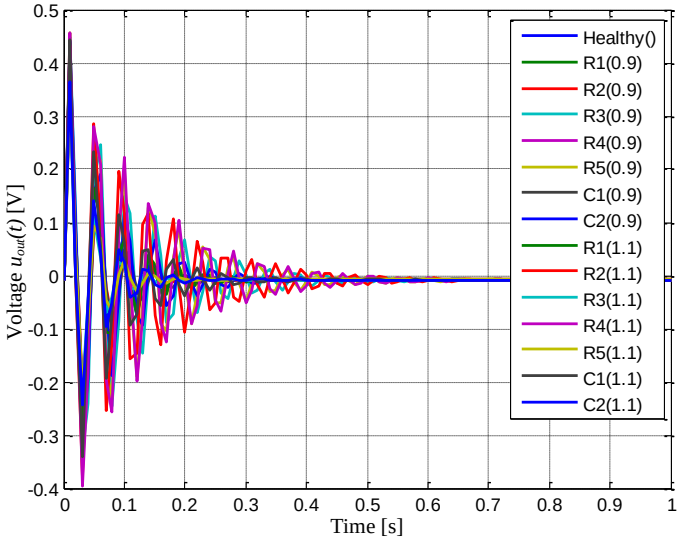

Fig. 4. Time domain circuit responses for all investigated states.

Pearson's correlation coefficient has been utilized as a parameter to assess the response of S_i relative to the state S_0:

$$r_{S_0 S_i} = \frac{\operatorname{cov}\left(u_j^{S_0}(t), u_j^{S_i}(t)\right)}{\sigma(u_j^{S_0}(t)) \cdot \sigma(u_j^{S_i}(t))}, \tag{5}$$

where $\operatorname{cov}\left(u_j^{S_0}(t), u_j^{S_i}(t)\right) = \overline{u_j^{S_0}(t) \cdot u_j^{S_i}(t)} - \overline{u_j^{S_0}(t)} \cdot \overline{u_j^{S_i}(t)}$ is covariance, $\overline{u_{out}^{S_i}(t)}$ is the expected circuit response for state S_i (and corresponding fault); $\sigma(S_i)$ is standard deviation of state S_i. Correlation values between the nominal response and all other states under consideration are depicted in Table 1.

Table 1. Correlation values between state S_0 and other states.

State	Differentiate	Gradient	Laplacian
S_0	1.0000	1.0000	1.0000
S_1	0.9972	0.2797	0.9724
S_2	0.9596	0.3575	0.7142
S_3	0.8738	-0.0766	0.8898
S_4	0.9842	-0.2881	0.5470
S_5	0.9439	0.3184	0.9634
S_6	0.9523	0.1293	0.6606
S_7	0.9430	-0.5787	0.9411
S_8	0.9982	-0.5142	0.8725
S_9	0.8891	0.1299	0.8368
S_{10}	0.9613	0.5285	0.4956
S_{11}	0.9321	0.5883	0.9568
S_{12}	0.9822	-0.4872	0.5683
S_{13}	0.9494	-0.6759	0.8990
S_{14}	0.9669	0.5666	0.8954

Correlation coefficients are going to SOM and the network should cluster the data into separate groups.

3.1. Interpretation and description of results

The Matlab environment has been utilized for method implementation and SOM neural network construction. According to the procedure from subsection 2.2 and the number of input data, the SOM architecture is presented in Fig. 5. The output topology must consist of much more neurons then states under consideration which has been inferred from many simulations and experience. Therefore, the output matrix is a map 7x6=42 neurons.

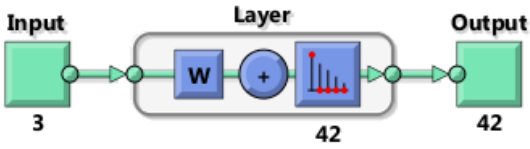

Fig. 5. Network architecture.

Fig. 6 presents SOM neighbour weight distances, where a dark color indicates relatively large weight (long distance) and light color means small weight. Fig. 7 present visualizations of the weights that connect each input to each of the output neurons (dark color = large weight), i.e. if the connection patterns of two inputs are very similar, the inputs were highly. In the example none of inputs are the same so it suggests low correlation between inputs which is much more suitable.

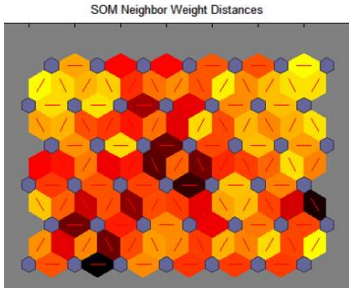

Fig. 6. SOM Neighbor Weight Distances.

Figs. 6 and 7 can be utilized for results evaluation in the case of any optimization process. Nevertheless, the main aim of the method is to cluster data (CUT state) into separate groups, then the most important is Fig. 8 (left). It tells how many data points are associated with each neuron, i.e. for 100% correct location of fault states each neuron should be linked with one input.

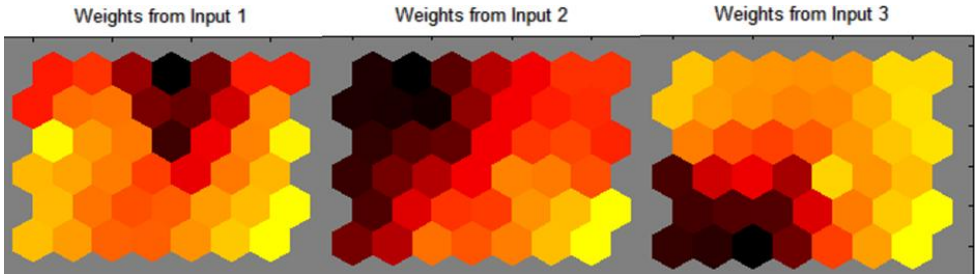

Fig. 7.Weights from SOM inputs.

The left subplot in Fig. 8 is the output map with the number of samples belonging to each neuron. The right subplot shows interpretation of sample hits with labelled circuit faults associated with a particular neuron.

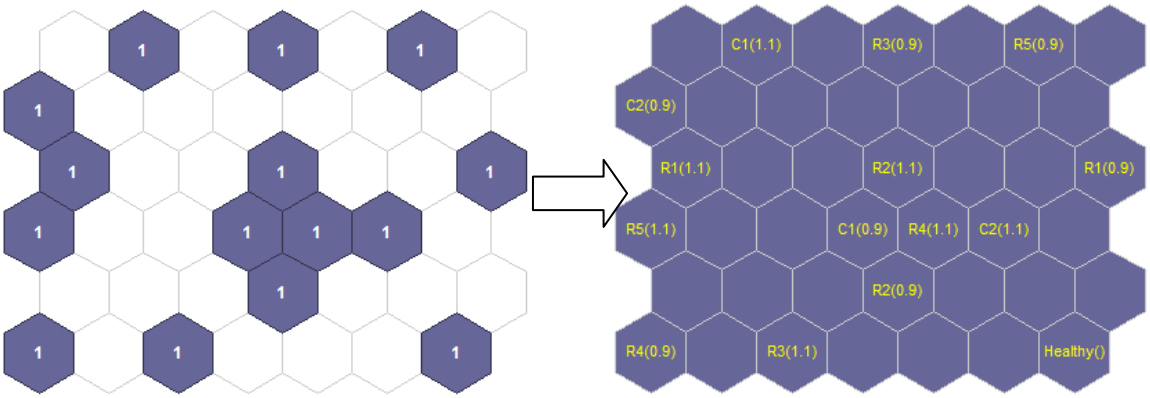

Fig. 8. Sample hits – raw data from SOM (left) and state interpretation (right).

Now, it is quite easy to draw a conclusion because a healthy state is far from other states (no neighbor state bordering with it), whereas R4(1.1) is close to 4 states: C2(1.1), C1(0.9), R2(0.9) and R2(1.1). It means that the test engineer must take into consideration a possibility of incorrect localization under tolerance distribution and different soft fault deviations. However, soft fault has been set to 10% which is very low deviation from the nominal value.

4. Frequency domain testing

In this section two examples with larger number of states have been investigated. The goal is to apply the method in the frequency domain without any feature extraction and calculation before data entering the SOM network. As mentioned before, the method should be fast in implementation, hence the pre-processing is assumed to be needless.

4.1. Sallen-Key Band Pass Filter

The filter from Fig. 4 has been evaluated again, but in the frequency domain. Again, all elements have been checked $\mathbf{S}=\{S_0,S_1,\ldots,S_{14}\}$={Healthy, R_1(-), R_2(-), R_3(-), R_4(-), R_5(-), C_1(-), C_2(-), R_1(+), R_2(+), R_3(+), R_4(+), R_5(+), C_1(+), C_2(+)}, where (-) indicates the value of the element for dev^{lower}=0.3 and (+) means dev^{upper}=0.3 according to eq. (1). The frequency responses for all states are drawn in Fig. 9 between 1 kHz and 500 kHz in the semi-logarithmic scale.

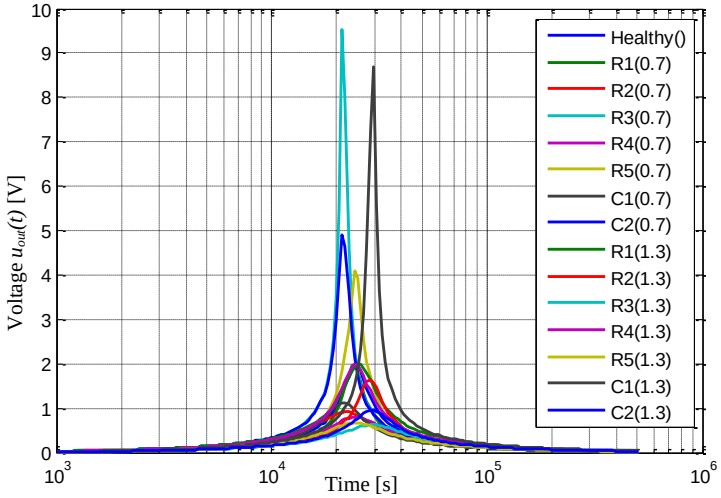

Fig. 9. Frequency responses in test point *[out]* for all faults.

The number of input data is 190 whereas the output map is constructed from 9x8=72 neurons.

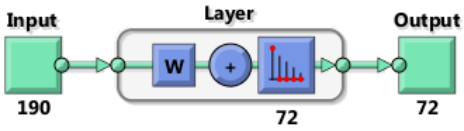

Fig. 10. Network architecture.

After 200 epochs of the learning process, the output map looks like that in Fig. 11 where all states are isolated unequivocally. Comparing with the time domain, the healthy state is again far enough from other states but e.g. R2(0.7) is close to C1(0.7) and R1(0.7) which may be caused by other deviation and the frequency domain.

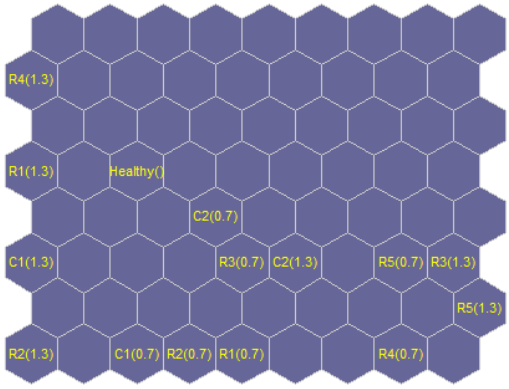

Fig. 11. State clustering results for BPF (Fig. 4).

The results obtained from SOM have been compared with other well-known methods, i.e. feed-forward neural network and radial basis function neural network. The comparison was made on several levels like: detection and localization rate, ambiguity regions and time consumption. Summary results are in Table 2.

Table 2. Comparison of fault diagnosis for different types of neural networks.

Type of Classifier	Input data per state	Output structure	Detection	Localization	Ambiguity set	Time [s]
SOM	190	9x8	Yes	15	0	5.35
Neural Network FF	190	3 layers (20, 15, 10 neurons)	Yes	5	4	93.5
Neural Network RBF	190	15	Yes	15	0	5.75

Table 2 shows correct detection rate for all neural networks, however only RBF and SOM allow for 100% localization of all faults. More, time consumption necessary for learning is almost 20 times greater for FF-NN. It flows from the number of input data and this is the reason for feature extraction in case of FF-NN. The fastest learning time is for SOM and besides the output map gives visualisation of circuit states, what is difficult to obtain for other networks.

4.2. ECG amplifier circuit

Next example is the output stage of an ECG amplifier (Fig. 12) [46] which may be applied for real signal acquisition. The input stage of the ECG amplifier together with e.g. input

drivers is composed of an instrumentation amplifier (e.g. INA128) and it is not presented here, however it plays an important role in ECG acquisition.

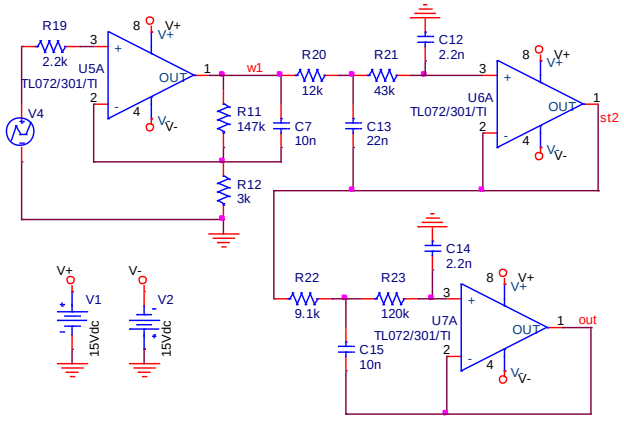

Fig. 12. ECG amplifier.

All elements have been checked $\mathbf{S}=\{S_0,S_1,\ldots,S_{24}\}=\{$Healthy, $R_{11}(-)$, $R_{12}(-)$, $R_{20}(-)$, $R_{21}(-)$, $R_{22}(-)$, $R_{23}(-)$, $C_7(-)$, $C_{12}(-)$, $C_{13}(-)$, $C_{14}(-)$, $C_{15}(-)$, $R_{11}(+)$, $R_{12}(+)$, $R_{20}(+)$, $R_{21}(+)$, $R_{22}(+)$, $R_{23}(+)$, $C_7(+)$, $C_{12}(+)$, $C_{13}(+)$, $C_{14}(+)$, $C_{15}(+)$,$\}$, where (-) indicates the value of the element for $dev^{lower}=0.5$ and (+) means $dev^{upper}=0.5$ according to eq. (1). The frequency responses for all states are drawn in Fig. 9 between 1 Hz and 10 kHz. Each characteristic is composed of 162 points within the aforementioned range. Hence, the input layer equals 162 neurons what is seen in Fig. 14. The output map is a 10x10 neuron matrix. Overall the learning process has taken approximately 6 seconds for 200 epochs and after all the classifier can recognize unequivocal 20 states out of 25. Similar results are gathered from the RBF neural network in comparable time. The worst results have been obtained for a typical feed-forward neural network whose training process is time-consuming and localization is on a very low level. Hence, FF-NN does not give appropriate diagnostic information and the application to analog fault localization is questionable.

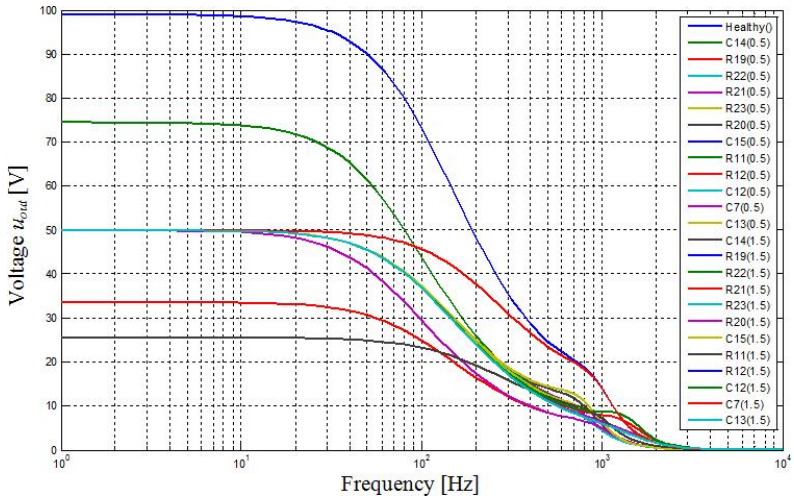

Fig. 13. ECG amplifier frequency responses for all faults in the test point *[out]*.

Let us look closer at the circuit schematic in Fig. 12. Resistor R19 is connected in series with the positive input of U5A operational amplifier. Without any doubt the deviation of R19 could not be detected without information about current in this branch.

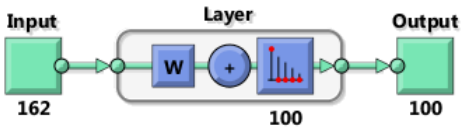

Fig. 14. Network architecture.

If such a brief conclusion is drawn then the undamaged circuit is also detected (there is word "yes" in brackets in Table 3).

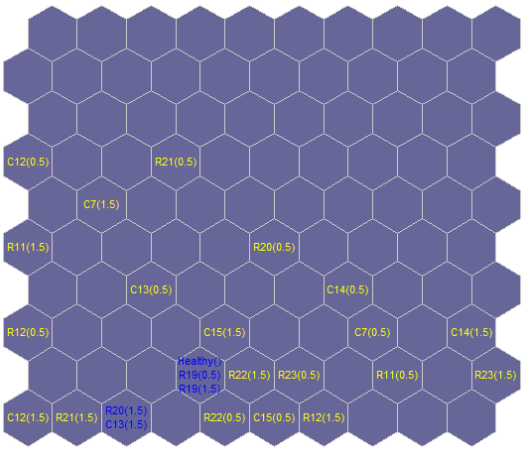

Fig. 15. Clustering results for the ECG amplifier.

Table 3. Comparison of fault diagnosis for different types of neural networks.

Type of Classifier	Input data per state	Output structure	Detection	Localization	Ambiguity set	Time [s]
SOM	162	10x10	No(yes)	20	2	6.16
Neural Network FF	162	3 layers (20, 15, 10 neurons)	No(yes)	7	6	284.44
Neural Network RBF	162	25	No(yes)	20	2	7.26

5. Conclusions

A new approach to analogue circuit fault localization has been proposed in this paper. The method belongs to SBT techniques and the primary use of the method is at the development stage i.e. before the production stage. The method gives information about detection and localization relatively fast comparing to FF-NN and the time is comparable with RBF-NN. The main advantage of SOM is visualisation of results. All similar ("neighbor") faults can be recognized on the basis of the output map. Hence, the test engineer can pay much more attention to such elements in the circuit. Comparison with other neural networks and results shows that the use of the SOM neural network is giving a fast and reliable answer to the question whether the response (or selected features) provide detection and/or location of faults at the appropriate assumed level.

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