DOI 10.2478/v10171-012-0045-8

# Averaged models of pulse-modulated DC-DC power converters. Part I. Discussion of standard methods

### WŁODZIMIERZ JANKE

Technical University of Koszalin Śniadeckich 2, 75-411 Koszalin e-mail: wjanke@man.koszalin.pl

(Received: 12.04.2012, revised: 30.08.2012)

**Abstract:** The averaged models of switch-mode DC-DC power converters are discussed. Two methods of averaged model derivation are considered – the first, based on state-space averaging and the second, on the switch averaging approach. The simplest converters: BUCK, BOOST and BUCK-BOOST working in CCM (continuous conduction mode) or DCM are taken as examples in detailed considerations. Apart from the ideal converters, the more realistic case of converters with parasitic resistances is analyzed. The switch averaging approach is used more frequently than the other and is believed to be more convenient in practical applications. It is shown however, that in the deriving the averaged models based on the switch-averaging approach, some informalities have been made, which may be the source of errors in the case of converters with parasitic resistances, or working in DCM mode.

 $\textbf{Key words:} \ \ Power \ converters, \ pulse-width \ modulation, \ BUCK, \ BOOST, \ BUCK-BOOST, \ averaged \ models$ 

### 1. Introduction

In this series of two papers, the switch-mode DC-DC power converters with pulse-width modulation (PWM) are discussed, in particular – the description of such converters based on averaged models. The group of DC-DC power converters is a broad class of power conversion circuits with enormous range of applications. The circuit configurations, parameters, mathematical descriptions and applications of them are discussed in hundreds of papers, technical data sheets and application notes, conference proceedings as well as in many textbooks and tutorials (for example [1-7]). The averaged models of such converters are widely known, accepted and used in the analysis and design. The averaged models, devoted mainly to DC-DC converters are used in analysis of other groups of converters, such as AC-DC converters with

power factor corrections and DC-AC converters (inverters) as well. The considerations of the present papers are restricted to unidirectional, single-input, single-output DC-DC PWM converters with constant switching frequency. It is not the aim of this paper to make a survey of converters. The examples of the simplest converters are given only as the objects of the modeling methods discussed in the paper. The main purpose of the papers is to point out some limitations, inconsistencies or even errors of standard methods of averaged modeling of converters and to propose the new approach to averaged modeling of converters, free of the above shortcomings.

The DC-DC converter is supplied by the unregulated (and possibly fluctuating) voltage source  $v_G$  and deliver the constant or regulated DC voltage to the load represented by resistance R (or conductance G) in spite of changes or fluctuations of input voltage or load resistance. The typical power converter consists of the power stage (PS) and control circuit (CC) as depicted in Figure 1.

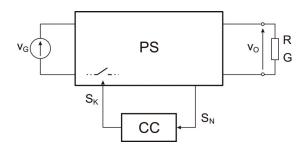


Fig. 1. The general structure of DC-DC converter

Power stage consists of capacitors, inductor coils (sometimes transformers) and semiconductor devices acted as switches. The term "ideal converter" is used throughout both parts of the paper. It denotes a converter which consists of ideal switches (zero voltage in ON state, zero current in OFF state) and the lossless linear inductors and capacitors. The control circuit "observes" the state  $s_N$  of power stage, usually the output voltage, and generates the control signal  $s_K$ . The considerations are restricted to converters containing only two switches and at least one of them is controlled by signal  $s_K$  from control circuit CC. For convenience it is assumed that there is one active or main switch (referred to as "transistor") and one auxiliary switch, referred to as "diode", and signal  $s_K$  controls the state of the main switch (although in modern, synchronous converters there is a pair of active switches, controlled by a pair of synchronous signals). The control signal  $s_K$  may be considered as a voltage applied to a control electrode (gate) of main switch. The high level of this signal drives the switch to ON state; low level – to OFF state. The states ON and OFF of converter correspond to the respective states of the main switch.

The durations of subintervals ON and OFF (Fig. 2) are related to switching period  $T_S$  (or switching frequency  $f_S = 1/T_S$ ) and duty ratio  $d_A$  by formulae:

$$d_A = t_{ON} / T_S, \quad 1 - d_A = t_{OFF} / T_S.$$
 (1)

A typical mode of converter operation is known as continuous conduction mode (CCM), another – as discontinuous conduction mode (DCM). The difference in simple converters depends on the waveforms of inductor current which, in DCM mode, is zero during the part of the OFF subinterval (referred to as OFF2).

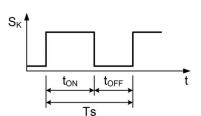


Fig. 2. The waveform of the control signal  $s_K$ 

The power converter, including the power stage and control circuit is a nonlinear, dynamical system with feedback. In some circumstances it exhibits the involved behavior, including bifurcations and chaos [8, 9], therefore the analysis and design of this type of circuit may be not a simple task [10-12]. The analysis or simulation of switch-mode converters may be performed with the use of exact large signal or simplified small signal models. On the other hand the full waveforms of currents and voltages for each subinterval may be analyzed, or the simplified description may be used, adopting the relations of currents and voltages averaged over the switching period. In the latter case, the average values of currents and voltages calculated for single switching period are used as variables in the equations describing the power stage of converter. These averaged variables may, of course, change their values in consecutive periods of switching, therefore they are considered as functions of time and described by differential equations. The switching frequency  $f_S$  is assumed to be much higher than the power stage natural frequencies and the frequencies of eventual changes of input voltage and load conductance. The changes of circuit variables during the single switching period are relatively small, therefore it is assumed, that in a single subinterval (ON or OFF) the circuit variables are constant or changes linearly over time.

In the present paper, the standard approaches to averaged modeling of switch-mode converters are presented. In Section 2 the state-space averaging technique is outlined. The more often used approach based on averaged switch modeling is described in Section 3. Apart from introductory remarks in Section 3.1, the averaged switch modeling for ideal converters are discussed in Section 3.2 and 3.3, and for converters with parasitic resistances – in Section 3.4. In Section 4 the small-signal modeling of converters is discussed.

The large-signal instantaneous values of voltages (or other quantities) are denoted by symbols  $v_G$ ,  $i_L$  etc. The local averaged values in each subinterval are denoted as  $v_G(ON)$ ,  $i_L(ON)$  etc. Their averaged values over the whole switching period are denoted by subscript "S" (sometimes omitted). The large-signal quantities (especially averaged) may be represented as a sum of steady-state values (denoted exemplary as  $V_G$ ,  $I_L$ ) and small-signal, variable values, such as  $v_g(t)$ ,  $i_l(t)$ . The s-domain representation of small-signal variables are denoted, for example, as  $V_g(s)$ ,  $I_l(s)$ .

The averaged models are believed to accurately describe the power stages of converters in low-frequency range (in practice – below approximately 0.2 of switching frequency  $f_S$ ) and are used in the design of control circuits of converters. The alternative approach to control circuit design, based on the analysis of full time-dependencies of instantaneous values of currents and voltages [10, 13, 14], is not considered in the paper.

# 2. State space averaging

### 2.1. Introduction

State space equations are the widely known form of the description of dynamical system and usually are written in the matrix form

$$\dot{\mathbf{x}} = \mathbf{A} \cdot \mathbf{x} + \mathbf{B} \cdot \mathbf{u},\tag{2}$$

$$\mathbf{y} = \mathbf{D} \cdot \mathbf{x} + \mathbf{E} \cdot \mathbf{u},\tag{3}$$

where  $\mathbf{x}$  is a state vector,  $\mathbf{u}$  and  $\mathbf{y}$  are input and output vectors respectively.  $\mathbf{A}$ ,  $\mathbf{B}$ ,  $\mathbf{D}$ ,  $\mathbf{E}$  matrices depend on the topology of a system and on the characteristics of its components. For simple converters, such as BUCK or BOOST, the capacitor voltage and inductor current are usually chosen as the components of the state vector [1, 8, 10, 15].

### 2.2. Continuous conduction mode (CCM)

In *CCM* mode of operation, two topologies corresponding to two possible states of switches are possible, and respective matrices are denoted by subscript "1" for *ON* and "2" for OFF state. If any quantity w in converter has a value  $w_1$  in the *ON* state and  $w_2$  in the *OFF* state, then its average value  $w_S$  over the whole switching period  $T_S$  is:

$$w_S = d_A \cdot w_1 + (1 - d_A) \cdot w_2. \tag{4}$$

Strictly speaking,  $w_1$  is the local average value of w in the ON state and  $w_2$  – in OFF state, therefore the notation w(ON) and w(OFF) are alternatively used.

The essence of the state-space averaging description of converters [1, 8] consists in applying the formula (4) to matrices **A**, **B**, **D**, **E** in state equations, for example:

$$\mathbf{A}_S = d_A \cdot \mathbf{A_1} + (1 - d_A) \cdot \mathbf{A_2}. \tag{5}$$

The averaged state equations of converter are:

$$\dot{\mathbf{x}}_S = \mathbf{A}_S \cdot \mathbf{x}_S + \mathbf{B}_S \cdot \mathbf{u}_S, \tag{6}$$

$$\mathbf{y}_S = \mathbf{D}_S \cdot \mathbf{x}_S + \mathbf{E}_S \cdot \mathbf{u}_S. \tag{7}$$

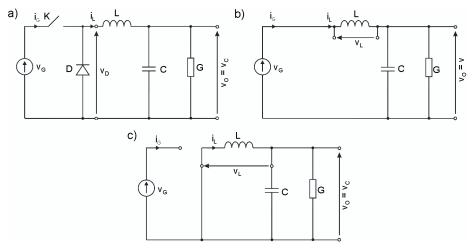


Fig. 3. Power stage of ideal BUCK converter (a) and its equivalent circuits for ON (b) and OFF (c) subintervals. Symbol K denotes the main switch

The ideal *BUCK* converter is taken as an example. Its power stage is shown in Figure 3a) and equivalent circuits for *ON* and *OFF* subintervals, in Figures 3b) and 3c) respectively. The capacitor voltage  $v_C$  and inductor current  $i_L$  are chosen as state variables, input voltage  $v_G$  as the only element of input vector  $\mathbf{u}$ ; voltage  $v_O$  and current  $i_G$  – as vector  $\mathbf{y}$ .

$$\mathbf{x} = \begin{bmatrix} v_C \\ i_L \end{bmatrix},\tag{8}$$

$$\mathbf{u} = \mathbf{v}_G, \tag{9}$$

$$\mathbf{y} = \begin{bmatrix} v_O \\ i_G \end{bmatrix}. \tag{10}$$

In CCM mode, the matrices A, B, D, E for subintervals ON and OFF, are

$$\mathbf{A}_{1} = \begin{bmatrix} -\frac{G}{C} & \frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix},\tag{11a}$$

$$\mathbf{A}_2 = \begin{bmatrix} -\frac{G}{C} & \frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix},\tag{11b}$$

$$\mathbf{B}_1 = \begin{bmatrix} 0\\ \frac{1}{L} \end{bmatrix},\tag{12a}$$

$$\mathbf{B}_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix},\tag{12b}$$

$$\mathbf{D}_1 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix},\tag{13a}$$

$$\mathbf{D}_2 = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix},\tag{13b}$$

$$\mathbf{E}_1 = \begin{bmatrix} 0 \\ 0 \end{bmatrix},\tag{14a}$$

$$\mathbf{E}_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}. \tag{14b}$$

It is seen that  $v_O = v_C$ . The matrices **A** and **E** remains the same in *ON* and *OFF* and are equal to averaged matrices whereas **B**<sub>S</sub> and **D**<sub>S</sub> are calculated according to Equation (4). The resulting, averaged state equations of ideal *BUCK* converter in *CCM* are:

$$\begin{bmatrix}
\frac{dv_C}{dt} \\
\frac{di_L}{dt}
\end{bmatrix} = \begin{bmatrix}
-\frac{G}{C} & \frac{1}{C} \\
-\frac{1}{L} & 0
\end{bmatrix} \cdot \begin{bmatrix} v_C \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{d_A}{L} \end{bmatrix} \cdot v_G, \tag{15}$$

$$\begin{bmatrix} v_0 \\ i_G \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & d_A \end{bmatrix} \cdot \begin{bmatrix} v_C \\ i_L \end{bmatrix} .$$
 (16)

### 2.3. Discontinuous conduction mode (DCM)

For converter in *DCM* mode, three different topologies exist for subintervals *ON*, *OFF1* and *OFF2* of the durations  $d_A \cdot T_S$ ,  $d_B \cdot T_S$  and  $(1 - d_A - d_B) \cdot T_S$  respectively, therefore the formula for averaged matrices is of the following, exemplary form (similarly for other matrices):

$$\mathbf{A}_S = d_A \cdot \mathbf{A_1} + d_B \cdot \mathbf{A_2} + (1 - d_A - d_B) \cdot \mathbf{A_3}. \tag{17}$$

The equivalent circuit of *BUCK* converter in *DCM* mode of operation for *OFF2* sub-interval is shown in Figure 4.

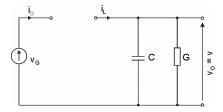


Fig. 4. Equivalent circuit of ideal BUCK converter in DCM, for OFF2 subinterval

The respective matrices for *OFF2* are as follows:

$$\mathbf{A_3} = \begin{bmatrix} -\frac{G}{C} & 0\\ 0 & 0 \end{bmatrix},\tag{18}$$

$$D_3 = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}, \tag{19}$$

$$\mathbf{B}_3 = \mathbf{E}_3 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}. \tag{20}$$

The averaged matrices for ideal BUCK in DCM are given by:

$$\mathbf{A}_{SDCM} = \begin{bmatrix} -\frac{G}{C} & \frac{d_A + d_B}{C} \\ -\frac{d_A + d_B}{L} & 0 \end{bmatrix}, \tag{21}$$

$$\mathbf{B}_{SDCM} = \begin{bmatrix} 0 \\ \frac{d_A}{I_L} \end{bmatrix},\tag{22}$$

$$D_{SDCM} = \begin{bmatrix} 1 & 0 \\ 0 & d_A \end{bmatrix}. \tag{23}$$

The quantity  $d_B$  in Equation (21) is unknown and should be found from additional dependencies. It may be shown [16], that for *BUCK* converter the condition holds:

$$\frac{d_B}{d_A} = \frac{v_G - v_O}{v_O}. (24)$$

The resulting equations for vector **x** (of type 8) leads to:

$$\frac{dv_O}{dt} = \frac{1}{C} \left( -G \cdot v_O + \frac{v_G}{v_O} \cdot d_A \cdot i_L \right),\tag{25}$$

$$\frac{di_L}{dt} = 0. (26)$$

As a result of the obtained formula (26), the averaged description of ideal *BUCK* in *DCM* includes only one differential equation of the first order (i.e. Equation 25), therefore the converter in *DCM* is a first order system, which may be described in *s*-domain by transmittances having only a single pole (contrary to the description in *CCM*, which corresponds to 2-nd order system). The same is true for other simple converters e.g. *BOOST* or *BUCK-BOOST*.

The equations obtained by state-space averaging describe the converter dynamics for low frequency range and are, in general, a set of nonlinear algebraic-differential equations. The small-signal description of converters in the frequency domain will be discussed in the further parts of the paper.

The averaged and small-signal models of *DC-DC* converters based on state-space equations are general, formal description of any type of converter and any operation mode. This description is widely known [1, 4, 8, 10], and is presented here briefly, to give a possibility to compare with averaged models obtained in different ways. The objections to its correctness are met only exceptionally [16, 17], but in many sources the inconveniencies of its practical use are arisen. They are involved with such situations as the need for including the parasitic resistances [1, 4], the operation of converter in *DCM* [1, 16] or taking into account the changes of load conductance [18]. According to opinions in [1, 3, 4], the electrical and electronic engineers and students are much more familiar with circuit descriptions based on Kirchhoff laws and equivalent circuits than with the matrix manipulations. The popular circuit simulators (as SPICE [19]) are not adapted to averaged matrix description.

## 3. Averaged switch modeling

### 3.1. General approach

The averaged switch modeling as a method of the description of switched-mode converters was introduced over twenty years ago. The first systematic presentation of this method may be found in papers of Vorperian [17, 20] and next, the method (with various modifications) was presented in many papers and textbooks, for example [1-4, 10, 21-24]. The authors of the above works usually point out the advantages of "switch averaging" over the state-space averaging approach resulting from a simplicity of switch averaging and the convenience of its use. It should be noted however, that some opinions about the switch averaging technique advantages seems to be doubtful. The example is a statement that the averaged switch model once derived may be introduced into any converter circuit [1, 20] or, that switch averaging itself lead to linear description of converter [4]. Other problems resulting from the use of averaged switch models, especially in the presence of parasitic resistances of switches or in the case of converter working in *DCM* are discussed in further parts of this section, as well as in next part of this paper series.

The most clear presentation of the idea of averaged switch approach may be found in a book [1], Ch. 7.5 and in tutorial [2]. The contents of the subsections 3.1-3.3 is based mainly on the above sources and on earlier works of Vorperian [17, 20]. The principal idea of averaged switch modeling is based on the division of the converter power stage into linear, time-invariant subcircuit A and a pair of switches B (the case of greater number of switches is not considered here), as shown in Figure 5.

The structure of subcircuit *B* depends on the type of converter. The basic structures are presented in Figures 6. The configurations of switches in Figures 6a) and 6b) correspond to *BUCK* and *BOOST* converters respectively. The scheme of *BOOST* converter is presented later, in Figure 7a). The configuration of Figure 6c) may be found for example in *BUCK-BOOST*, or *SEPIC* converters, depending on eventual connection of points *P1* and *P2*.

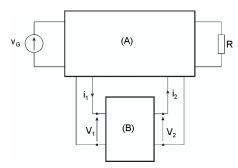


Fig. 5. The power stage division in the switch averaging approach. Subcircuit *A* consists of capacitors and inductors (eventually transformers) only. Subcircuit *B* contains only semiconductor switches

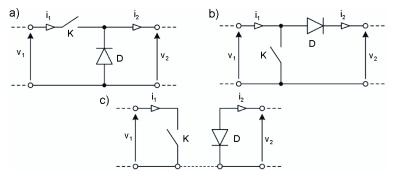


Fig. 6. The connection of switches in subcircuit B of Figure 5

# 3.2. Ideal converters in continuous conduction mode (CCM)

By comparing Figures 3a) and 6a) it is seen, that for ideal BUCK converter:  $i_1 = i_G$ ;  $i_2 = i_L$ ;  $v_1 = v_G$ ;  $v_2 = v_D$ . For ideal *BUCK* converter in *CCM* mode, one obtains from Figure 6a), for *ON* subinterval (K - ON, D - OFF):

$$i_1(ON) = i_2(ON), \tag{27}$$

$$v_2(ON) = v_1(ON) \tag{28}$$

and for OFF subinterval (K - OFF, D - ON):

$$i_1(OFF) = 0, (29)$$

$$v_2(OFF) = 0. (30)$$

By applying Equation (4), the averaged value  $i_{IS}$  of current  $i_I$  is obtained:

$$i_{1S} = d_A \cdot i_2(ON) + (1 - d_A) \cdot 0 = d_A \cdot i_2(ON).$$
 (31)

Similarly:

618 W. Janke Arch. Elect. Eng.

$$v_{2S} = d_A \cdot v_1(ON) + (1 - d_A) \cdot 0 = d_A \cdot v_1(ON). \tag{32}$$

In book [1], tutorial [2], in papers [17, 20] and in other works concerning averaged switch modeling approach, the similar equations are adopted instead of Equations (31), (32), namely

$$i_{1S} = d_A \cdot i_{2S}, \tag{33}$$

$$v_{2S} = d_A \cdot v_{1S}. \tag{34}$$

The application of Equations (33), (34) instead of (31), (32) which are obtained above in formal way, demands the assumption that:

$$i_2(ON) = i_{2S} \text{ and } v_1(ON) = v_{1S}.$$
 (35)

Such assumptions are not made in [1, 2, 17, 20] and, in general, may be not fulfilled. It is important to point out, that the voltage  $v_1$  and current  $i_2$  of switch subcircuit in Figure 6a) correspond to input voltage  $v_G$  and inductor current  $i_L$  of ideal *BUCK* converter. It may be observed, that for ideal converters in *CCM*, the values of inductor current  $i_L(ON)$  and input voltage  $v_G(ON)$  in *ON* subinterval are equal to averaged values  $i_{LS}$  and  $v_{GS}$ , therefore the use of Equations (33), (34), instead of (31) and (32) does not lead to errors.

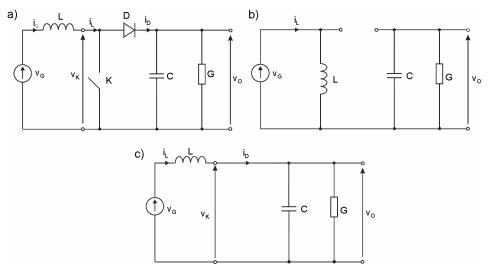


Fig. 7. The power stage of ideal *BOOST* converter (a) and its equivalent circuits for *ON* and *OFF* subintervals – (b) and (c) respectively

Similar derivation may be performed for ideal *BOOST* converter in *CCM*. The power stage of ideal *BOOST* converter is shown in Figure 7a) and equivalent circuits for *ON* and *OFF* sub-intervals are presented in Figures 7b) and 7 c) respectively. The configuration of switches correspond to Figure 6b). By comparing Figures 6b) and 7a) it is seen, that  $i_1 = i_L$ ;  $i_2 = i_D$ ;  $v_1 = v_K$ ;  $v_2 = v_O$ . For subinterval *ON*:

$$v_1(ON) = 0, (36)$$

$$i_2(ON) = 0. (37)$$

For phase *OFF*:

$$v_1(OFF) = v_2(OFF), \tag{38}$$

$$i_2(OFF) = i_1(OFF). (39)$$

Therefore, using (4), we have:

$$v_{1S} = (1 - d_A) \cdot v_2(OFF), \tag{40}$$

$$i_{2S} = (1 - d_A) \cdot i_1(OFF).$$
 (41)

In papers discussing the averaged switch modeling, a slightly different equations are adopted, namely:

$$v_{1S} = (1 - d_A) \cdot v_{2S} \tag{42}$$

and:

$$i_{2S} = (1 - d_A) \cdot i_{1S}. \tag{43}$$

It means, that the unspoken assumptions have been made, that:

$$v_2(OFF) = v_{2S}$$
 and  $i_1(OFF) = i_{1S}$ . (44)

The quantities  $v_2$  and  $i_1$  in subcircuit of Figure 6b) correspond to output voltage and inductor current of *BOOST* converter. For ideal *BOOST* in *CCM*, the output voltage  $v_0(OFF)$  and inductor current  $i_L(OFF)$  are equal to average values  $v_{OS}$  and  $i_{LS}$ , so, in this case, Equation (44) is fulfilled.

The pairs of Equations (33), (34) for BUCK and (42), (43) for BOOST are represented by a special type of ideal transformer in [1, 2] and related works. The averaged models of switching subcircuits of Figures 6a) and b) are represented in [1] and [2] by equivalent circuits shown in Figures 8 a) and b). The transformer in Figure 8 may be replaced by a pair of properly defined controlled sources – see Figure 8 c). The averaged model of a full converter, according to scheme of Figure 5 is obtained by connecting the averaged model of a switch pair, shown in Figure 8 for a BUCK or BOOST to the rest of a circuit, i.e. voltage source  $v_G$ , inductor, capacitor and load R. The example of averaged model of ideal BUCK converter in CCM obtained this way is shown in Figure 9.

According to Figure 9, the following equations may be written:

$$L \cdot \frac{di_{LS}}{dt} = d_A \cdot v_{GS} - v_{OS}, \tag{45}$$

$$i_{LS} = C \cdot \frac{dv_{OS}}{dt} + \frac{v_{OS}}{R}.$$
 (46)

The above equations are consistent with Equation (15) obtained by state-space averaging. Similar observation is true for other ideal converters working in *CCM*.

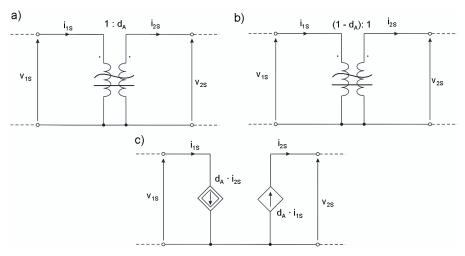


Fig. 8. The models of switching subcircuits of Figs. 6a) and 6b) corresponding to *BUCK* and *BOOST* converters [1, 2]. The equivalent circuit of model (a) containing a pair of controlled sources is shown in (c)

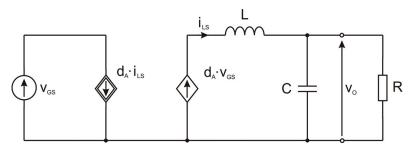


Fig. 9. Averaged model of ideal BUCK converter in CCM obtained with the use of switch averaging

The described procedure of the derivation of averaged models of *BUCK* and *BOOST* introduced in [1, 2, 17, 20] was applied to analysis and design of converters described in many references. However, in this derivation, some informalities may be observed namely, for *BUCK* converter the Equations (33), (34) are used instead of (31), (32) and for *BOOST*, Equations (42), (43), instead of (40), (41). Therefore, the question arises, if these models may be generally accepted, or should be treated as special case models, true only under special assumptions. The problem is discussed in further part of the paper.

### 3.3. Ideal converters in discontinuous conduction mode (DCM)

A DC-DC power converter designed for operation in *CCM* may move to *DCM* if the load current becomes sufficiently low (that corresponds to higher values of load resistance). The operation in *DCM* may be intentionally chosen because the turn-off process of a diode is faster, and the description of circuit dynamics is simpler than in *CCM*. Therefore the averaged

models for *DCM* are important and are presented in the literature [1, 2, 4, 16, 17, 26]. The averaged models of switch pairs such as shown in Figure 6, applied to operation in *DCM* are discussed for example in [1, 2, 16] and [17]. Before the presentation of these models it should be mentioned that there is some controversy about the dynamical features of basic converters in *DCM*.

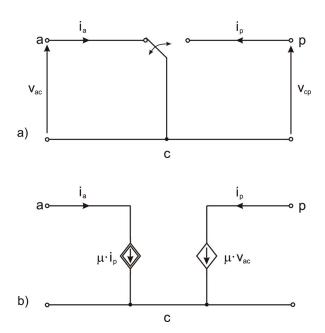


Fig. 10. Averaged model of switch pair for DCM according to [17]

The averaged model of switch pair may be described by Figure 10, [17] and by following equations (the notation is adopted from [17]):

$$i_a = \mu \cdot i_p, \tag{47}$$

$$v_{cp} = \mu \cdot v_{ac}, \tag{48}$$

where:

$$\mu = \frac{d_A^2}{2L \cdot f_s} \cdot \frac{v_{cp}}{i_a} = \frac{d_A^2}{2L \cdot f_s} \cdot \frac{v_{ac}}{i_p}.$$
 (49)

The above equations have been derived for ideal *BUCK-BOOST* converter by the analysis of the waveforms of the inductor current. The power stage of ideal *BUCK-BOOST* converter is shown in Figure 11a) and its equivalent circuits for *ON*, *OFF1* and *OFF2* subintervals – in Figures 11 b), c) and d) respectively. The waveforms of the currents of inductor and both switches are depicted in Figure 12. Apart from the notation used throughout the present paper, the symbols corresponding to Figure 10 (and used in [17]) are added in Figures 11 and 12.

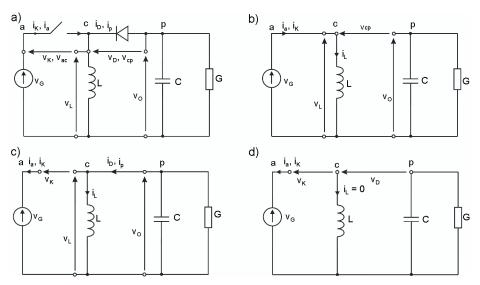


Fig. 11. The ideal BUCK-BOOST converter (a) and its equivalent circuits for ON (b), OFF1 (c) and OFF2 (d) subintervals. Apart from symbols used throughout this paper, the notation of Vorperian [17] is applied

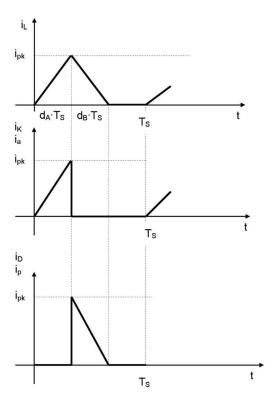


Fig. 12. The waveforms of currents of inductor (a), transistor (b) and diode (c) in ideal *BUCK-BOOST* converter for *DCM* 

The slope of the inductor current (and currents of respective switches in ON and OFFI subintervals) is  $v_L/L$ . In paper [17] these slopes are expressed as  $v_{ac}/L$  and  $-v_{cp}/L$  and used in derivation of Equations (47)-(49). It is evident from Figures 11 b), c) that the formulas for these slopes used in [17] are valid only under assumption that,

$$v_{LS} = 0 \tag{50}$$

and therefore:

$$\frac{di_{LS}}{dt} = 0. ag{51}$$

Conditions (50), (51) are true and may be obtained by state-space averaging procedure for simple converters (it was shown for the example of *BUCK* converter in Section 2). As the result of Equations (50), (51), the averaged model of converter is of the first order (having only one reactive element i.e. capacitor). The problem is, that in [17], the conditions (50), (51) are not expressed explicitly nor mentioned, and in further derivation, the averaged converter model in *DCM* is treated as a second order system (similarly as in other papers, for example [1, 2, 16]), such as the conditions (50), (51) would not be true. The authors of the mentioned works are aware of the inconsistency of that with the results of space-state averaging procedure, but are rather inclined to suppose, that the space-state averaging approach is erroneous [16, 17].

The derivation of the averaged switch models for DCM presented in [1] and [2] differs from the approach given in [17] and is involved with the use of artificial elements such as "lossless resistor"  $R_e$  (for BUCK  $R_e = 2L/(d_A^2 \cdot T_S)$  according to [1, 2]) and the "controlled power source" p(t), but the objections to it are similar to those presented above. The schematic representation of such models for BUCK and BOOST is given in Figure 13 a) and b). It may be observed, that these models are of the second order, different than models obtained by state-space averaging approach for DCM.

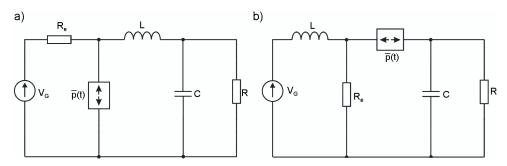


Fig. 13. The averaged models of BUCK and BOOST converters in DCM, according to [1] and [2]

It may be concluded, that there are several objections to models of converters operated in *DCM*, presented or discussed in [1, 2, 16, 17], based on the "switch averaging" approach. The model derivation is inconsistent, the parameters of models of the switch pair are dependent on external parameters (such as inductance in Equation (49), the order of the resulting averaged model of converter differs from that derived by state-space averaging approach.

### 3.4. The converters with parasitic resistances

In the above considerations the components of converters are assumed to be ideal, in particular the parasitic resistances of inductors, capacitors and semiconductor switches are neglected. The accuracy of the converter analysis may be improved by taking into account these resistances. The models of converter components including parasitic resistances are presented in Figure 14. It should be pointed out, that the models of converter components presented in Figure 14, although more accurate than ideal models, are only approximations of real device behavior.

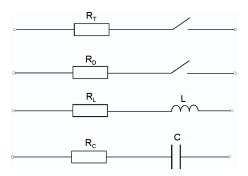


Fig. 14. Models of the components of converter.  $R_T$ ,  $R_D$ ,  $R_L$  and  $R_C$  denote the parasitic resistances of transistor, diode, inductor and capacitor respectively

The derivation of averaged models of switches taking into account the parasitic resistances is presented below for BUCK converter in CCM as an example. The part of BUCK scheme including the transistor and diode with resistances  $R_T$  and  $R_D$  is shown in Figure 15 and its equivalent circuits for ON and OFF subintervals, in Figures 16 a) and b) respectively.

According to procedure presented in subsections 3.1 and 3.2, the pair of ideal switches in Figure 15, corresponding to Figure 6 a), should be described in the form of averaged model by equation:  $v_{2S} = d_A \cdot v_1$  (ON) (i.e. Eqn. 32 in Sec. 3.2). In references [1] and [2], Equation (34) is used instead of (32) and this doesn't result in errors, because, for ideal converter, the condition (35) is fulfilled. Therefore the condition (35) should be verified for converter with parasitic resistances. From Figure 16 a) one obtains:

$$v_1(ON) = v_{GS} - R_T \cdot i_{2S}. {52}$$

From Figure 16 b):

$$v_1(OFF) = v_{GS} + R_D \cdot i_{2S}. \tag{53}$$

The average value of  $v_I$  is therefore:

$$v_{1S} = v_1(ON) \cdot d_A + v_1(OFF) \cdot (1 - d_A) =$$

$$= v_{GS} - i_{2S} \cdot [d_A \cdot R_T - (1 - d_A) \cdot R_D].$$
(54)

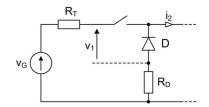


Fig. 15. The input part of BUCK converter with parasitic resistances

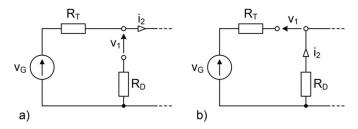


Fig. 16. Equivalent circuits of BUCK of Figure 15 for subintervals ON (a) and OFF (b)

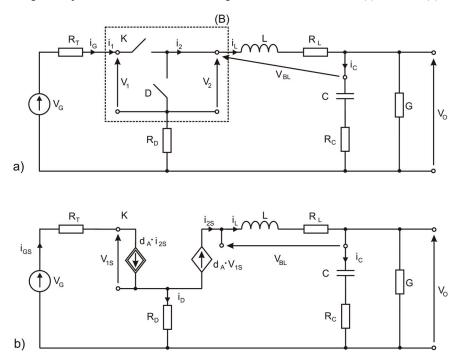


Fig. 17. BUCK with parasitic resistances (a) and its equivalent circuit (b) including model of Figure 8 c)

It is seen that  $v_{1S} \neq v_1(ON)$ , therefore condition (35) is not fulfilled and, as a result, Equation (34) is erroneous for converter with parasitic resistances. This observation presented here for *BUCK* converter may be applied also to other converters. The differences between the

averaged model obtained by state-space averaging and switch averaging for converters in the presence of parasitic resistances were mentioned in the literature [22], but no satisfactory explanation has been given.

The large-signal averaged model of converter with parasitic resistances may be obtained by replacing the pair of ideal switches in full converter scheme, by equivalent circuit of Figure 8. It is shown for *BUCK* with parasitic resistances in Figure 17.

From Figure 17 one obtains:

$$v_G = d_A \cdot i_L \cdot R_T + v_{1S} + i_D \cdot R_D, \tag{55}$$

$$v_O + v_{RL} = d_A \cdot v_{1S} + i_D \cdot R_D, \tag{56}$$

$$i_D = -(1 - d_A) \cdot i_L. \tag{57}$$

From Equations (55)-(57) we get:

$$v_{BL} = d_A \cdot v_G - v_O - i_L \cdot \left[ d_A^2 \cdot R_T + (1 - d_A)^2 \cdot R_D \right]. \tag{58}$$

The formula (58) is used in the discussion presented in the next part of the paper.

Another approach to the problem of including parasitic resistances of transistor and diode in averaged models is presented in [4], Ch. 10, [27, 28]. In these references the "averaged value"  $R_{TS}$  of the resistance  $R_T$  of transistor is calculated on the base of "energy conservation rule" which leads to the equation:

$$i_{1S}^2 \cdot R_{TS} = \frac{1}{T_S} \int_0^{T_S} i_1^2 \cdot R_T \cdot dt.$$
 (59)

The result is:

$$R_{TS} = \frac{R_T}{D_A}. (60)$$

The averaged resistance of a diode, calculated in similar way, is:

$$R_{DS} = \frac{R_D}{1 - D_A}. ag{61}$$

The averaged model of the respective part of *BUCK* converter obtained this way is shown in Figure 18.

By replacing resistances  $R_T$  and  $R_D$  in Equation (58) by equivalent resistances  $R_{TS}$  and  $R_{DS}$  given by (60), (61) and replacing  $D_A$  by  $d_A$  in (60) and (61) one obtains the modified Equation (58) in the form:

$$v_{BL} = d_A \cdot v_G - v_O - i_L \cdot \left[ d_A \cdot R_T + (1 - d_A) \cdot R_D \right]. \tag{58'}$$

The values of  $v_{BL}$  obtained from formulas (58) and (58') are different.

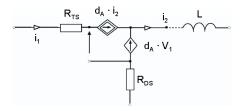


Fig. 18. Averaged model of the pair of switches in BUCK converter according to [4, 27, 28]

# 4. Averaged small-signal models

For the analysis of converter dynamics and the design of control circuits it is convenient to use the linear small-signal model of converter. In the case of state-space averaging approach, it may be obtained by representing vectors  $\mathbf{x}$ ,  $\mathbf{u}$ ,  $\mathbf{y}$  and duty ratio  $d_A$  in the following form:

$$\mathbf{x}_S = \mathbf{X} + \mathbf{x}_m, \tag{62}$$

$$\mathbf{y}_{S} = \mathbf{Y} + \mathbf{y}_{m}, \tag{63}$$

$$\mathbf{u}_S = \mathbf{U} + \mathbf{u}_m, \tag{64}$$

$$d_A = D_A + d_a, (65)$$

where X, Y etc. are steady-state values and  $x_m$ ,  $y_m$  – small-signal (disturbance) values. By introducing the above expressions into equations (6), (7) and neglecting small quantities of the second order (products of small-signal values) one obtains the small signal model of converter in the form [1, 8, 25]:

$$\dot{\mathbf{x}}_{m} = \mathbf{A}_{S0} \cdot \mathbf{x}_{m}(t) + \mathbf{B}_{S0} \cdot \mathbf{u}_{m}(t) + + \left[ (\mathbf{A}_{1} - \mathbf{A}_{2}) \cdot \mathbf{X} + (\mathbf{B}_{1} - \mathbf{B}_{2}) \cdot \mathbf{U} \right] \cdot \mathbf{d}_{a}(t),$$
(66)

$$\mathbf{y}_{m}(t) = \mathbf{D}_{SO} \cdot \mathbf{x}_{m}(t) + \mathbf{E}_{SO} \cdot \mathbf{u}_{m}(t) +$$

$$+ [(\mathbf{D}_{1} - \mathbf{D}_{2}) \cdot \mathbf{X} + (\mathbf{E}_{1} - \mathbf{E}_{2}) \cdot \mathbf{U}] \cdot d_{a}(t).$$
(67)

The Equations (66), (67), are the small-signal approximation of Equations (6), (7). The matrices  $A_{SO}$ ,  $B_{SO}$ ,  $D_{SO}$ ,  $E_{SO}$  correspond to  $A_{S}$ ,  $B_{S}$  etc. and are obtained by substituting  $D_{A}$  for  $d_{A}$  e.g. in Equation (5):

$$\mathbf{A}_{SO} = D_A \cdot \mathbf{A}_1 + (1 - D_A) \cdot \mathbf{A}_2. \tag{68}$$

 $\mathbf{B}_{SO}$ ,  $\mathbf{D}_{SO}$ ,  $\mathbf{E}_{SO}$  are obtained similarly. The next step is to write the equivalent of Equations (66), (67) in s domain and to find the frequency characteristics of the magnitude and phase of properly defined transmittances.

Similar rule of deriving the small-signal approximation may be applied to averaged switch models discussed in Section 3.2. For example, each quantity in averaged model expressed by Equations (33), (34) for ideal *BUCK* converter in *CCM* is represented as:

$$i_{1S} = I_1 + \widetilde{i_1}(t), \tag{69}$$

$$v_{1S} = V_1 + \widetilde{v}_1(t), \tag{70}$$

$$i_{2S} = I_2 + \widetilde{i}_2(t),$$
 (71)

$$v_{2S} = V_2 + \widetilde{v}_2(t), \tag{72}$$

$$d_A = D_A + d_a(t). (73)$$

The sign  $\sim$  is used to distinguish the small-signal terms from full large-signal quantities. After introducing Equations (69)-(73) into (33), (34) the separate equation systems may be obtained for steady-state quantities:

$$I_1 = D_A \cdot I_2, \tag{74}$$

$$V_2 = D_A \cdot V_1 \tag{75}$$

and for small signals:

$$\widetilde{i}_1 = I_2 \cdot d_a + D_A \cdot \widetilde{i}_2,\tag{76}$$

$$\widetilde{v}_2 = D_A \cdot \widetilde{v}_1 + V_1 \cdot d_a \tag{77}$$

Equations (76), (77) may be represented by equivalent circuit shown in Figure 19 being the small-signal averaged model of the pair of switches in *BUCK* converter in *CCM* mode. By connecting the other elements (in accordance with general scheme of Figure 5), one obtains the averaged small-signal model of ideal *BUCK* in *CCM*, shown in Figure 20.

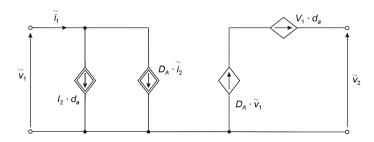


Fig. 19. Averaged small-signal model of the pair of switches in BUCK converter

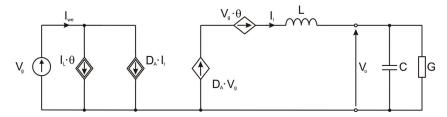


Fig. 20. Averaged small-signal model of ideal BUCK converter in CCM suitable to s-domain analysis

From the s-domain small-signal model, several transmittances of the power stage are derived. The most important are: input-to-output transmittance  $H_g$  (known also as audio susceptibility) and control-to-output transmittance  $H_d$  [1, 4], defined as:

$$H_g = \frac{V_o(s)}{V_g(s)}\bigg|_{\Theta=0},\tag{78}$$

$$H_d = \frac{V_o(s)}{\Theta(s)} \bigg|_{V_g = 0},\tag{79}$$

where  $V_o$ ,  $V_g$ ,  $\theta$  are s-domain small-signal (perturbation) values of output and input voltage and duty ratio respectively. Other transmittances may express the small-signal dependencies of inductor current on  $V_g$  and  $\theta$ , or the dependence of output voltage on load current [1, 4]. The exemplary formulas for transmittances  $H_g$ ,  $H_d$  for ideal BUCK converter in CCM are as follows:

$$H_g = \frac{D_A}{LC \cdot s^2 + G \cdot L \cdot s + 1},\tag{80}$$

$$H_d = \frac{V_G}{LC \cdot s^2 + G \cdot L \cdot s + 1}. (81)$$

The above expressions for ideal BUCK converter in CCM (as well as transmittances of other simple converters in CCM) are presented in many sources, including textbooks, e.g. [1, 4]. In the case of converters in DCM, or converters with parasitic resistances it is more difficult to find the proper description of transmittances in the literature. As it is mentioned earlier, the averaged models in DCM, based on state-space approach differ from that obtained by switch-averaging [1, 2, 16, 17]. Similar inconsistencies are observed for converters with parasitic resistances. For example, the way of introducing the parasitic resistances of transistor and diode, proposed in [4, 27, 28], differs from results obtained according to procedure presented in [1] and [2]. The formulas for small-signal transmittances of basic converters may be found in application notes of switch-mode converter manufacturers. It is interesting that the parasitic resistances  $R_T$  and  $R_D$  of semiconductor switches are usually not accounted for in these formulas (e.g. [29-31] for BUCK and BOOST).

# 5. Summary

In the paper, the averaged models of *DC-DC* power converters working in *PWM* mode with constant switching frequency are discussed. The averaged model of the power stage of *DC-DC* converter is a set of equations (or equivalent circuit) describing the values of currents and voltages averaged over the single switching period. Two standard methods of creating the averaged models of converters have been described, the first, based on state-space averaging and the second – using averaged models of ideal switch pair. The methods, applicable to

various kinds of converters, have been presented by examples of the simplest converters: *BUCK*, *BOOST* and *BUCK-BOOST*. The above methods are generally known and presented in many sources.

The switch averaging approach is presented in the literature as more convenient than state-space averaging and is more frequently used. The known procedure of deriving averaged switch models, analyzed carefully in Section 3 of the paper arises some objections. As has been shown in Section 3.2, the averaged models of the pairs of switches in *BUCK* and *BOOST* converters are obtained under the assumptions true only for ideal converters working in *CCM*. Analysis presented in Section 3.4 shows, that these assumptions may be not fulfilled in the presence of parasitic resistances of converter components. The deriving the averaged switch models for converters in *DCM*, presented in the literature, contains also some informalities. As a result, the models of converters obtained this way, are of the second order – different from that, obtained by state-space averaging.

### References

- [1] Erickson R.W., Maksimovic D., Fundamentals of Power Electronics. 2-nd Edition, Kluwer (2002).
- [2] Maksimovic D., Erickson R.W., *Advances in Averaged Switch Modeling and Simulation*. Power Electronics Specialists Conference, Tutorial Notes (1999).
- [3] Basso P., Switch-Mode Power Supply Spice Cookbook. McGraw-Hill (2001).
- [4] Kazimierczuk M.K., Pulse-Width Modulated DC-DC Power Converters. J. Wiley (2008).
- [5] Wu K.C., Switch-Mode Power Converters. Elsevier Academic Press (2006).
- [6] Kazimierczuk M.K., Czarkowski D., Resonant Power Converters. 2-nd Edn, J. Wiley (2011).
- [7] Mohan N., Undeland T.M., Robbins W.P., *Power Electronics: Converters, Applications and Design.* 3rd Edn., J. Wiley (2003).
- [8] Tse C.K., Bernardo M. D., Complex Behavior in Switching Power Converters. Proc. IEEE 90(5): 768-781 (2008).
- [9] Wong S.C., Wu X., Tse C.K., Sustained Slow-Scale Oscillation in Higher Order Current-Mode Controlled Converter. IEEE Trans. on Circ. and Syst. II, 55(5): 489-493 (2008).
- [10] Maksimowic D., Stankovic A.M., Thottuvelil V.J., Verghese G.C., *Modeling and Simulation of Power Electronic Converters*. Proc. IEEE 89(6): 898-912 (2001).
- [11] Mohan N., Robbins W.P., Undeland T.M. et al., Simulation of Power Electronics and Motion Control Systems an Overview. Proc. IEEE, 82(8): 1287-1302 (1994).
- [12] Pietrenko W., Janke W. Kazimierczuk M.K., Application of Semianalytical Recursive Convolution Algorithms for Large-Signal Time-Domain Simulation of Switch-Mode Power Converters. IEEE Trans. on Circuits and Systems 48: 1246-1252 (2001).
- [13] Rajasekaran V., Sun J., Heck B.S., Bilinear Discrete-Time Modeling for Enhanced Stability Prediction and Digital Control Design. IEEE Trans. on Power Electronics 18 (1): 381-389 (2003).
- [14] Maksimovic D., Zane R., Small-Signal Discrete-Time Modeling of Digitally Controlled PWM Converters. IEEE Trans. on Power Electronics 22(6): 2252-2256 (2007).
- [15] Middlebrook R.D., Čuk S., A general unified approach to modeling switching-converter power stages. Proc. IEEE Power Electronic Specialists Conf. 18-34 (1976).
- [16] Sun J. et al., Averaged modeling of PWM Converters Operating in Discontinuous Conduction Mode. IEEE Trans. on Power Electronics 16(4): 482-492 (2001).
- [17] Vorperian V., Simplified Analysis of PWM Converters Using Model of PWM Switch. Part II: Discontinuous Conduction Mode. IEEE Trans. on Aerospace and Electronic Systems 26(3): 497-505 (1990).

- [18] Janke W., The Extension of Small Signal Model of Switching DC-DC Power Converters. Podstawowe Problemy Energoelektroniki, Elektromechaniki i Mechatroniki, PPEEm'2007, 2: 241-246 (2007).
- [19] PSPICE Manual, version 4.03, MicroSim Corporation (1990).
- [20] Vorperian V., Simplified Analysis of PWM Converters Using Model of PWM Switch. Part I: Continuous Conduction Mode. IEEE Trans. on Aerospace and Electronic Systems 26(3): 490-496 (1990).
- [21] Sanders S.R., Verghese G.C., Synthesis of Averaged Circuit Models for Switched Power Converters. IEEE Trans. on Circuit and Systems 38: 905-915 (1991).
- [22] Dijk van E. et al. *PWM-Switch Modeling of DC-DC Converters*. IEEE Trans. on Power Electronics 10(6): 659-664 (1995).
- [23] Biolek D., Biolkova V., Kolka Z., Averaged Modeling of Switched DC-DC Converters Based on SPICE Models of Semiconductor Switches. Proc. 7-th WSEAS Conf. Circuits, Systems, Electronics, Control and Signal Processing.
- [24] Hren A., Milanovic M., Dynamic Analysis of SEPIC Converter. Automatika 48(3-4): 137-144 (2007).
- [25] Middlebrook R.D., Small-Signal Modeling of Pulse-Width Modulated Switched-Mode Power Conwerters Proc. IEEE 76(4): 343-354 (1988).
- [26] Xu J., Wang J., Bifrequency Pulse-Train Control Technique for Switching DC-DC Converters Operating in DCM. IEEE Trans. On Industrial Electronics 58(8): 3658-3667 (2011).
- [27] Czarkowski D., Kazimierczuk M.K., Energy-Conservation Approach to Modeling PWM DC-DC Converters. IEEE Trans. on Aerospace and Electronic Systems 29(3): 1059-1063 (1993).
- [28] Kazimierczuk M.K., Czarkowski D., Application of the Principle of Energy Conservation to Modeling the PWM Converter. 2-nd IEEE Conf. on Control Applications 291-296 (1993).
- [29] Qiao M., Parto P., Amirani R., Stabilize the Buck Converter with Transconductance Amplifier, International Rectifier. Appl. Note AN-1043.
- [30] Choudhury S., Designing a TMS320F280x Based Digitally Controlled DC-DC Switching Power Supply. Texas Instruments, Appl. Report SPRAAB3 (2005).
- [31] Zaitsu R., Voltage Mode Boost Converter Small Signal Control Loop Analysis Using the TPS61030. Texas Instruments, Appl. Report SLVA274A (2009).