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THE POSITION AND SPEED MEASUREMENT MODULE IMPLEMENTED IN FPGA DEVICE

ABSTRACT *In the paper the position and speed measurement module implemented in FPGA (Field Programmable Gate Array) structure is presented. The module is part of motion processor applied to control DC(Direct Current) and PMSM (Permanent Magnet Synchronous Motor) motors. The module interfaces to quadrature incremental encoders with two outputs signals displayed by 90 electrical degrees and output giving one pulse per revolution. Digital filters of the module make the system resistant to electrical noise. The module is implemented on a Spartan-3E FPGA structure manufactured by Xilinx. Results velocity and position measurement are presented.*

Keywords: *position measurement, speed measurement, permanent magnet synchronous motor, DC motor*

1. INTRODUCTION

A specialized motion processors with feedback loops are used more and more often in servo drives. Usually they control a PMSM (Permanent Magnet Synchronous Motors) or DC (Direct Current) motors. The development of FPGA

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devices make possibility to uses them to built motion processors. To speed and position measure there are most often uses resolvers or incremental encoders. Encoders provide greater measurement precision compared to resolvers [3]. A special measurement module have to be implemented in FPGA structure to interface resolver or encoder to motion processor and speed and position determine.

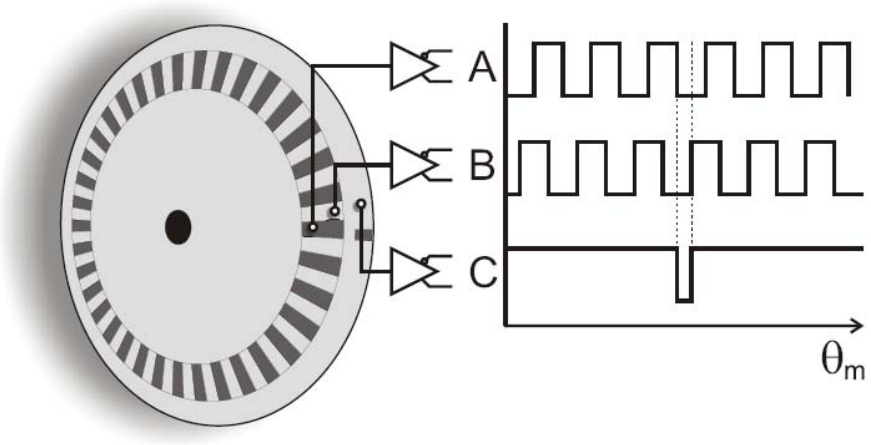

Fig. 1. The principle incremental encoders action

Detection of movement direction in incremental encoders requires the usage of two channels “A” and “B”, which signals are shifted by 90 electrical degrees. The third channel “C” generates one impulse per revolution and is a reference signal.

Resolution and maximal frequency of output impulses are the basic parameters of an encoder. The maximal frequency of measured signals from the encoder dependent on the type of the encoder and reaches 1 MHz.

The measurement circuit should be resistant to electromagnetic interference, mechanical vibration etc.

Electronic circuits which cooperate with encoders contain filters which protect the circuit against electromagnetic interference, detect movement direction and position measure.

Usually specialized measurement cards based on microprocessors with dedicated encoders inputs or ASIC circuits are used to measure speed and position.

2. SPARTAN – 3E PROGRAMMABLE CIRCUIT

Spartan – 3E is a FPGA (Field Programmable Gate Array) circuit manufactured in 90nm technology [5]. The Spartan – 3E product line belongs to the Spartan – 3 circuit family and is characterized by its large logic resources. Its internal structure is regular. Configurable Logic Blocks (CLBs) are the main system blocks of those circuits. They contain highly flexible logic resources configuration based on Look-up Tables (LUTs). Other important blocks include configurable blocks of RAM memory (Block RAM), hardware multiplexers (Multiplexer Blocks), clock signal synthethizers DCM (Digital Clock Management). Particular blocks are interconnected via signal lines of different length, which ensure correct signal propagation. Communication with the outside world is realized by means of configurable input/output blocks (I/O blocks). A block schematic of the Spartan – 3E circuit is presented on Figure 2.

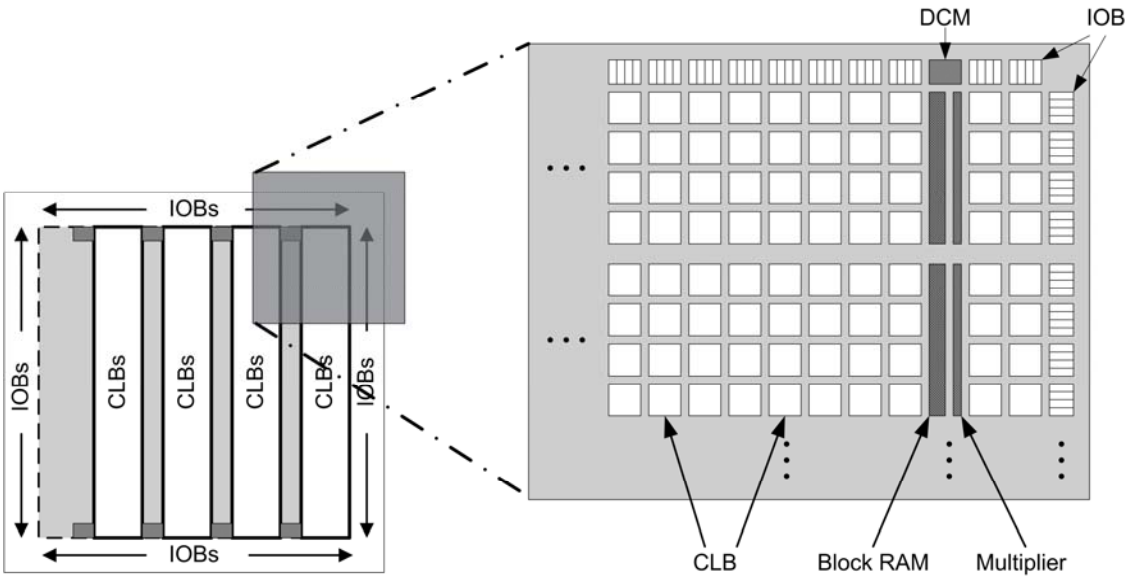

Fig. 2. Block diagram of the system Spartan-3E

In the presented system there was used the XC3S1600E device. It contain 1.6 million gates (System Gates).

The circuit can be programmed in-system using Xilinx Platform Flash PROM memory, SPI and BPI interfaces, serial or parallel interface or using JTAG. Programming of the circuit is done by writing a configuration of connection bit map into the RAM memory. The number of write cycles is unlimited. The

program is written in VHDL (Very high speed integrated circuit Hardware Description Language) which is a IEEE standard. Xilinx ISE software was used for simulation and compilation of the design.

3. POSITION AND SPEED MEASUREMENT MODULE

The presented speed and position measuring module cooperates with quadrature incremental encoders. It was implemented in programmable XC3S1600E device.

The module has inputs for channels A, B and C from encoders, contain digital filters, logic decoding signals system and position and speed counters [2].

A block schematic of the measurement system is presented in Figure 3.

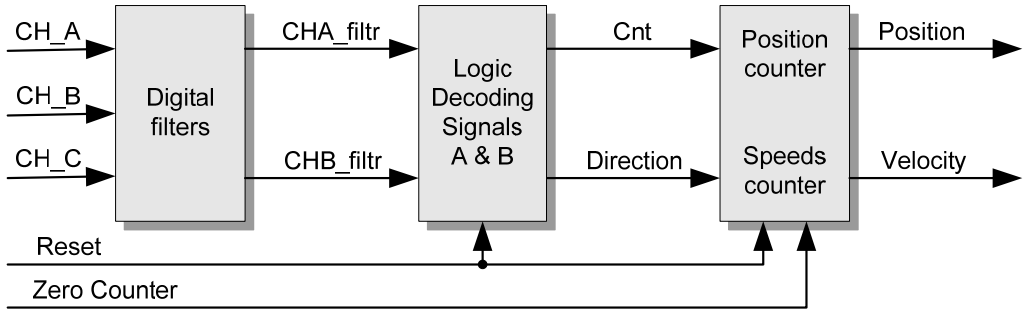

Fig. 3. Block diagram of the measurement system

The digital filters block includes two connected in cascade filters. The first filter eliminates pulses shorter than T_{min}. The minimum pulses duration is calculated on formulas:

$$f_{max}=V_{max}*cp,$$

$$T_{min}=1/2*f_{max},$$

where:

f_{max} – maximal frequency of pulses train from encoder,

V_{max} – maximal rotary speed [rev/sec.],

cp – quantity of pulses generated by encoder in one channel during one revolution [incr./rev].

Measuring of pulses duration is made separately for each channel. The filter is presented in Figure 4.

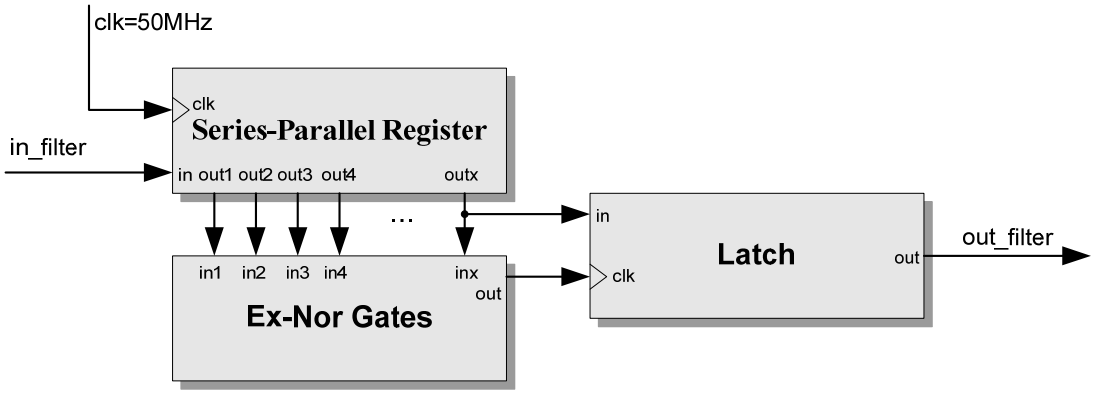

Fig. 4. The filter rejecting short pulses

The signals from encoder input to a series-parallel register. Bits in the register are transferred from 50 MHz frequency.

The Ex-Nor gate verify whether all the outputs of register are in the same state. If they are in the same state, the state of register is latched. Outputs of Latch is output of the filter.

When the outputs bits of the register are in different states, the state of the output filter is the last state of the Latch. This filter introduces delay to the signal being measured. This delay is fault, but it doesn't influence on results of the measurement.

The second filter eliminates pulses which appear only in a single channel. This filter is implemented in a form of state machine. The purpose of this filter is to eliminate of pulses generated during small amplitude motion oscillation or electrical noise.

Another block is the block of detection of motion direction. The detection of motion direction is based on the pulses sequence appearance in A channel and B channel. There is tested state of signals in A channel and B channel (Fig. 5). The change of motion direction is recognized when state of signals in both channels is different and sequence change state in A and B channels is different [1].

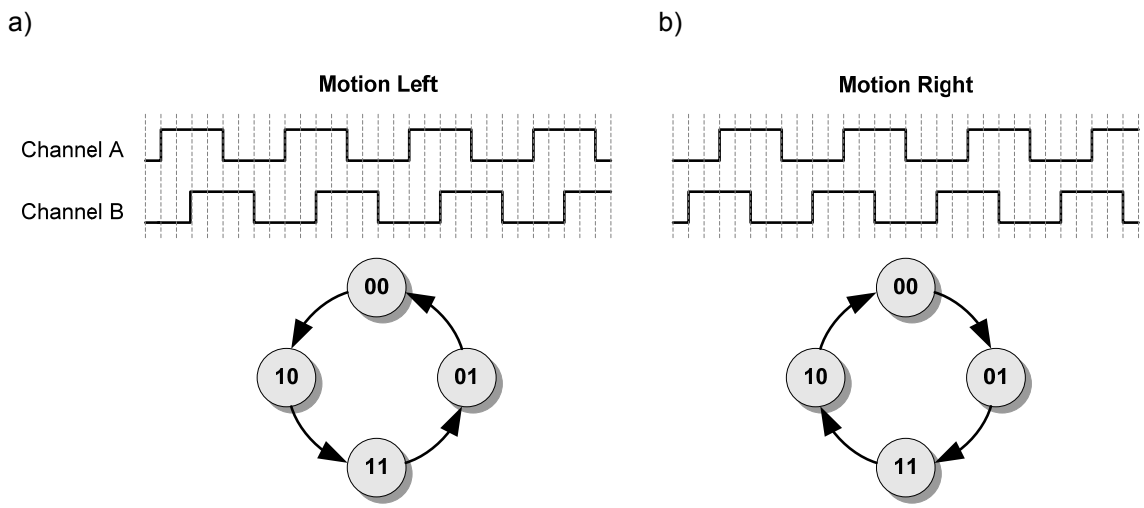

Fig. 5. Motion direction designate by motion direction block:
a) broken line – channels A and B state testing, b) proper A and B channels state for right and left motion direction

Output signals from this block are: direction signal and clock pulses CNT for the position and speed block (Fig. 3). The clock pulses CNT are set on rising and reset on falling edges of coming pulses from A channel or B channel [4].

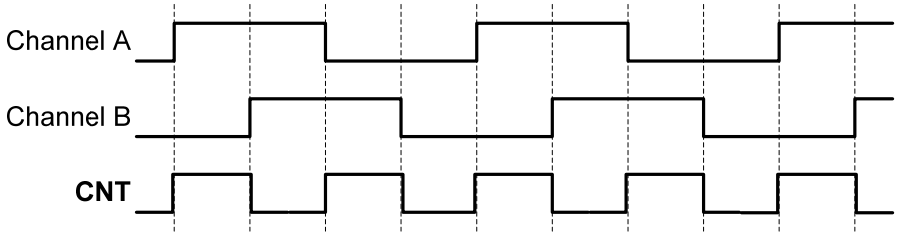

Fig. 6. Clock pulses from motion direction block

The speed and position block is composed of two counters. The position and speed counters count on rising and falling edges of CNT pulses from motion direction block. The resolution of the measuring system is four times bigger in relation to one channel encoder resolution.

The position counter is 32 bits length. The speed counter counts pulses from the direction block in fixed period time. It is 16 bits length.

The system enables cooperation with a C channel.

The position and speed measurement module has been implemented in Spartan-3E XC3S1600 device by means of VHDL language. To test of the

module the serial RS-232 interface was implemented also. As a prototyping platform was used Xilinx MicroBlaze Development Kit 1600 Edition, with FX2-WW extensions card of Digilent.

4. EXPERIMENTAL RESULTS

The measurement station for testing presented position and speed measurement module implemented in FPGA device is shown in Fig. 7.

a)

b)

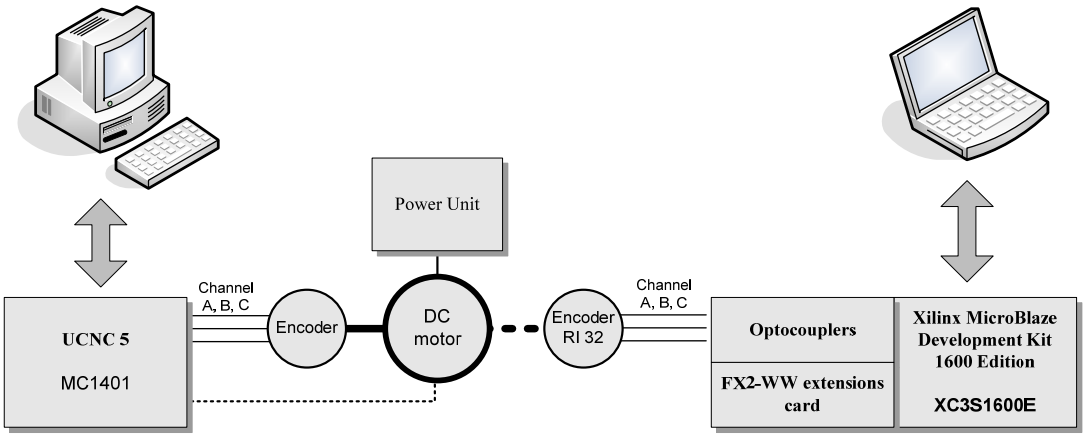

Fig. 7. The measurement station:
a) photograph of station, b) block diagram of the station

The station is composed of:

- DC motors with reference encoder (5000incr/rev) and tested encoder (RI32 5000 incr/rev),
- PC computer with expansion motion card based on MC1401A motion processor of PMD,
- PC computer with tools software in LabVIEW to visualisation results of tests of module,
- Tested position and speed measurement module implemented in XC3S1600E device.

The PC computer with expansion motion card was used to programming DC motors movement and to measure reference speed and position. The second computer with tools software was connected via RS232 interface to Xilinx MicroBlaze Development Kit 1600 Edition with XC3S1600E device. It was used to visualisation speed and position from the measurement module and compare them with reference position and speed received from expansion motion cards.

The tested encoder RI32 was connected to measurement module by 5 m shielding wire placed nearby DC motor and power unit. The connection of encoder to measurement module was realized by means of optocouplers.

The tests was realized for different motion programme. The most important was oscillation movement with different period time and displacement. The maximal speed was 3000 rev/min.

The realized tests proved good speed and position measurement by the module. The module was electrical noise immune in tested noise environment.

During the tests there appears position difference between position from expansion card and module. The difference don’t exceed 1 pulse and don’t increased.

5. REMARKS AND CONCLUSION

The presented module implemented in FPGA structure with incremental encoder is used to speed and position measure mainly in servo-drives. It is possible to implement in various FPGA devices. The module is a part of motion processor destined to control DC and PMSM motors. The realized tests confirm correct speed and position measurement. The module will be more tested for bigger rotary speed and bigger encoder resolution.

LITERATURE

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MODUŁ POMIARU PRĘDKOŚCI I POŁOŻENIA ZAIMPLEMENTOWANY W STRUKTURZE FPGA

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STRESZCZENIE *W artykule przedstawiono zaimplementowany w układzie FPGA (ang. Field Programmable Gate Array) moduł pomiaru prędkości i położenia. Moduł ten jest częścią procesora ruchu przeznaczonego do sterowania silnikami DC (ang. Direct Current) i PMSM (ang. Permanent Magnet Synchronous Motor). Interfejs wejściowy układu współpracuje z przetwornikami obrotowo-impulsowymi przyrostowymi, zawierającymi dwa wyjścia sygnałowe przesunięte o 90 stopni elektrycznych, oraz wyjście indeksu (1 impuls/obrót) (rys. 1).*

Prezentowany blok realizuje pętle pomiaru prędkości i położenia. Został on zaimplementowany w strukturze układu Spartan-3E firmy Xilinx (rys. 2). Program modułu napisano w języku VHDL. Do symulacji i kompilacji projektu bloku pomiaru prędkości i położenia wykorzystano oprogramowanie ISE.

Moduł ten cechuje odporność na zakłócenia elektryczne. Zawiera on dedykowane filtry cyfrowe, odfiltrowujące zakłócenia wejściowe do modułu (rys. 4).

Bardzo istotnym zagadnieniem jest detekcja kierunku ruchu i pomiar położenia. Prezentowany moduł zawiera rozwiązania zapewniające prawidłową detekcję kierunku ruchu i prawidłowy pomiar poło-

żenia (rys. 5, 6). Jest to szczególnie istotne w przypadku oscylacyjnego ruchu, zwłaszcza gdy przemieszczenia są małe a oscylacje wysokiej częstotliwości. Proste techniki detekcji nie zapewniają właściwego pomiaru, powodując utratę impulsów, bądź zliczają te same impulsy wielokrotnie.

W celu przeprowadzenia badań zbudowano stanowisko badawcze. Przeprowadzono badania modułu pomiaru prędkości i położenia z wykorzystaniem przetwornika obrotowo impulsowego przyrostowego w różnych programach ruchu w środowisku zakłóceń elektrycznych. Wyniki pomiarów porównano z układem referencyjnym zbudowanym na karcie PC z procesorem ruchu MC1401A firmy PMD (rys. 7). Wyniki pomiarów położenia badanego modułu nie różniły się więcej niż o 1 inkrement.

Prezentowany moduł pomiaru prędkości i położenia będzie częścią procesora ruchu zbudowanego w oparciu o układ FPGA.