Invited paper

Challenges in ultrathin oxide layers formation

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Abstract — In near future silicon technology cannot do without ultrathin oxides, as it becomes clear from the „Roadmap'2000". Formation, however, of such layers creates a lot of technical and technological problems. The aim of this paper is to present the technological methods that potentially can be used for formation of ultrathin oxide layers for next generations ICs. The methods are briefly described and their pros and cons are discussed.

Keywords — silicon technology, oxidation, PECVD, RTO, gate oxide, ultrathin layers.

1. Introduction

The ultrathin silicon oxide layers have been within the scope of interest of researchers for many years, now. However, only recently, this topic has become of great importance to ICs manufacturers. They have created an extreme pressure, which results in great number of works on the problems related with ultrathin oxide manufacturing, characterisation and reliability. The reasons are clear when looking at „Roadmap'2000" (see Table 1). It is not only that within two to three years the equivalent oxide thickness is expected to fall below 1.5 nm, but also, that the methods of its formation in this thickness range is not known.

The roadmap, however, does not explain the physical background of these revolutionary steps. These physical reasons are, obviously, dependent on the type of the semiconductor device considered. Thus, for MOSFETs, where ultrathin oxides are used for **gate dielectrics**, the reasons for their thickness reduction are:

- to increase transconductance, as: $g_m \sim C_{ox} \sim \varepsilon_{ox}/t_{ox}$;
- to avoid short channel effects, as: $t_{ox} \sim 1/\lambda$;
- to minimise parasitic oxide charge effect.

In DRAMs, such layers are used for **capacitor dielectric**, and their reduction allows farther reduction of area covered by capacitors A_C, while maintaining minimum storage charge, as: $Q_{\min} \approx V_p C_{ox} \sim V_p A_C \varepsilon_{ox}/t_{ox}$.

In EEPROMs and Flash EPROMs, where they are used as **injection dielectric** farther reduction of these layers thickness results in increase of injection efficiency, as $I_{tunnel} \sim \exp(-\beta/t_{ox})$.

In all these applications, lists of prime parameters to be obtained are little different, still, in all of them these layers are playing very important role in device operation.

In some of the presented above cases dependencies shown prove, that reduction of dielectric layers thickness can be compensated by increase of dielectric layer permittivity. This is a promising sign, as further reduction of dielectric layer thickness is very limited due to basic physical limitations (one cannot form continuous layer of less that one monolayer thickness, although such thin layer would have unacceptably low reliability). Another words, by changing the dielectric layer from the so far used silicon oxide to the material characterised by higher than the oxide permittivity value, we can achieve the same goals without farther reducing the dielectric layer thickness. In fact, this move should also to be taken into account when looking for the next stage ultrathin gate dielectric technology.

2. What does define final oxide thickness?

If we compare the size of a SiO_2 molecule with expected thickness of the ultrathin oxide layer, that we want to obtain in the real device, we realise, that the layers we are dreaming about in the future are only few (two to three) monolayers thick[1]. This thickness is also comparable with the thickness of interface region (as it was determined some years ago by HRTEM method), interface roughness and „natural oxide"[2] thickness. Thus, it becomes clear, that all the situations where silicon can become oxidised have to be taken into account when ultrathin oxide growth is studied. The final oxide thickness is determined by following processes:

- silicon surface cleaning process;
- oxidation process (in case of thermal oxidation this would include all its individual stages, namely: preoxidation stage heating up, oxidation itself, and post oxidation – e.g. POA if applicable).

During the „silicon era" few different approaches for silicon cleaning have to be distinguished and shortly discussed in reference to the main technological aim – i.e. formation of ultrathin oxides on Si surface.

[1] We have to realise, however, that due to the amorphous character of the oxide layer, the oxide thickness cannot be, for formal reasons, expressed in number of monolayers.

[2] The „natural oxide" is an oxide of poor quality spontaneously grown when the bare silicon surface is exposed to the ambient atmosphere (unless is purposely hydrogen terminated).

Table 1
Long term roadmap

Indicators	Years					
	1999	2002	2005	2008	2011	2014
Technology node [nm]	180	130	100	70	50	35
T_{ox} equivalent OET [nm]	$1.9 \div 2.5$	$1.5 \div 1.9$	$1.0 \div 1.5^{*)}$	$0.8 \div 1.2^{*)}$	$0.6 \div 0.8^{*)}$	$0.5 \div 0.6^{*)}$
MPU gate length post etch [nm]	140	90	65	45	30	20
*) Technology of these dielectric layers is not yet known.						

The original „RCA method" proposed by Kern [1] has been focused on leaving the silicon surface unprotected, however, with minimum oxide layer on its top. It consisted of S.C.-1 and S.C.-2 being followed by HF etching of silicon oxide, as last treatment. Due to extremely high reactivity of bare silicon surface, „natural oxide" was growing spontaneously afterwards. As a result of that, the starting point for silicon oxidation would strongly depend on the time spent between HF last etching and the beginning of the oxidation process. It is important to realise that the quality of the „natural oxide" (as it grows in clean-room atmosphere) is very poor in both, purity and defects.

Realising the fact, that inevitably, at the beginning moment of oxidation we have certain thickness of natural oxide, the approach has been changed to „better good purity than poor". In practice this has ment, that HF etching has been moved in-between the S.C.-1 and S.C.-2 processes. The S.C.-2, being the last in this sequence, left the silicon surface covered with some 1.5 nm to 2.0 nm of the „chemical oxide", which was still of poor quality, but at least was grown in controlled, chemical ambient. Thus, „chemical oxide" exhibited better than „natural oxide" purity and did not change its thickness in time giving reasonable and repeatable starting point for the standard oxidation process.

When ultrathin oxides are to be formed (e.g. below 3.0 nm), however, even the lower range of the „chemical oxide" thickness is difficult to accept. Thus, a lot of the pressure has been made to find out some other possible cleaning procedures, which would result in still thinner oxide to start oxidation from. This has led to the hydrogen passivated silicon surfaces, in which pretty stable Si-H bonds are created at the silicon surface, by HF last etch. In fact, only these procedures allow the growth of ultrathin oxide in a controllable way starting from basically bare silicon surface.

The oxidation process is also not a one step process, thus, the oxide growth can take place during all of them. The schematic view of the processing stages for the thermal oxidation is shown in Fig. 1. In fact, oxide growth can take place any time when hydrogen termination is removed (due to elevated temperature or even intensive rinsing in water). Thus, in the thermal processing, the silicon surface is prone to oxidation already during the temperature ramp up and temperature stabilisation stage, and later, also during the post oxidation annealing – POA (if applicable),

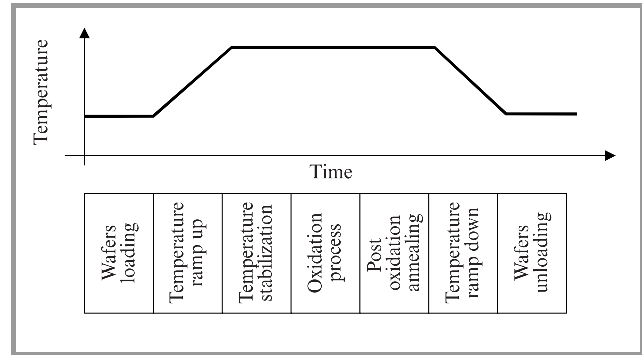

Fig. 1. The schematic view of the temperatures in the furnace during all the stages of the thermal oxidation process performed in the classical furnace.

or temperature ramp down. As a consequence, the finally obtained oxide thickness can differ from the assumed one determined basing on the kinetics of the oxidation process used only. This problem will be discussed in more detail in paragraphs below.

3. High temperature thermal oxidation in classical furnace

3.1. Kinetics of thermal oxidation

The kinetics of thermal oxidation process has been studied already for many years. The most important problem to overcome in these studies was how to avoid the mentioned above influence of pre- and post-oxidation steps on the oxide growth. The only group that succeeded in this respect was Young et al. [2], who installed ellipsometer in their furnace, allowing *in situ* dynamic readout of the oxide growth[3]. However, also this experimental set up required that the important assumptions had to be made – namely, they had to assume the refractive index temperature dependence.

[3]Although such experiments gave a lot of information for studies on oxidation kinetics, from practical point of view they were of practically limited use, as for real processing it is the final oxide thickness (including the influence of pre- and post-oxidation stages) that matters.

The well known set of curves they received is shown in Fig. 2. The first obvious consequence of these curves is that ultrathin oxides require extremely short oxidation times, particularly for higher oxidation temperatures. For example, formation of ultrathin oxide in 1000°C takes, according to the presented curves, few minutes only.

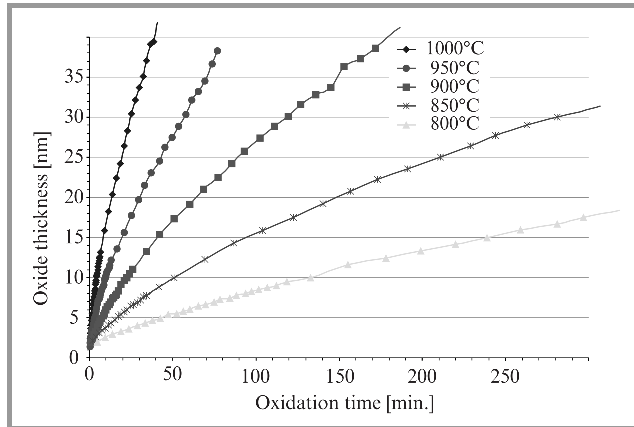

Fig. 2. Kinetics of thermal oxidation in the range of ultrathin and very thin oxide layers for exemplary temperatures from the range between 800°C and 1000°C.

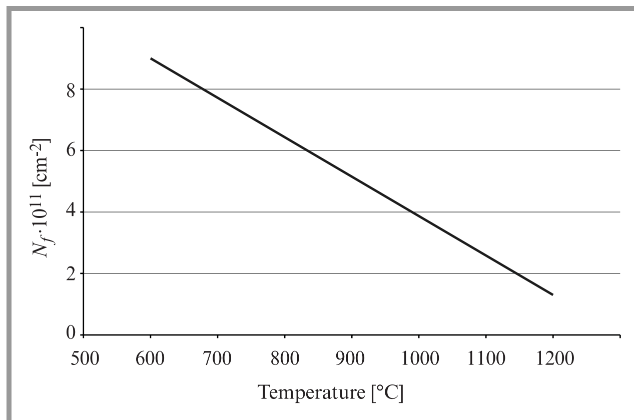

Fig. 3. The experimentally obtained relation of N_f (density of fixed oxide states) versus oxidation temperature, showing the relation of oxide quality with the temperature of its formation.

Much more controllable, in this thickness region, is oxidation in lower temperatures (e.g. 800°C), however it is widely known (see Fig. 3) that higher is the oxidation temperature the better is oxide quality (this relation is also known as „Deal's triangle"). Thus, some sort of compromise has to be reached. It seems that these compromises are set differently in different companies, according to their previous experience and technological skills.

It has been already shown before [3, 4] that oxidation rate can also be decreased by reducing the oxygen partial pressure during the process. The reduction of oxygen partial pressure can be performed either by running the process under the vacuum conditions (with some oxygen refilling) or by oxygen mixing with the neutral ambient gas (like argon). Although the former solution requires dedicated, vacuum tight set up – the latter one can be performed in classical furnace, only after some minor modifications.

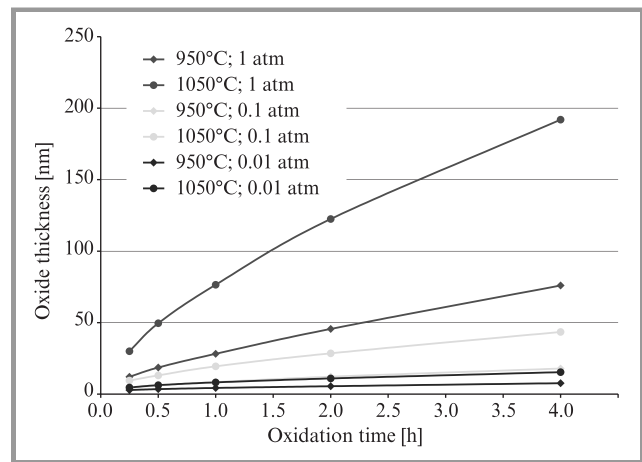

Fig. 4. The experimentally obtained kinetics of high temperature oxidation under the reduced pressure conditions, showing that by reducing the oxygen partial pressure one can significantly slow down the oxidation rate for given process temperature.

The exemplary kinetics of such oxidation is presented in Fig. 4. One can realise that from the ultrathin oxide layer formation, the interesting oxygen partial pressure would be of the order of 0.001. One has to realise, however, that mixing of gases in such proportions is not a trivial problem.

3.2. Issues resulting from furnace construction

3.2.1. Gas exchange rates

The horizontal furnaces are, in order to allow simultaneous processing of few wafers lots, is about 2 m long, while the tube diameter is wafer size dependent. This results in very high volumes of the furnace tubes, which has crucial consequences as far as the gas exchange issue is considered. For the sake of simplicity we will consider in our discussion below oxidising gas as pure oxygen, although, in reality, oxidising gas may be a mixture of oxygen and ambient gas (nitrogen or argon) and/or chlorium containing gases (e.g. HCl or TCE). The oxidation time is, then, determined technically by the time between mass flow controller (MFC) on oxygen gas line is turned on (to begin oxidation) and then off (to end the process). The situation looks totally different from the wafers located along the furnace tube in the quartz boats point of view. Prior to oxidation start the furnace tube is filled with ambient gas (usually nitrogen or argon) with some very small addition of the oxygen (to avoid pitting), which has been flowing through it during the previous stages of the process (namely, during: loading the tube, heating up the whole furnace and temperature

stabilisation). The oxygen getting through the tube end replaces the previous gas composition gradually (see Fig. 5). Assuming, for the sake of simplicity, that the „new gas" is replacing „old one" without mixing with it nor any turbulence, the moment that the wafers face oxidising ambient is position (in the tube) dependent. Consequently, the wafers located at the far end of the tube start their oxidation first, while the one close to the loading station – the last. This effect could be reduced (or even eventually compensated) if only the gas replacement after the oxidation process would have the same dynamics (resulting from the same gas flow). However, this simple method does not hold when gas mixing and some turbulence during the gas flow is taken into account.

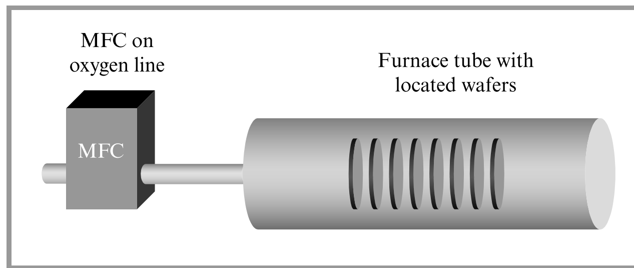

Fig. 5. Schematic view of the classical furnace set up, with the mass flow controller controlling the oxidation time, and wafers located along the furnace tube.

We can, therefore, conclude that some period of wafers oxidation time is basically out of the control and that this time is for particular furnace gas flow rate dependent. In order to reduce it, the possibly high gas flows rates are advantageous.

The gas flow rate is, however, limited from the top by cooling effect of the wafers and creation of turbulence flow within the furnace tube. Particularly the former effect is extremely important in high temperature oxidation, which is so sensitive to the process temperature. Consequently, the gas flow is limited (depending on the diameter of the tube, which in turn depends on the processed wafers diameter) to few standard litres per minute (slm), which when compared with typical volumes of tubes results in at least few minutes of gas replacement stage.

This discussion proves that few minutes of uncontrollable oxidation seem to be unavoidable in oxidation in standard furnaces.

3.2.2. Temperature ramp up and ramp down dynamics

The time length of the temperature ramp up is limited by wafer warpage effect. It is, therefore, determined by the diameter of the wafers used[4], however, for number of years already the 10°C/min has seemed to be the widespread standard value of the ramp up rate. Typical stand-by temperature of the furnace is usually between 700°C and 750°C, hence, even for low oxidation temperatures (like e.g. 800°C) the ramping up must take at least some minutes.

On the contrary to ramping up, the ramping down dynamics is only furnace construction dependent. It has to be pointed out, that it is often even slower than the ramp up rate, thus, we have yet some more minutes of wafers presence in high temperature and, as a result of it – still longer time of probable uncontrollable oxidation.

Traditionally, the post-oxidation period was supposed to be not affecting the control of the oxidation process. This has been true, for thicker oxides, where due to the saturation type of kinetics of oxidation, the rate of oxide growth for thicker oxides is much smaller than for very thin ones. For the ultrathin oxides, however, there is no significant difference between oxide growth rate before and after oxidation process, thus, in this case post-oxidation growth can also influence considerably to the final thickness of the oxide layer. This effect is, thus, also important for the setting POA stage for ultrathin oxide processing.

[4]In order to avoid wafer warpage due to non-uniform wafer heating during the heating process, low ramping rates have to be used.

4. Rapid thermal oxidation

Rapid thermal oxidation (RTO) technique, has been developed as one of the possible applications of rapid thermal processing (RTP) reactors that have been developed in late eighties. Commonly used for very short annealings, RTP reactors, which allow very high temperature processing (often up to 1300°C) and very abrupt temperature changes, have been often considered for oxidation process. As long as the thickness of the oxide to be grown was not so thin, there were no clear advantages of this process versus standard oxidation. Now, when considering ultrathin oxides formation, RTO seems to be very strong candidate to become new standard gate formation technique.

4.1. Kinetics of RTO process

Despite what has been believed at the beginning of its introduction to technology, RTO kinetics is essentially the same as of the standard thermal oxidation performed in the furnace. This point has been proved in [5], where theoretical model of high temperature oxidation successfully fitted to standard oxidation gave also excellent fit for RTO experimental data. The problems from the past where then attributed to poor modelling efforts and ignoring effects important within the region of ultrathin oxide from growth considerations. Important differences, however, do exist, but they refer to the pre- and post-oxidation period, allowing gaining better control over the whole oxidation process. First of all, RTO reactors operate on single wafers, thus, the inner volume of the quartz tube is very small (of the order of few litres only – comparing to the horizontal furnace of several hundreds litres). Hence, in RTO, the gas exchange times are very small indeed.

Also ramping up and ramping down rates are in RTO very high, due to high electric power applied to the heating systems and very small heated mass (one wafer only). The ramping rates of the order of 200°C/s are not uncommon in this type of equipment.

These two features allow solving the problem of too long pre- and post-oxidation stages in ultrathin oxidation.

Extremely fast ramping generates, however, some other problems in RTO processing. The main issue here is uniformity of the temperature across the wafer at all the stages of the process, namely, during: ramp up, oxidation and ramp down. Number of effects affects this uniformity. This results, at the worst case, in build up of dislocations and slip lines within the silicon substrate, thus, these effects they cannot be ignored. The most important of them will discussed briefly below.

In order to obtain so high ramping rate without the wafer warpage, temperature across the wafer has to be uniform during the whole process. Wafer edges, however, radiate out heat much easier than wafer inner part, thus, in order to satisfy this demand, special profile of the energy source radiation has to be executed in the reactor (higher energy at the wafer edges to compensate mentioned above energy loss at the edges)[5]. If this condition is not satisfied, cooler wafer edges create a mechanical stress upon the inner wafer part, which has two different consequences. First, the mechanical stress triggers up the build up of the structural defects in the processed wafers. Secondly, mechanical stress has significant influence upon the kinetics of the oxidation process hence, we may obtain non-uniform oxide thickness. For ultrathin oxide layers, where we hope to control formation of few monolayers of the oxide, lack of uniformity, as well as defects in the silicon substrate, are very important reliability issues. Thus, both effects are dangerous for modern ICs, hence, high priority to solve this problem.

The nature of the heating in RTO reactors is also different than in classical furnaces, as the energy transfer from the source to the wafer takes place, in this case, by photons radiation and not by convection mechanism. Thus, the temperature of the object in the reactor is dependent on the absorption properties of the material to be heated. The obvious consequence of this fact is that silicon wafer which may be covered by various patterned layers (of different absorption properties) can exhibit locally different temperatures. Such temperature differences result in local stress, which after incubation period leads to local defects in the wafer structure. Even local differences in the same type of layer thickness (e.g. field oxide – FOX and gate oxide – GOX) can lead to dislocations, as can be seen in [6]. This is a very serious problem, as no compromise can be made in patterning the layers used for ICs construction (they result from the ICs layouts), nor we can change the types of layers used.

Concluding on RTO, we could say, that two main problems of ultrathin oxidation in standard furnace seem to be solved by the RTO, however, other technological problems are generated by this technique. Still, RTO is obviously among the most important players for extreme ultrathin oxide formation.

[5]Thus, RTO reactors can perform well only for the assumed by manufacturer wafer size.

5. Plasma enhanced chemical vapour deposition

Plasma enhanced chemical vapour deposition (PECVD) is one of the few deposition methods which involves chemical reaction between gas reagents introduced into the reactor, thus, no chemical bonds with the substrate are established. Very important consequence of this fact is that, unlike in thermal oxidation, new layer can be grown on any substrate, as the substrate is not a source of any chemical elements needed for the reaction. Hence, this method gives us a lot technological flexibility. Above all, changing the types of gases supplied to the system, can immediately, without removing the wafer from the system, switch the type of material deposited. Hence, this method can basically be considered not only for single, but also for double, or even multiple layers formation. These are obviously very important pros for CVD techniques.

In PECVD methods very reactive radicals are produced rather by plasma excitation than thermal activation. This allows considerable reduction of temperature required for the CVD process. For example, silicon oxide layers can be formed in temperatures around 150°C ÷ 400°C rather than in 600°C ÷ 1000°C, which drastically reduces „thermal budget" of the ICs manufacturing.

On the other hand, precision of the deposition time control is very good, as due to the facts, that PECVD takes place in vacuum chamber, and the process without plasma basically does not take place.

From the early beginning, however, due to previously mentioned well known relation between the formation temperature and quality of the oxides, PECVD have never been seriously considered for gate oxide layer formation. Thus, the main advantage of this method, as it was believed then, was possibility to manufacture thick dielectric layers at the high deposition rate and very low temperatures. This has oriented PECVD methods for many years mainly for manufacturing thick dielectric films[6]. Even now, most of the process recipes are for processes characterised by deposition rate of the order of 50 nm/min. In order to control well deposition rates within the ultrathin range we require, however, deposition rates at least 10 times lower.

Reoptimising the PECVD process in order to meet such deposition rates is, however, possible although is not a trivial matter – it usually requires some changes in typical set up (e.g. lower MFCs range, or adding gas mixing modules). Then, the problems of non-uniformity and overall

[6]The exception to this rule were investigations of possible use of PECVD ultrathin films for DRAM capacitors (where the requirements for quality of the dielectric layers are much lower), which were carried out since late eighties.

poor quality of the deposited layers still have to be overcome. So far, the properties of PECVD layers have fallen well behind the ones obtained by thermal oxidation (including RTO) but much effort is spent in order to improve the results.

6. Other techniques reported

It is interesting to realise what are other candidates for ultrathin oxide processing. Among them, we have two processes that have been in the waiting-room of the silicon technology already for number of years, namely: plasma anodisation and oxidation. There is also number of completely new techniques around. One of the most interesting among them seems to be GRILOX. Below you will find brief comments on their possible applicability to ultrathin oxides formation.

6.1. Plasma anodisation

Plasma anodisation is a process in which oxygen ions that are produced in plasma region, are transported to the oxide-silicon interface due to the electric field appearing across the already formed oxide (on the top of silicon wafer), where they undergo chemical reaction with silicon atoms that forms silicon oxide layer. This process, as it was proved experimentally many years before [7], allows formation of thin but also ultrathin oxide layers in low temperatures and with the growth rate enabling full control of the process and its automation. The control of the process is very simple, as one measures voltage drop across the sample – plasma system, which value can be scaled vs. oxide thickness.
Due to reasons similar to mentioned in description of PECVD, also in plasma anodisation there is no problem with the pre- and post-oxidation growth (as it was the case for thermal oxidation).
The properties of the obtained oxide layers were reported [8] to be comparable with classical thermal oxidation (especially after performing additional short annealing procedure).
The feature that prevented, in our opinion, previous application of plasma anodisation for silicon processing was the fact, that by its nature the process is single wafer. Nowadays, when more and more processes are performed in single wafer reactors, this is no more a decisive drawback.

6.2. Plasma oxidation

Plasma oxidation instead of using oxygen ions uses oxygen neutral radicals excited in the plasma region. They are eagerly forming the bonds with silicon if they meet them. As the oxygen radicals are not charged, their transport through the already formed oxide layer can take place due to diffusion, which cannot be very effective in low temperature that this process takes place in. Thus, the process kinetics saturates very quickly, at the thicknesses of the order of few monolayers. One cannot control the process very efficiently, however setting the process parameters in such a way that the saturation thickness would be thickness of interest, seems to be very interesting proposal for ultrathin oxide formation in very low temperatures.

Both above mentioned techniques allow basically combining them with some reduced pressure techniques, thus, are prone to farther development when the need of double gate insulators will come.

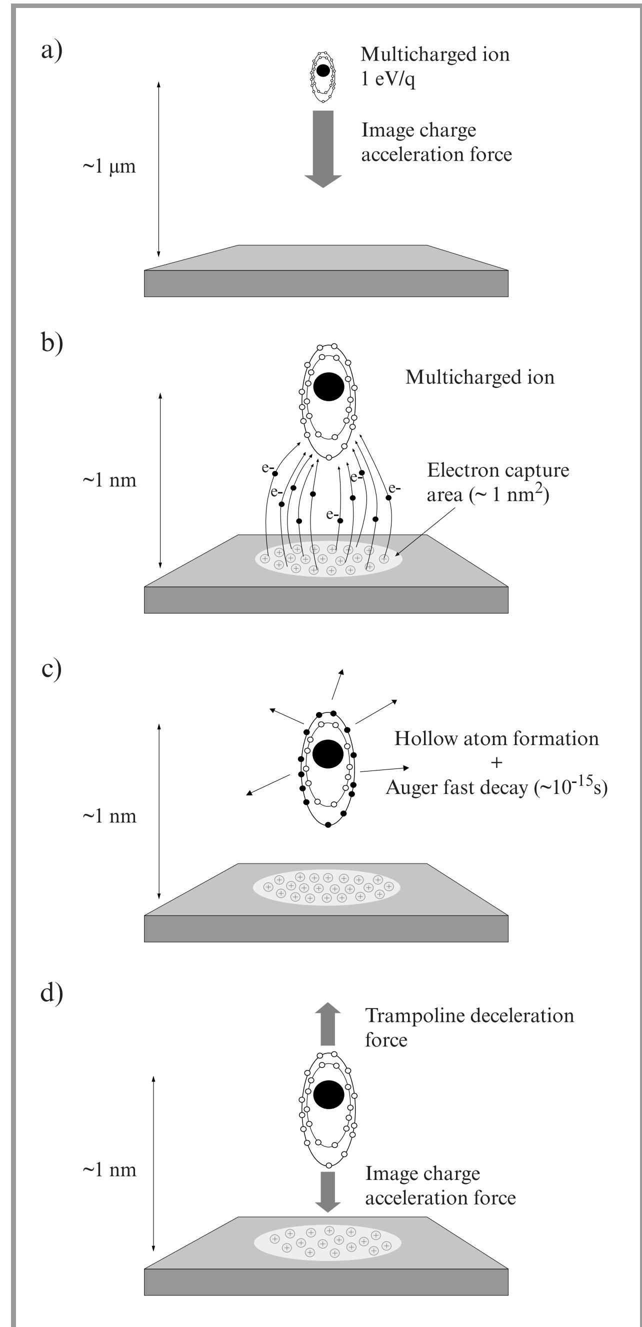

Fig. 6. Schematic view of the stages (a ÷ d) of the GRILOX process leading to the oxidation of the silicon surface by low energy multicharge ions collisionless interaction with the silicon surface [9].

6.3. GRILOX

This method, which is subject to number of patent pendings, and is described in more details for example in [CC], relays on „trampoline effect", which prevents slow multicharged ion bombardment of the solid state surface (see Fig. 6). During this process, surface bonds of the substrate break up and this state can be kept on for some minutes, due to the very high vacuum in the experimental system (10^{-10} Tr). Introduction of some oxygen into the system results in the formation of silicon – oxygen bonds, namely – formation of silicon oxide. As there is no electric field within he already formed monolayers of the oxide layer, there are no means to support oxygen transport through it towards silicon surface (similarly like in plasma oxidation). Thus, process ends very quickly, when only two, three monolayers of oxide are formed. This way the process ends well within interesting region of ultrathin oxide layers and no special control method of oxidation kinetics is required. So far we do not know anything about the properties of ultrathin oxide formed by this method, however, thus, it is too early to calculate its chances in the competition. Still, it certainly is worth noticing and keeping an eye on the results of its development in near future.

7. Conclusions

After the presented above discussion it seems clear, why the „Roadmap'2000" does not specify the technology of the gate dielectrics after 2005 (expected thickness below 1.5 nm). All the discussed methods have some pros and cons. Some, like thermal oxidation have been used for long for GOX in the ICs manufacturing, have very good reputation for the quality of the layers, but bring many problems with the ultrathin oxidation process control. RTO seems to solve some of the problems that classical thermal oxidation has with the process control, however, it brings some others.

PECVD, on the other hand, has never been seriously considered for such demanding process as GOX fabrication, however a lot of effort has been recently spent in order to study possible limits of the obtained layers quality improvement. Still, good control of the process and low temperature make this method worth studying as possible technology of ultrathin GOX.

In respect to plasma anodisation and plasma oxidation one should realise, that the features of these method, which until now, were considered as unacceptable from the mass scale manufacturing point of view, are no more so decisive. Good properties of the anodic oxide, as well as precise control of the process and its low temperature are definitely important factors for these methods.

Finally, one should realise that also completely new methods are appearing (like e.g. GRILOX) and that they need some time to prove weather they can take part in the competition to become next generation technology of the ultrathin gate dielectric, or not.

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