Paper

Characterization of SOI fabrication process using gated-diode measurements and TEM studies

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Abstract — SOI fabrication process was characterized using electrical and TEM methods. The investigated SOI structures included partially and fully depleted capacitors, gated diodes and transistors fabricated on SIMOX substrates. From C-V and I-V measurements of gated diodes, the following parameters of partially depleted structures were determined: doping concentration in both n- and p-type regions, average carrier generation lifetimes in the region under the gate and generation velocity at top and bottom surfaces of the active layer. Structures with short lifetime were studied using a transmission electron microscope. TEM studies indicate that the quality of the active layer in the investigated structures is good. Moreover, these studies were used to verify the thicknesses determined by means of electrical characterization methods.

Keywords — microelectronics, SOI technology, characterization.

1. Introduction

The idea of the investigations was to use nondestructive electrical methods for determining the areas with the highest density of defects and then use TEM to determine the type of the defects. The carrier generation-recombination lifetime is the most sensitive indicator of semiconductor quality. Defects and impurities reduce carrier lifetime, therefore the structures with low lifetime were studied by TEM. The software developed by the authors enables not only carrier lifetime to be extracted from C-V and I-V characteristics but also layer thicknesses and doping concentration.

In our investigations we have used structures from two SIMOX wafers, **A** and **B**, differing in the thickness of the active layer. In both cases the gates were made of poly-Si. The structures fabricated on wafer **A** were partially depleted, while those fabricated on wafer **B** – fully depleted.

2. Electrical measurements

Initially the basic parameters of SOI structures were determined using C-V and I-V characteristics. The characteristics were measured simultaneously in order to reduce temperature related errors. Software with statistical methods implemented was used to reduce noise and disturbances for currents as low as 10^{-13} A.

Using the method described in [1] the thicknesses of the layers were calculated from C-V characteristics. The results are presented in Table 1.

The doping concentration versus depth for partially depleted SOI devices, calculated from C-V characteristics, is presented in Figs. 1 and 2. The dotted lines are placed

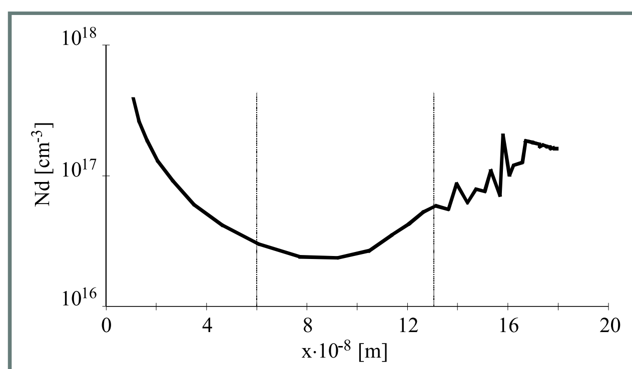

Fig. 1. Typical doping concentration versus depth for n-type area.

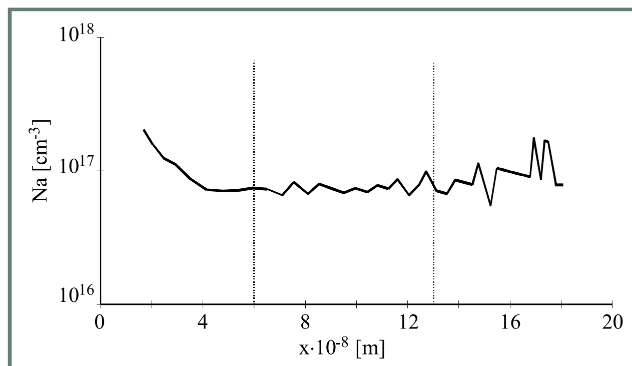

Fig. 2. Typical doping concentration versus depth for p-type area.

at the distance of three Debye lengths from top and bottom interface, therefore the results from the region within these lines should be correct. Also the average doping concentration was calculated. The following results were obtained: $Nd = 5.5 \div 8.6 \cdot 10^{16}$ [cm^{-3}] for n-type area and $Na = 7.3 \div 9.3 \cdot 10^{16}$ [cm^{-3}] for p-type area.

Using the method described in [2–4] the generation carrier lifetime and surface generation velocity in partially depleted structures were extracted from I-V characteristics measured

Table 1
The thicknesses calculated from C-V characteristics

Wafer	A [μm]	B [μm]
Gate oxide over the n-type region	0.031 ÷ 0.0325	0.0161 ÷ 0.0179
Gate oxide over the p-type region	0.032 ÷ 0.033	0.0175 ÷ 0.0177
Active layer of the n-type region	0.178 ÷ 0.185	0.080 ÷ 0.090
Active layer of the p-type region	0.184 ÷ 196	0.0776 ÷ 0.98

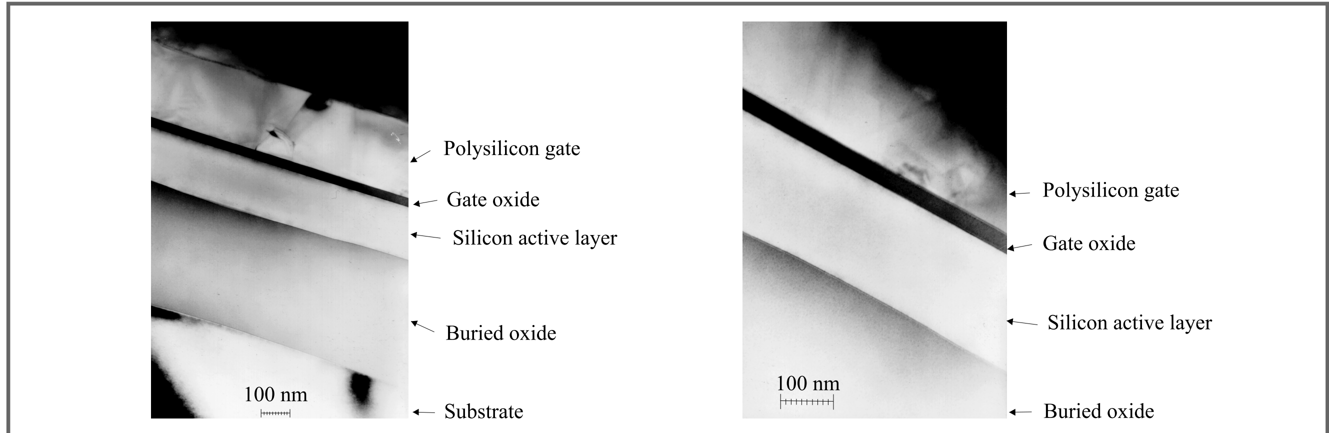

Fig. 3. Cross sectional TEM micrographs of type A SOI structures for two different magnification.

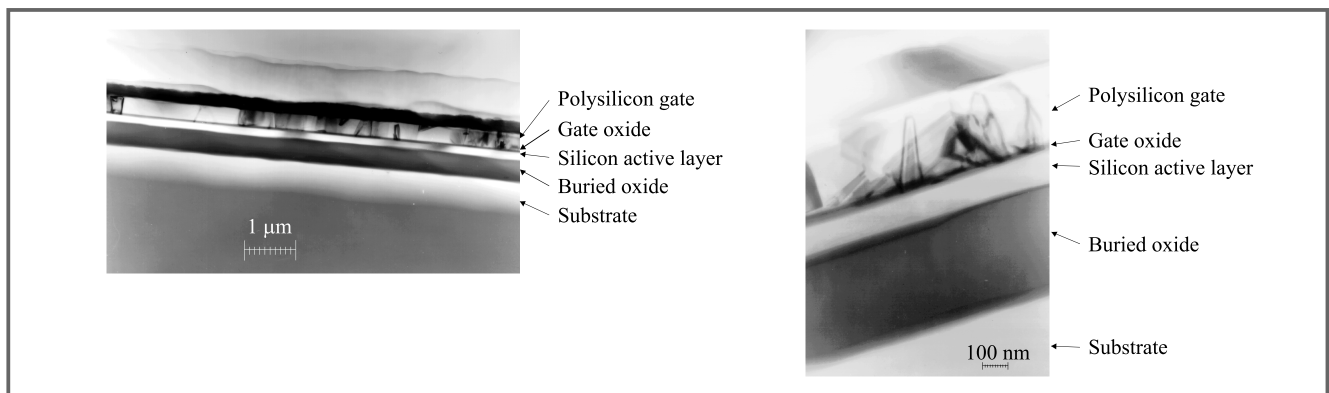

Fig. 4. Cross sectional TEM micrographs of type B SOI structures for two different magnification.

versus front gate voltage and back gate voltage. The calculation yielded generation lifetime $\tau_g = 0.45\ \mu s \div 0.6\ \mu s$ and the generation velocity at the front surface $s_g = 5.6 \div 9.1$ [cm/s] and the back surface $s_b = 5.1 \div 8.4$ [cm/s].

For fully depleted structures carrier recombination lifetime was calculated using the model described in [5]. The recombination time values ranged from 0.45 μs to 0.94 μs.

3. TEM studies

The structures with the minimum values of generation and recombination lifetime were investigated using TEM. The cross sectional TEM micrographs of both types of the structures A and B are presented in Figs. 3 and 4.

Although the investigated samples were prepared specifically to facilitate the observation of defects, no defects were observed in the active silicon layer. Only poly-Si grains were visible. Thickneses of the layers were determined from TEM micrographs. The results are presented in Table 2.

Table 2
The thicknesses determined from TEM micrographs

Wafer	A [μm]	B [μm]
Gate oxide	0.030 ÷ 0.032	0.0178 ÷ 0.018
Active silicon layer	0.18 ÷ 0.19	0.11 ÷ 0.12
Buried oxide	0.40 ÷ 0.42	0.35 ÷ 0.42

In case of partially depleted structures the agreement between the thicknesses determined electrically and those determined with TEM is excellent. However, in case of fully depleted devices the thickness of active layer measured electrically is too low. It is possible that for this case the thicknesses of accumulation and inversion layers must be

taken account. Gate oxide thickness obtained from TEM is probably too high because of the difficulties with precise determination of the layer edges.

4. Conclusions

The developed methods may be used to monitor the SOI fabrication process. The fundamental parameters of SOI devices are determined including the carrier lifetime – a comprehensive indicator of process quality. The software enabling very low currents to be measured and the whole measurement system may be used in many research areas. The developed method of preparing SOI samples for TEM studies at precisely determined locations of test structures increases the probability of observing defects in which the experimenter is interested. The method may be efficiently used to examine semiconductor materials.

Acknowledgement

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Andrzej Jakubowski – for biography, see this issue, p. 18.

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