Invited paper

On the extraction of threshold voltage, effective channel length and series resistance of MOSFETs

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Abstract — The first part of this article presents the modeling of the long-channel bulk MOSFET as a particular case of the SOI MOSFET. The second part reviews compares and scrutinizes various methods to extract the threshold voltage, the effective channel and the individual values of drain and source resistances. These are important device parameters for modeling and circuit simulation.

Keywords — threshold voltage, channel length, series resistance, parameter extraction.

1. Introduction

Since the early 1980s, the MOSFET has become the most widely used semiconductor device in very large scale integrated circuits. This is due mainly to the fact that the MOSFET has a simpler structure, costs less to fabricate, and consumes less power than its bipolar transistor counterpart.

In this article, we will first present, in Section 2, an overview of the modeling of long-channel bulk MOSFET [1–11] as a particular case of the long-channel SOI MOSFET [12–16]. Then, we will focus on issues related to extraction of MOSFET device parameters [17–20] and it will be organized into three sections. Section 3, covers the topic of extracting the threshold voltage. An overview is first provided to discuss and compare the advantages and disadvantages of various existing extraction methods for the threshold voltage.

Section 4 is concerned with the various methods for extracting the effective channel length, probably the most important device parameter of the MOSFET. They include a method based on metallurgical junctions, current-voltage method, capacitance-voltage method, shift and ratio method, and a method based on device simulation. The procedures and developments of these methods are discussed and their accuracy, advantages, and disadvantages are compared.

Section 5 deals with the extraction of the drain and source resistances of MOSFETs, which are important device parameters in characterizing the voltage drops in the drain and source regions of these devices.

2. MOSFET modeling

The fundamental benefits of the silicon-on-insulator (SOI) structure over the traditional bulk MOSFET have motivated considerable recent research work [12–16]. The main benefits include suppression of latch-up, higher circuit speed, lower power consumption, greater immunity to radiation, increase of the density, 3D integration, and reduction of short-channel effects. Good review articles were presented recently by Jurczak [14] describing and comparing the various SOI's models, and by Alles [13] scrutinizing the motivations of using SOI in integrated circuits.

Probably the most important motivation today for using the SOI device is the lower power consumption, especially in the portable electronics arena where the supply voltage is reduced in order to decrease the power consumption. If the supply voltage is reduced, the threshold voltage must also be reduced. However, the degree of the reduction of the supply and threshold voltages is limited by the subthreshold slope, which is defined as the gate voltage required to increase the drain current by one order of magnitude in weak inversion. The SOI device has a larger subthreshold slope and thus a lower leakage current than its bulk counterpart. This allows the use of a SOI MOSFET with a small threshold voltage, thus the use of a smaller supply voltage, without having to be concerned with a significant leakage current. On the other hand, for the bulk MOSFET, a large threshold voltage, and thus a large supply voltage, is needed to ensure a small leakage current in the device.

2.1. Modeling of the (SOI) MOSFET

Figure 1 gives the schematic of silicon-on-insulator MOSFET. It can be seen that the main feature differentiating the SOI MOSFET from its bulk counterpart is the fact that the SOI MOSFET has both front and back oxide interfaces and therefore is subjected to charge coupling effects between the two gates. The bulk MOSFET can therefore be considered as a special case of an SOI MOSFET with a very large semiconductor film thickness. The mixed boundary condition at the front oxide-silicon interface yields

$$V_{GS}^{f} - V_{FB}^{f} = \Psi_{Sf} + \frac{\varepsilon_s \xi_{Sf}}{C_{of}} , \qquad (1)$$

where V_{GS}^{f} is the front-gate voltage, V_{FB}^{f} is the front-flatband voltage, C_{of} is the front-oxide capacitance, Ψ_{Sf} is the front-

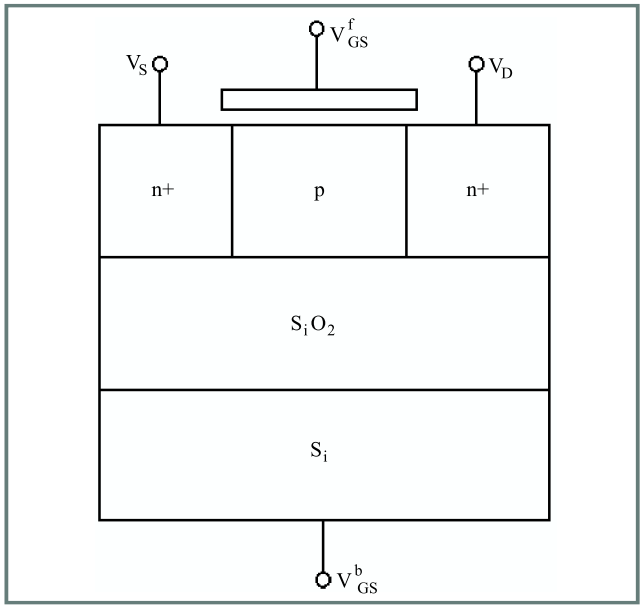

Fig. 1. A two-dimensional SOI MOSFET structure showing the top and bottom Si-SiO_2 interfaces.

surface band bending and ξ_{Sf} is the front-surface electric field.

On the other hand, at the back oxide-silicon interface, the boundary condition is

$$V_{GS}^b - V_{FB}^b = \Psi_{Sb} - \frac{\varepsilon_s \xi_{Sb}}{C_{ob}} , \tag{2}$$

where V_{GS}^b is the back-gate voltage, V_{FB}^b is the back-flatband voltage, C_{ob} is the back-oxide capacitance, Ψ_{Sb} is the back-surface band bending and ξ_{Sb} is the back-surface electric field. The front-interface ($x = 0, \Psi = \Psi_{Sf}$ and $\xi = \xi_{Sf}$) and at the back-interface ($x = t_b, \Psi = \Psi_{Sb}$ and $\xi = \xi_{Sb}$), are related by [14–16,18]:

$$\xi_{Sf}^2 - F^2(\Psi_{Sf}, V) = \xi_{Sb}^2 - F^2(\Psi_{Sb}, V) \equiv \alpha , \tag{3}$$

where $F^2(\Psi, V)$ is the Kingston function defined by [4]:

$$F^2(\Psi, V) \equiv \int \frac{-2\rho}{\varepsilon_s} d\Psi = $$
$$= \frac{2}{\beta^2 L_D^2} \left(\left(e^{-\beta\Psi} + \beta\Psi - 1 \right) + \right.$$
$$\left. + \frac{n_o}{p_o} \left(e^{-\beta V} \left(e^{\beta\Psi} - 1 \right) - \beta\Psi \right) \right) \tag{4}$$

and α, unlike the bulk MOSFET, is not equal to zero but is a parameter that quantifies the charge coupling between the front- and back-gates. Here, p_o and n_o are the equilibrium hole and electron densities, $\beta = q/kT$ is the inverse of the thermal voltage, and L_D is the extrinsic Debye length given by

$$L_D = \left(\frac{\varepsilon_s}{q\beta\, p_o} \right)^{1/2} . \tag{5}$$

Finally, the semiconductor film thickness t_b can be expressed by

$$t_b = \int_{\Psi_{Sb}}^{\Psi_{Sf}} \frac{d\Psi}{\xi} . \tag{6}$$

The values of $\Psi_{Sf}, \Psi_{Sb}, \xi_{Sf}$ and ξ_{Sb} can be calculated numerically from Eqs. (3)–(6).

The drain current for the SOI MOSFET can be expressed by the following single-integral equation [16]:

$$I_D = \mu_n \frac{W}{L_{eff}} \left[C_{of} \left(\left(V_{GS}^f - V_{FB}^f \right) \left(\Psi_{SfL} - \Psi_{Sfo} \right) + \right. \right.$$
$$\left. - \frac{\left(\Psi_{SfL}^2 - \Psi_{Sfo}^2 \right)}{2} \right) + \frac{Q_b n_o^2}{\beta} \left(\beta V_{DS} + e^{-\beta V_{DS}} - 1 \right) +$$
$$+ \varepsilon_s \int_{\Psi_{Sbo}}^{\Psi_{Sfo}} \xi\left(\Psi, V = 0\right) d\Psi - \varepsilon_s \int_{\Psi_{SbL}}^{\Psi_{SfL}} \xi\left(\Psi, V = V_{DS}\right) d\Psi +$$
$$+ \frac{\varepsilon_s t_b \left(\alpha_L - \alpha_o \right)}{2} + \tag{7}$$
$$\left. + C_{ob} \left(\left(V_{GS}^b - V_{FB}^f \right) \left(\Psi_{SbL} - \Psi_{Sbo} \right) - \frac{\left(\Psi_{SbL}^2 - \Psi_{Sbo}^2 \right)}{2} \right) \right] ,$$

where Q_b is the body depletion charge ($Q_b = -qN_A t_b$), $\Psi_{Sf}(y = y_s) = \Psi_{Sfo}$, $\Psi_{Sf}(y = y_d) = \Psi_{SfL}$, $\Psi_{sb}(y = y_s) = \Psi_{Sb}$, $\Psi_{Sb}(y = y_d) = \Psi_{SbL}$, $\alpha(y = y_s) = \alpha_o$, $\alpha(y = y_d) = \alpha_L$, and $L_{eff} = (y_d - y_s)$ is the effective channel length.

2.2. Pierret-Shield's model

For a very large t_b, as would be the case for a bulk MOSFET, the charge coupling between the front- and back gate diminishes, and α_o and α_L approach zero. Also, for this case, there will be a point x_o inside the semiconductor at which $\Psi(x = x_o) = \xi(x = x_o) = 0$. Taking the point x_o to be the back interface, we get $\Psi_{Sbo} = \Psi_{SbL} = 0$, and Eq. (7) reduces to Pierret-Shield's model [8] for the bulk MOSFET:

$$I_D = \mu_n \frac{W}{L_{eff}} \left[C_o \left(\left(V_{GS} - V_{FB} \right) \left(\Psi_{SL} - \Psi_{So} \right) + \right. \right.$$
$$\left. - \frac{\left(\Psi_{SL}^2 - \Psi_{So}^2 \right)}{2} \right) + \varepsilon_s \int_0^{\Psi_{So}} F\left(\Psi, V = 0\right) d\Psi +$$
$$\left. - \varepsilon_s \int_0^{\Psi_{SL}} F\left(\Psi, V = V_{DS}\right) d\Psi \right] , \tag{8}$$

where $\Psi_S(y = y_s) \equiv \Psi_{So}$ and $\Psi_S(y = y_d) \equiv \Psi_{SL}$. This model is also valid for long-channel MOSFETs under all inversion conditions.

2.3. Charge-sheet model

It should be pointed out that using the following empirical approximation,

$$\left(F^2\left(\Psi, V\right) \right)^{1/2} \approx$$
$$\approx \frac{2^{1/2}}{\beta\, L_D} \left(\left(\beta\, \Psi - 1 \right)^{1/2} - \frac{\left(\beta\, \Psi - 1 \right)^{-1/2}}{2} \right) , \tag{9}$$

Pierret's model yields to the charge-sheet model [1, 9, 10] defined by

$$I_D = \mu_n \frac{W}{L_{eff}} \left[C_o \left((V_{GS} - V_{FB})(\Psi_{SL} - \Psi_{So}) - \frac{(\Psi_{SL}^2 - \Psi_{So}^2)}{2} \right) + \right.$$
$$- \frac{qN_A L_D 2^{3/2}}{3} \left((\beta\Psi_{SL} - 1)^{3/2} - (\beta\Psi_{So} - 1)^{3/2} \right) +$$
$$\left. + qN_A L_D 2^{1/2} \left((\beta\Psi_{SL} - 1)^{1/2} - (\beta\Psi_{So} - 1)^{1/2} \right) \right]. \quad (10)$$

This model, which is also valid for long-channel MOSFETs under all inversion conditions, has an error of 5% or less compared the Pao-Sah counterpart. This model has been classically derived from the assumption that the inversion charge is an infinitesimally thick layer near the interface.

2.4. Strong inversion model

The drain current models discussed above can be simplified under the strong inversion condition. For this case, the surface band bending increases very little with increasing gate bias and this allows one to assume that band bending is nearly independent of the gate bias under strong inversion. Thus,

$$\Psi_{So} \approx 2\phi_B \,, \quad (11)$$

at the source, and

$$\Psi_{SL} \approx 2\phi_B + V_{DS} \,, \quad (12)$$

at the drain where ϕ_B is the bulk potential. Also, under strong inversion, the inequality $\beta\Psi >> 1$ is valid, and Eq. (4) can be approximated by

$$F^2(\Psi, V) \approx \frac{2\Psi}{\beta L_D^2} \,. \quad (13)$$

Putting Eqs. (11)–(13) into Eq. (8), and integrating the resulting equation yields the following analytic expression for the drain current:

$$I_D = \mu_n \frac{W}{L_{eff}} C_o \left[\left(V_{GS} - V_{FB} - 2\phi_B - \frac{V_{DS}}{2} \right) V_{DS} + \right.$$
$$\left. - \frac{2(2\varepsilon_s q N_A)^{1/2}}{3C_o} \left((V_{DS} + 2\phi_B)^{3/2} - (2\phi_B)^{3/2} \right) \right] . \quad (14)$$

It is important to mention that the model in Eq. (14) is valid only when the inversion layer is present in the entire channel, a case which holds for a relatively small drain voltage.

2.5. SPICE model

The simplest MOSFET SPICE model (i.e., level-1 model) [3–6] can be obtained as follows. Consider the case of strong inversion and assume

$$V_{DS} \gg 2\phi_B \,. \quad (15)$$

Next, using the Taylor's series to approximate the terms having the power of 3/2 in Eq. (14), one obtain:

$$I_D = \mu_n \frac{W}{L_{eff}} C_o \left[V_{GS} - V_T - \frac{V_{DS}}{2} \right] V_{DS} \,, \quad (16)$$

where

$$V_T \equiv V_{FB} + 2\phi_B + \frac{2(\varepsilon_s q N_A \phi_B)^{1/2}}{C_o} \quad (17)$$

is the threshold voltage. Equation (17) can be rewritten by noting that its last term is related to the maximum depletion charge Q_{dmax} (i.e., Q_d becomes Q_{dmax}) which occurs at the onset of inversion,

$$V_T \equiv V_{FB} + 2\phi_B - \frac{Q_{dmax}}{C_o} \,. \quad (18)$$

It is important to point out that Eq. (17) is valid only when the substrate voltage V_{BS} is zero (i.e., no body effect). On the other hand, Eq. (18) is more general and is valid with the presence of body effect, provided the depletion charge accounts for the effect of V_{BS}.

Clearly, the threshold voltage is an important parameter for modeling the MOSFET. Beside modeling V_T, as was done in Eqs. (17) and (18), such a parameter can be determined by extraction methods, which will be discussed in detail in next section.

3. Extraction of the threshold voltage

3.1. Previous methods

One of the most important parameters to model the operation of a MOSFET is the threshold voltage, V_T . There are several definitions of threshold voltage [2, 4, 21] and many methods have been developed to extract this parameter. The majority of procedures used to determine V_T are based in the strong inversion operation characteristics. The most common methods are [18]: a) defining V_T as the gate voltage corresponding to a certain predefined practical constant drain current [17]; b) finding the gate voltage axis intercept of the linear extrapolation of the $I_D - V_{GS}$ characteristics at its maximum first derivative (slope) point [4]; c) determining V_T at the maximum of the second derivative of I_D with respect to V_{GS} [22]; d) finding the gate voltage axis intercept of the ratio of the conductance to the square root of the transconductance, which requires two derivatives of the data [23].

The procedures for extracting V_T by the linear and second-derivative extrapolation methods are illustrated in Figs. 2a and 2b, respectively.

In this figure, the measured data are from an n-MOSFET with mask channel length of 0.6 μm, oxide thickness of 14 nm and channel doping of 10^{17} cm^{-3}. For the linear extrapolation method V_T is determined by extrapolating at the point of maximum slope on the $I_D - V_{GS}$ characteristics. On the other hand, the second-derivative extrapolation method determines V_T at the point where the second derivative of $I_D - V_{GS}$ is maximum.

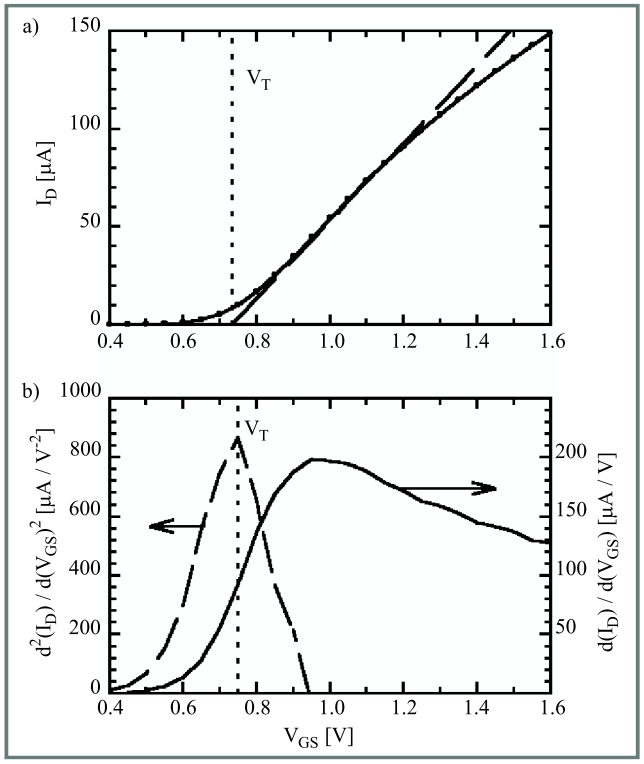

Fig. 2. Illustration of the linear extrapolation (a) and second derivative (b) methods to extract V_T.

Other methods have been proposed. One uses the subthreshold operation characteristics to determine V_T from the gate voltage necessary to make the surface potential equal to twice the bulk potential [24]. Recently a new procedure was presented to extract the threshold voltage independently of the presence of source and drain parasitic resistances [25].

Contrasting with previous methods where the extraction algorithm is generally restricted to the strong inversion characteristics, or perhaps to the subthreshold characteristics, a recent method [26, 27] that uses the transition from subthreshold to strong inversion operation to determine the threshold voltage was presented. This transition method does not utilize any differentiation of the data, rather it makes use of integration which greatly reduces the effect of possible random noise or measurement error in the experimental data.

3.2. Transition's method

The drain current in the subthreshold region, can be modeled by an exponential expression of the form [1–11]

$$I_D = I_{S0} \exp\left[\beta\left(V_{GS} - V_T\right)/n\right], \tag{19}$$

where V_{GS} is the intrinsic gate-to-source voltage, and n is a quality factor known as the subthreshold slope. I_{S0} is a coefficient that depends on the gate capacitance per unit area, the effective size, the effective mobility of the channel, the thermal voltage, and the intrinsic drain-to-source voltage [6, 18].

In contrast, in strong inversion, the drain current can be modeled for small V_{DS} by a linear expression of the form [1–11]

$$I_D \approx K\left(V_{GS} - V_T\right)V_{DS}, \tag{20}$$

where K depends on the gate capacitance per unit area, the effective size and the effective mobility of the channel. In the transition region neither Eqs. (19) nor (20) are valid and the $I_D - V_{GS}$ characteristics change from exponential to linear behavior, or correspondingly, the $\ln I_D - V_{GS}$ characteristics change from linear to logarithmic behavior, as depicted in Fig. 3 for a 10 μm long *n*-channel MOSFET

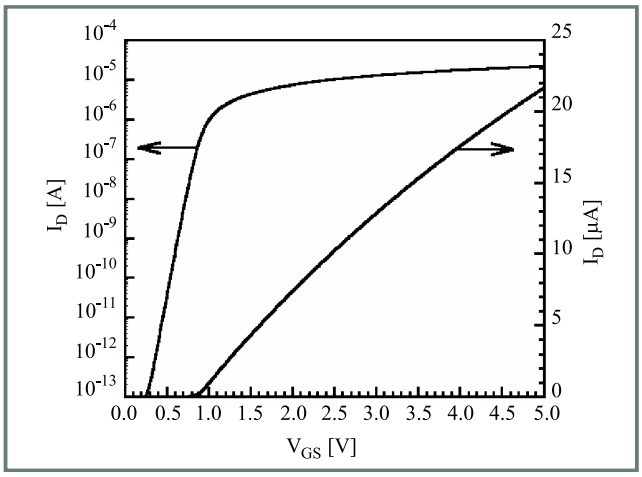

Fig. 3. Drain current as a function of gate voltage for BSIM3v3.2 modeled variable mobility long n-channel MOSFET, at $V_{BS} = 0$, $V_{DS} = 50$ mV.

simulated using the AIM-SPICE [6] Level 17 BSIM3v3.2 model [5]. This transition from linear to logarithmic behavior is analogous to the I-V characteristic of a diode with a parasitic series resistance. To eliminate the effects of the series resistance in a diode, an integral function was proposed [28, 29].

As previously stated, the threshold voltage is the value of gate voltage at which the $I_D - V_{GS}$ characteristics change from exponential to linear behavior. In order to find this transition point and thus extract the threshold voltage we will use an auxiliary function that has already proved its usefulness in getting rid of parasitic resistances when extracting the model parameters of diodes [28, 29].

First, the drain current of the MOSFET is measured versus gate voltage from below to well above threshold with zero body bias and a small constant value of drain voltage. Second, the following function is numerically calculated from

the measured data:

$$G(V_{GS}, I_D) = V_{GS} - 2\frac{\int_{V_{GSb}}^{V_{GSa}} I_D(V_{GS})\, dV_{GS}}{I_D}, \qquad (21)$$

where V_{GSb} and V_{GSa} are the lower and upper limits of integration corresponding to gate-to-source voltages below and above threshold, respectively.

Third, when $G(V_{GS}, I_D)$ is plotted as a function of $\ln I_D$ it becomes a linear function wherever $I_D(V_{GS})$ is exponential, and additionally it has the property of vanishing wherever $I_D(V_{GS})$ is linear [28, 29]. Therefore, a plot of G versus $\ln I_D$ should be a straight line below threshold, where the current is dominated by diffusion and consequently it is predominantly exponential. Furthermore, G should drop abruptly to zero as soon as the threshold voltage is surpassed, since above this point the current is dominated by drift and hence it is predominantly lineal.

Figure 4 presents a plot of such a behavior of G, which was numerically calculated using Eq. (21) and the data in

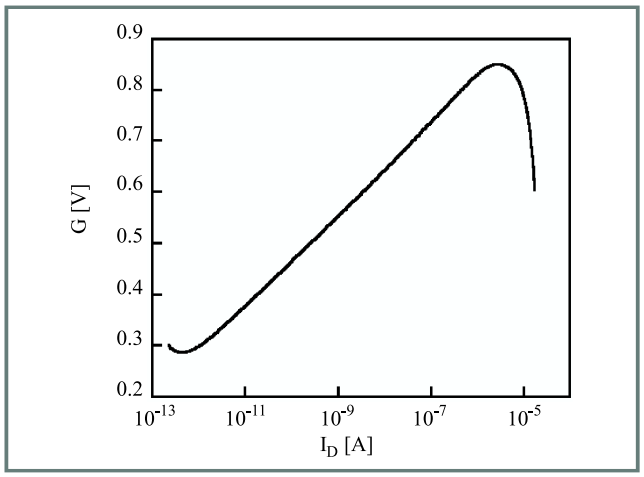

Fig. 4. Function G calculated by applying Eq. (21) to the modeled $I_D - V_{GS}$ characteristics of the previous figure. The maximum G represents the value of $V_T = 0.850$ V.

Fig. 3. As expected, the curve is seen to behave approximately as a straight line until it reaches a maximum value of about 0.850 V, at which point it falls rapidly towards zero indicating that the current has become predominantly lineal. This maximum value of G corresponds to the threshold voltage of the device and compares well to the value of $V_T = 0.855$ V which was separately extracted for this device using the conventional second-derivative method.

4. The effective channel length

The so-called channel length is a broad description of three different channel lengths. One is the mask channel length L_m, which denotes the physical length of the gate mask. Another is the electrical effective channel length L_{eff}, which defines the length of a region near the Si-SiO_2 interface in which the inversion free-carrier density is controlled by the gate voltage. This channel length is given by

$$L_{eff} = L_m - \Delta L_{eff}, \qquad (22)$$

where ΔL_{eff} is the effective channel length reduction illustrated in Fig. 5. The third channel length used frequently is

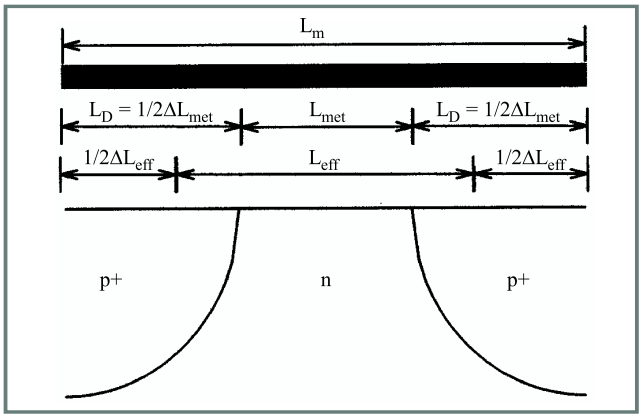

Fig. 5. Device structure of a p-channel MOSFET showing the definitions of L_{eff}, L_{met} and L_m.

the metallurgical channel length L_{met}, which is the distance between the source and drain metallurgical junctions at the Si-SiO_2 interface:

$$L_{met} = L_m - \Delta L_{met}, \qquad (23)$$

where $\Delta L_{met} = 2L_D$, and L_D is the length of the lateral diffusion of the source or drain region (see Fig. 5).

The precise determination of the effective channel length is not straightforward due mainly to the uncertainty as to whether the portion of the drain and source regions underneath the gate should be considered as part of L_{eff} (i.e., $L_{eff} > L_{met}$) or as part of the drain and source series resistance and thus not part of L_{eff} (i.e., $L_{eff} = L_{met}$). Recent studies have concluded [30, 31] that the theory of $L_{eff} > L_{met}$ is more appropriate because the free-carrier density in the drain and source regions underneath the gate is influenced by the gate voltage.

Since ΔL_{eff}, and thus L_{eff}, cannot be measured directly, various methods have been developed in the literature to extract them from the current-voltage characteristics [32–37], capacitance-voltage characteristics [38–44], or physical insight provided by numerical simulation [30, 45]. The main disadvantage of the methods based on current-voltage characteristics, called the I-V methods, is that they are often obscured by the presence of the parasitic drain and source series resistance. On the other hand, the main disadvantage of the capacitance-voltage (C-V) methods, is that equipment with high resolution is required to measure the small capacitances in the MOSFET (in the order of fento farads). Methods based on device physical insight require results simulated from device simulators, the accuracy of which depends on the proper selection of model parameters.

In the following sections, the development of the different extraction methods will be discussed.

4.1. Current-voltage methods

4.1.1. Terada-Muta or Chern et al. method

The method by Terada-Muta [33] or Chern et al. [34] was derived based on the following simple current-voltage relationship for the drain current in the linear region:

$$I_D = \frac{W}{L_{eff}} \mu C_o \left(V_{GS} - V_T\right) V_{DS} \,, \tag{24}$$

where W is the channel width, C_o is the oxide capacitance per unit area, μ is the effective free-carrier mobility, V_T is the threshold voltage, and V_{GS} and V_{DS} are the intrinsic gate-source and drain-source voltages, respectively. The intrinsic voltages can be related to the external gate-source and drain-source voltages (V_g and V_d):

$$V_{GS} = V_g - I_D R_S \tag{25}$$

and

$$V_{DS} = V_d - I_D \left(R_S + R_D\right) . \tag{26}$$

Here R_D and R_S are the drain and source parasitic series resistances illustrated in Fig. 6.

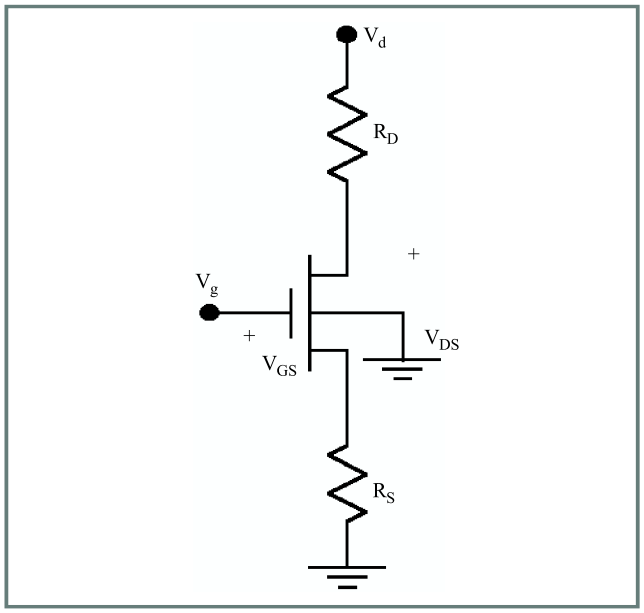

Fig. 6. MOSFET equivalent circuit including the source and drain series resistances (R_S and R_D) and having the body and source terminals grounded.

Combining Eqs. (24) and (26), the total channel resistance, R_m, can be expressed by

$$R_m \equiv \frac{V_d}{I_D} = R_{DS} + \frac{\left(L_m - \Delta L_{eff}\right)}{\mu C_o W \left(V_{GS} - V_T\right)} \,, \tag{27}$$

where $R_{DS} \equiv (R_D + R_S)$ is the total drain and source resistance. For the linear region under study, $(V_g - V_T)$ is much larger than $I_D R_{DS}$, and $V_g \approx V_{GS}$. This results in

$$R_m = R_{DS} + \frac{\left(L_m - \Delta L_{eff}\right)}{\mu C_o W \left(V_g - V_T\right)} \,. \tag{28}$$

Then, according to Eq. (28), the plot of R_m versus L_m is a straight line for a given $(V_g - V_T)$, and the unique intersection of all the straight lines for different $(V_g - V_T)$ yields ΔL_{eff} on the L_m axis (i.e., x axis) and R_{DS} on the R_m axis (i.e., y axis). It is important to point out that the threshold voltage is a function of L_m.

Although widely used, the Terada-Muta method has been found to fail at nitrogen liquid temperature [36, 46] because it yields no unique intersection of the straight lines as illustrated in Fig. 7. In this figure we present R_m versus L_m plots of p-channel devices at temperatures of 300 K and 77 K, respectively. At 300 K, the unique intersection of the straight lines yields $\Delta L_{eff} \approx 0.3\,\mu$m on the x axis and $R_{DS} \approx 60\,\Omega$ on the y axis. On the other hand, the analogous procedure at 77 K yields no unique intersection of the straight lines, and even if the intersection of three of lines is used, a negative ΔL_{eff} is obtained, which is physically unsound for the conventional MOSFET under consideration.

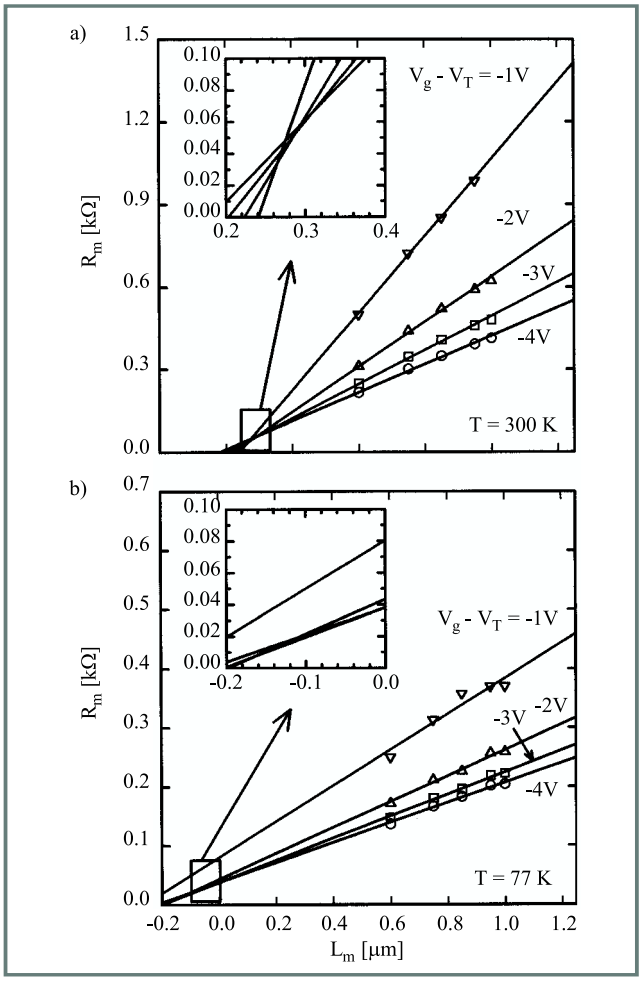

Fig. 7. The total channel resistance versus mask channel length for various gate voltages at (a) 300 K and (b) 77 K. The symbols are the measured data and the lines are the fittings to data using straight lines.

The Terada method may also fail [47] at room temperature for MOSFETs having a relatively high doping concentration

in the substrate. The failure of the Terada method can be attributed to the following assumptions used in developing the method: 1) the drain and source series resistances are independent of the gate bias; 2) V_T used in the method, and thus L_{eff} extracted, does not account for the effects of the series resistances; 3) $V_g \approx V_{GS}$; and 4) the free-carrier velocity saturation effect in the channel is negligible.
Recently, Terada and co-workers presented an improved extraction method [48], which proposed that ΔL_{eff} and R_{DS} extracted using their original method can be a function of the gate voltage due to the fact that the R_m versus L_m plot possesses several intersections of the straight lines. From these different intersections, a statistical approach is then used in their new method to determine the correct and unique ΔL_{eff} and R_{DS} based on the concept that the most accurate ΔL_{eff} and R_{DS} give rise to the least dependence of these two parameters on the gate bias.

4.1.2. Shift and ratio method

The shift and ratio (S & R) method, developed by Taur et al. [32], is based on the total channel resistance, which was given in Eq. (28) and can be rewritten as

$$R_m = R_{DS} + \left(L_m - \Delta L_{eff}\right) f\left(V_g - V_T\right) , \qquad (29)$$

where $f(V_g - V_T)$ is a general function describing the MOSFET behavior. The S & R method extracts ΔL_{eff} using at least two devices (i.e., ith and jth devices) having different mask channel lengths (i.e., L_{mi} and L_{mj}, one of which needs to be long), and the following functions S_i and S_j:

$$S_i \equiv \frac{dR_{mi}}{dV_g} \approx \left(L_{mi} - \Delta L_{eff}\right) \frac{df\left(V_g - V_{Ti}\right)}{dV_g} \qquad (30)$$

and

$$S_j \equiv \frac{dR_{mj}}{dV_g} \approx \left(L_{mj} - \Delta L_{eff}\right) \frac{df\left(V_g - V_{Tj}\right)}{dV_g} , \qquad (31)$$

where the assumption that R_{DS} and ΔL_{eff} are independent of V_g has been used. According to these equations, curves of S_i and S_j versus V_g can be constructed. To extract ΔL_{eff}, the S_i curve is first translated („shift") horizontally in the V_g axis with respect to the S_j curve by the amount

$$\Delta V_{ij} \equiv \left(V_{Ti} - V_{Tj}\right) , \qquad (32)$$

because the threshold voltage is a function of the channel length. Also, the S_i curve is magnified („ratio") in the S axis, with respect to the curve S_j, by a factor

$$r_{ij} \equiv \frac{L_{mi} - \Delta L_{eff}}{L_{mj} - \Delta L_{eff}} = \frac{S_i\left(V_g - \Delta V_{ij}\right)}{S_j\left(V_g\right)} . \qquad (33)$$

The key here is to find the ΔV_{ij} value for which r_{ij} is a constant. Taur et al. [32] solved ΔV_{ij} and r_{ij} using a statistical approach. Once the values of V_{ij} and r_{ij} are found, L_{eff} can be calculated from Eq. (33).

We have applied this method to n-channel MOSFETs with a channel width of 20 μm and mask channel lengths of 1.75, 2.00 and 20 μm. An increment of 100 mV for the gate voltage and drain voltage of 100 mV were used in the measurements. Figure 8 shows the S function versus V_g characteristics.

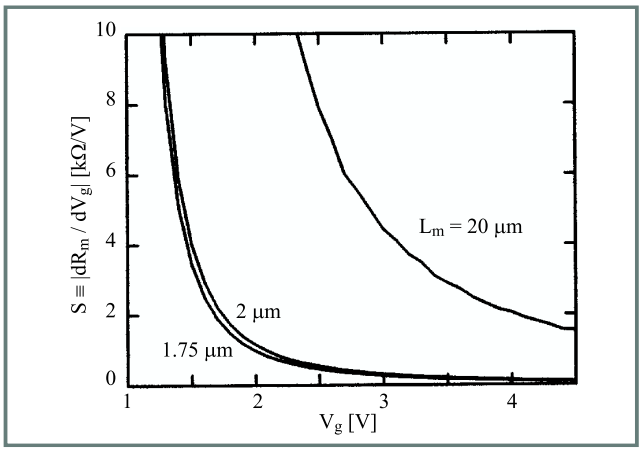

Fig. 8. The function S versus the gate voltage for MOSFETs with three different mask channel lengths.

The problem of a translation and a magnification in the original S & R method can be changed [18] to a more straightforward dual-translation problem by using two new functions:

$$T_i \equiv \ln\left(|S_i|\right) , \quad T_j \equiv \ln\left(|S_j|\right) . \qquad (34)$$

Figure 9a shows the T function versus V_g characteristics obtained from the experimental data.
Then, using the plots for $L_m = 2$ and 20 μm and different values of $\square V_{ij}$, we calculated the corresponding ΔT_{ij} by shifting the plot and carrying out a numerical fit for the range 2 V $< V_g <$ 5 V. The range $V_g <$ 2 V was not included in order to avoid moderate and weak inversion. Figure 9b presents ΔT_{ij} and the corresponding error versus $\square V_{ij}$ using the 2- and 20- μm MOSFETs. Since the error is minimal at about $\square V_{ij} = 0.07$ V, the solution is $\Delta T_{ij} = 2.58$, and we obtained $L_{eff} = 0.53$ μm.
While it is possible to eliminate the translation in the T axis by differentiating T_i with respect to V_g, it is better not to do so because such a mathematical manipulation would increase the effect of the noise on the experimental data.
We conclude that the S & R method is more complex in extracting L_{eff} than the Terada method. In addition, such a method may not be accurate in some cases due to the use of following assumptions: 1) the series resistances are assumed independent of the gate bias; 2) $V_g \approx V_{GS}$; and 3) the effect of drift velocity saturation along the channel is assumed negligible.

4.1.3. Conductance method

This method [36] accounts for the carrier drift velocity saturation effects [4–6] and has been used to extract the parameters at both room and liquid nitrogen temperatures.

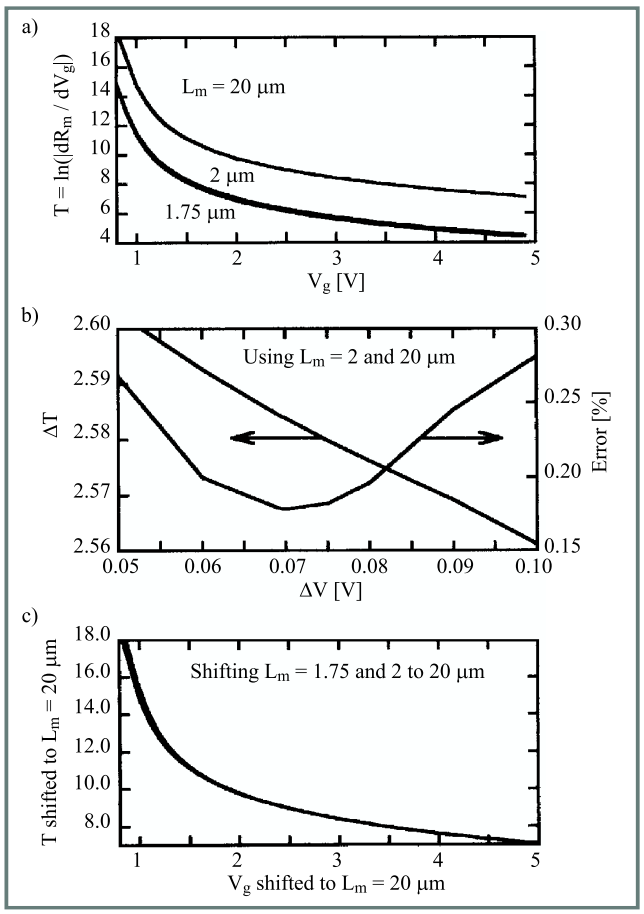

Fig. 9. (a) The function T versus the gate voltage for MOSFETs with three different mask channel lengths. (b) Shift in T versus the shift in gate bias and the corresponding error. (c) The plots for $L_m = 1.75$ and 2 μm shifted to the plot for L_m = 20 μm.

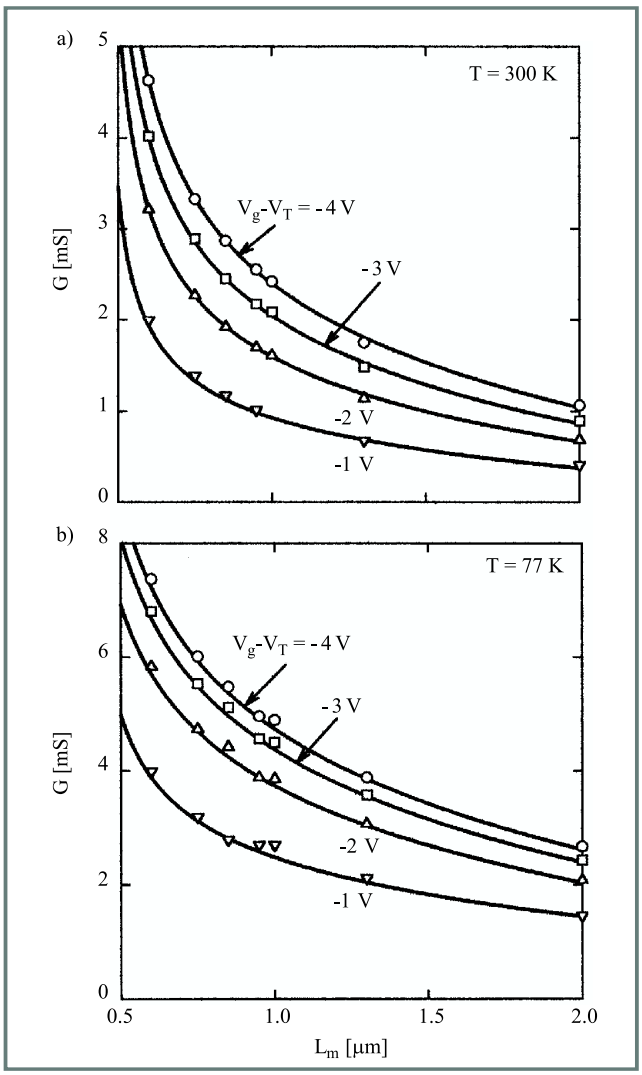

Fig. 10. Total channel conductance versus mask channel length for various gate voltages at (a) 300 K and (b) 77 K. The symbols are the measured data and the lines are the fittings to data using the conductance method.

Following the model proposed by Shur et al. [6, 49] and using the strong inversion condition and the approximation $V_g \approx V_{GS}$, the drain current can be expressed as

$$I_D = \frac{W\mu_{lf}C_o(V_g - V_T)V_{DS}}{L_{eff}\left(1+\dfrac{V_{DS}}{V_{SATE}}\right)}\,, \tag{35}$$

where μ_{lf} is the effective free-carrier mobility for low field and V_{SATE} is an effective voltage which accounts for the carrier velocity saturation effect. After some algebraic manipulations and approximations [36], the conductance is obtained

$$G = \frac{1}{2R_{DS}} + C_l L_{eff}^{1/3} + C_2 L_{eff}^{-2/3}\,, \tag{36}$$

where C_1 and C_2 are two constants governed by the following relationship:

$$\frac{C_2}{C_1} \approx -G_o R_{DS} L_{mo}\,, \tag{37}$$

where L_{mo} is the mean mask channel length of all the MOSFETs considered, and G_o is the mean conductance of these devices. Equation (36) allows one to determine R_{DS} and L_{eff} from the data of G as a function of V_g and L_m.

Figures 10a and 10b show the conductance versus mask channel length obtained from measurements (symbols) and from fitted model calculations (lines) for various gate voltages at 300 K and 77 K, respectively.

The extracted values of the total series resistance (i.e., drain and source series resistances) at 300 and 77 K are illustrated in Fig. 11. It is shown that R_{DS} decreases with increasing gate voltage (i.e., from 100 Ω to 80 Ω at 77 K, and from 270 Ω to 180 Ω at 300 K).

The extracted values of the effective channel length reduction, $\Delta\square L_{eff} = L_m - L_{eff}$, for the two temperatures are shown in Fig. 12. The results suggest that ΔL_{eff} depends weakly on V_g but strongly on temperature.

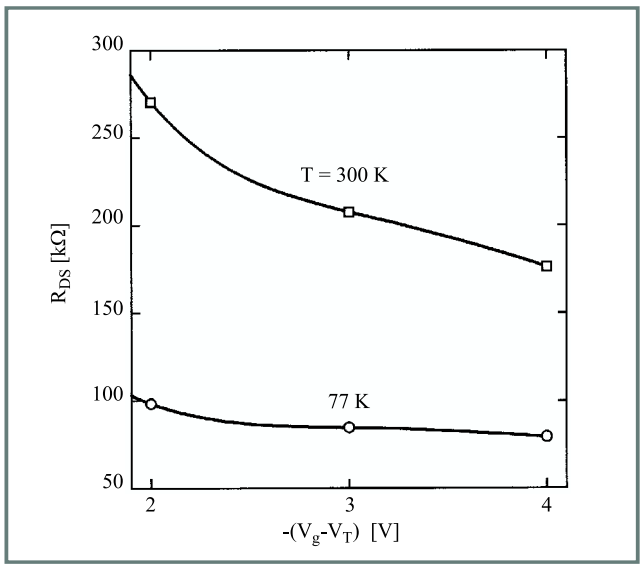

Fig. 11. Extracted values of the total drain and source series resistance versus gate voltages for two temperatures.

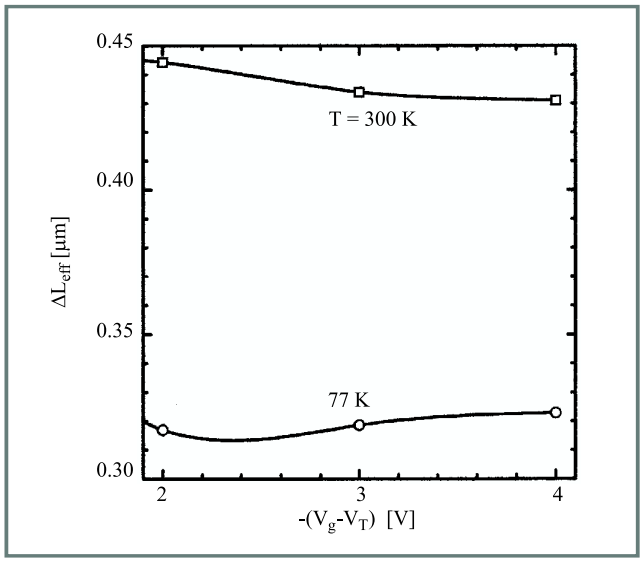

Fig. 12. Extracted values of the difference between the mask channel length and the effective channel length (i.e., $\Delta\Box L_{eff} = L_m - L_{eff}$) for two different temperatures.

4.1.4. Fikry et al. method

The method by Fikry et al. [50] also accounts for the carrier velocity saturation effect in the channel and uses the assumption of $V_g \approx V_{GS}$. The velocity saturation effect is imbedded in the following free-carrier mobility model:

$$\mu = \frac{\mu_o}{\left(1+\Theta\left(V_g - V_T\right)\right)\left(1+\dfrac{\mu_o V_d}{L_{eff}\nu_{sat}}\right)}, \qquad (38)$$

where μ_o is the low-field mobility, Θ is the mobility degradation factor due to the vertical field, and ν_{sat} is the saturation velocity of the carriers.

The following function is then used:

$$\frac{I_D}{g_m^{1/2}} = s^{-1/2}\left(V_g - V_T\right), \qquad (39)$$

where g_m is the transconductance and

$$s = \frac{L_m - \left(\Delta L_{eff} - \dfrac{\mu_o V_d}{\nu_{sat}}\right)}{W\,\mu_o C_o V_d}. \qquad (40)$$

The above two equations were derived by combining Eqs. (24), (26) and $V_g \approx V_{GS}$. The values of V_T and s are extracted by plotting $I_D/g_m^{1/2}$ versus V_g. Then, the plot of s versus L_m allows one to obtain μ_o from its slope and $\left(\Delta L_{eff} - \mu_o V_d/\nu_{sat}\right)$ from its intercept to the L_m axis. Thus, ΔL_{eff} can be determined from $\left(\Delta L_{eff} - \mu_o V_d/\nu_{sat}\right)$, provided the value of ν_{sat} is calculated from the following equation describing transconductance of the device biased in the saturation region:

$$g_m = W C_o \nu_{sat}. \qquad (41)$$

Alternatively, ΔL_{eff} can also be obtained from the extrapolation of $\left(\Delta L_{eff} - \mu_o V_d / \nu_{sat}\right)$ versus V_d plot, which is a straight line, to the y axis where V_d is zero. Simulations indicate [18] that this method is sensitive to the bias condition and that a small voltage should be used to make sure the MOSFET operated in the linear region.

Figure 13a shows the MEDICI simulation results of $I_D / g_m^{1/2}$ versus V_g for several mask channel lengths and $V_d = -50$ mV. The linear extrapolation of the curves to the V_g axis gives V_T. The corresponding plot of s versus L_m, illustrated in Fig. 13b, yields $W\mu_o C_o V_d = 0.99 \cdot 10^{-6}$ μm/Ω from its slope and $\left(\Box L_{eff} - \mu_o V_d / \nu_{sat}\right) = -0.0134$ μm from its intercept to the L_m axis. Then, using $C_o = 3.45 \cdot 10^{-7}$ F/cm^2, $|V_d| = 0.05$ V, $W = 1$ μm and $\nu_{satn} = \nu_{satp} = 10^6$ cm/s, we obtain $\mu_o = 57$ cm^2/V.s and $\Delta\Box L_{eff} = 0.015$ μm from the Fikry method.

If a larger bias condition of $V_d = -100$ mV is used in simulation, then $W\mu_o C_o V_d = 1.94 \cdot 10^{-6}$ μm/Ω, $\left(\Box L_{eff} - \mu_o V_d / \nu_{sat}\right) = -0.053$ μm, $\mu_o = 56$ cm^2/V.s and $\Delta\Box L_{eff} = 0.042$ μm. The fact that different V_d gives rise to different $\Delta\Box L_{eff}$ suggests that the method is sensitive to the bias condition and that a small voltage should be used to make sure the MOSFET operated in the linear region.

An alternative way to extract $\Delta\Box L_{eff}$ is extrapolating the $\left(\Box L_{eff} - \mu_o V_d / \nu_{sat}\right)$ versus V_d plot to the point of $V_d = 0$ (i.e., y axis), as illustrated in Fig. 14, which gives $\Delta\Box L_{eff} = 0.026$ μm.

4.1.5. Nonlinear optimization method

The nonlinear optimization method [51, 52] extracts ΔL_{eff} based on optimization techniques applied to current-voltage characteristics. This optimization technique, which are frequently implemented using statistical program like Splus [53], present two main advantages: (1) the consistent determination of all the parameters of the model because

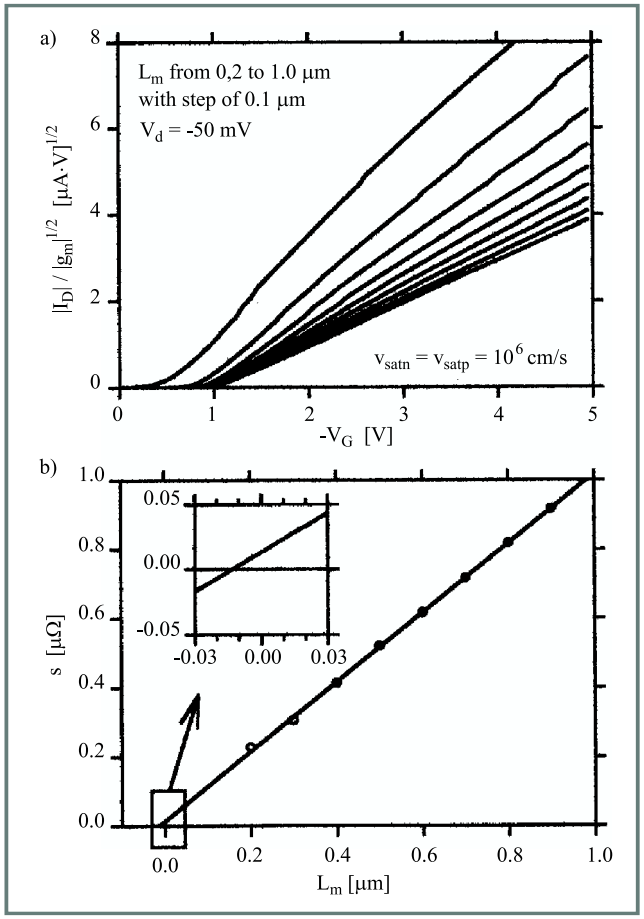

Fig. 13. (a) Calculated values of $I_D / g_m^{1/2}$ versus V_g for several mask channel length and $V_d = -50$ mV. The slopes of these approximate straight lines give the values of s. (b) Calculated values of s versus L_m. The slope of this approximate straight line yields $W\mu_o C_o^a V_d = 0.99 \cdot 10^{-6}\ \mu\text{m}/\Omega$ and the intercept of the line at the L_m axis gives $\left(\square L_{eff} - \mu_o V_d / v_{sat}\right) = -0.0134\ \mu\text{m}$.

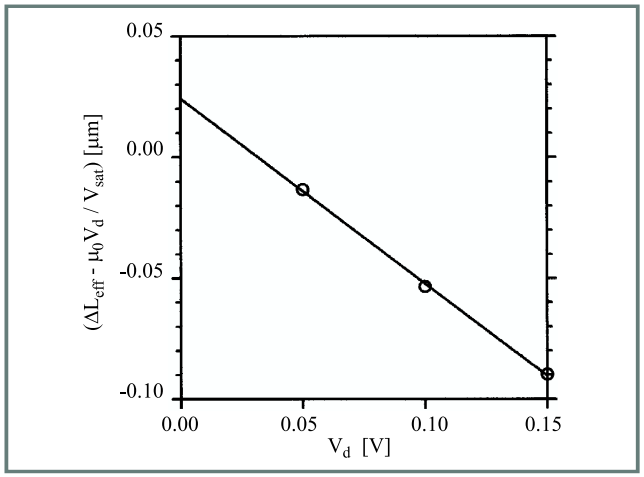

Fig. 14. Extracted values of $\left(\square L_{eff} - \mu_o V_d / v_{sat}\right)$ (open circles) for three different V_d. The intercept of the straight line passing through these points at the vertical axis (i.e., $V_d = 0$) yields $\square L_{eff} = 0.026\ \mu\text{m}$.

of the simultaneous extraction; and (2) the reduction of the effects of the noise on the experimental data due to the optimization techniques. There are two main disadvantages, however: (1) nonphysical parameters values can be obtained because of the pure fitting scheme, and (2) the requirement of a long computational process.

4.2. Capacitance-voltage method

To avoid the effect of the parasitic drain and source series resistances, which is a main mechanism causing the difficulty in the I-V methods, various methods have been developed to extract ΔL_{eff} from the capacitance-voltage characteristics (i.e., C-V methods) [39–44]. The main drawback of the C-V methods is the requirement of high resolution equipment to measure the small capacitances in MOSFETs. Moreover, it is somewhat difficult to correlate the C-V data and L_{eff}.

Among the various C-V extraction methods we find: 1) Sheu's method [40], which is based on the crude assumption that the capacitance between the inverted channel and the substrate is negligible [6]; 2) Vitanov's method [41], which is based on the wrong assumption that the capacitances for the source-body and drain-body junction regions can be neglected; 3) Lee's method [42], which uses various devices (i.e., various L_m) and the determination of the capacitance at which the C-V curves for different L_m start to deviate from each other; 4) Guo's method [43], which is similar to Leet's method; and 5) Latif's method [44] which accounts for capacitances that the Sheu-Ko's method neglected.

4.3. Simulation-based method

4.3.1. Narayanan et al. method

Narayanan et al. [30] estimated the value of ΔL_{eff} through the means of physical insight obtained from device simulation. We show in Fig. 15 the hole concentration at the interface for various V_g for a p-channel device. Based on the concept that the effective channel is the region in which the free-carrier concentration is controlled by the gate voltage. It was then suggested that the two points where the hole concentrations for different V_g start to deviate from each other (indicated by arrows in Fig. 15) are the edges of the effective channel. Such a definition is more accurate because it accounts for the transition regions between the deep channel and source/drain regions and because it is not affected by the gate voltage.

4.3.2. Niu et al. method

Niu et al. [45] also proposed a method to determine L_{eff} through the means of physical insight obtained from simulations. While Niu et al. agreed with the physical reasoning of Narayanan's method [30], they felt that it is somewhat subjective and arbitrary to determine the effective channel based on the two points where the free-carrier concentrations for different V_g start to deviate from each other.

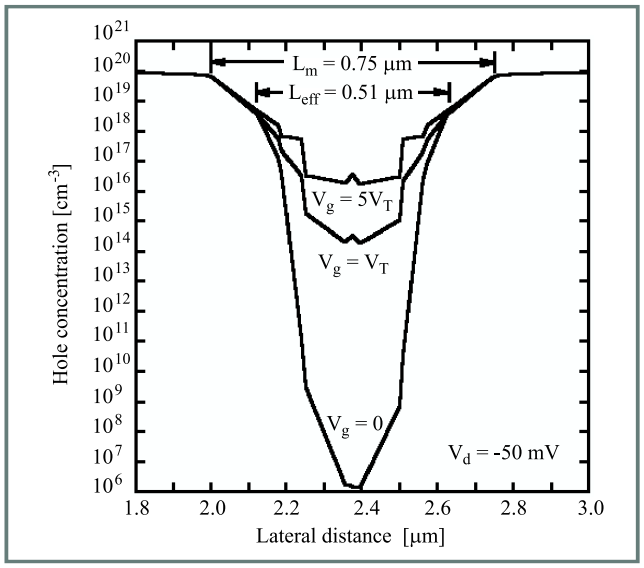

Fig. 15. Hole concentration at the interface of the p-channel MOSFET with $L_m = 0.75\ \mu m$.

Niu's method is based on the assumption that the diffusion current is negligible for a MOSFET biased in strong-inversion. Therefore, the following behavior should be found along the effective channel: 1) the inversion carrier concentration is nearly constant; 2) the lateral electric field (i.e., $-d\Psi/dx$) is also nearly constant to keep a constant drift current; 3) the electrostatic potential Ψ varies linearly with respect to the lateral distance x; and 4) the second derivative of the electrostatic potential with respect to x should be zero (i.e., $d^2\Psi/dx^2 = 0$). Then, Niu proposed that the edges of the effective channel should be defined at the points where $d^2\Psi/dx^2$ are maximum.

Figure 16a shows the doping profile along the channel at the interface, and the inversion free-carrier density simulated for different gate voltages are illustrated in Fig. 16b. Based on the Narayanan's method, L_{eff} is found to be about 1.2 μm, and the determination of the boundaries of the effective channel is somewhat subjective because the precise points where the curves start to deviate from each other are not very clear.

Figures 17(a)–(c) show Ψ, $d\Psi/dx$ and $d^2\Psi/dx^2$, respectively, at the interface along the channel for $V_g = -3$ V and $V_d = -0.05$ V. We see in Fig. 17a that Ψ varies approximately linearly with respect to x along the effective channel, but there are two different slopes because of the presence of the LDD regions. Four positive peaks and two negative peaks for $d^2\Psi/dx^2$ are shown in Fig. 17c.

Using the two closest positive peaks to define the effective channel, one will obtain a value of 0.9 μm. This value is incorrect because it is smaller than $L_{met} = 0.93\ \mu m$. A more

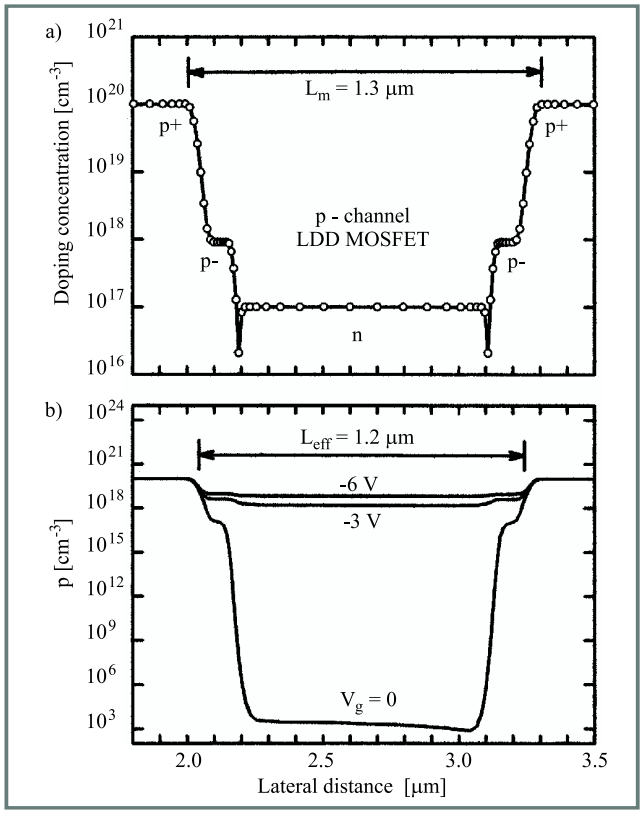

Fig. 16. (a) Impurity doping concentration at the Si-SiO_2 interface along the channel of the simulated LDD MOSFET with $L_m = 1.3\ \mu m$. (b) Hole concentration at the interface of the MOSFET for various gate biases.

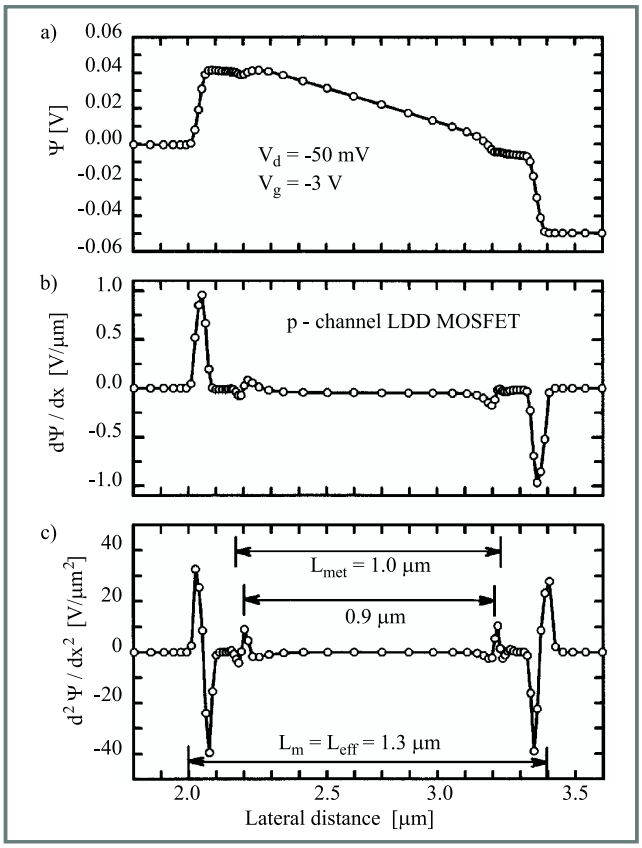

Fig. 17. (a) Electrostatic potential Ψ, (b) first derivative of the electrostatic potential with respect to x (i.e., $d\Psi/dx$), and (c) second derivative of the electrostatic potential with respect to x (i.e., $d^2\Psi/dx^2$) at the interface of the MOSFET with $L_m = 1.3\ \mu m$.

reasonable value of $L_{eff} = 1.3\,\mu m$ is obtained by using the two farthest positive peaks.

4.4. Comparison of various extraction methods

The Terada-Muta I-V method yielded a value for the effective channel length consistent with that determined from the simulation-based method [30] based on the physics that L_{eff} is the length of a channel region in which the inversion free-carrier density is controlled by the gate voltage. The same effective channel length has also been extracted from the S & R I-V method. In contrast, the C-V methods yield an effective channel length close to L_{met}.

5. Extraction of drain and source series resistance

The extraction of the individual values of the source and drain series resistances require either the knowledge of their sum $(R_D + R_S)$ and difference $(R_D - R_S)$, or the ability to extract the two parameters separately. In this section, we will deal mainly with the extraction of $(R_D - R_S)$.

The most widely method to extract the total drain and source series resistance $(R_D + R_S)$ was presented independently by Terada and Muta [33] and by Chern et al. [34] almost twenty years ago. Several other methods [52, 54–59] have been developed recently.

It is a common practice to assume that the parasitic resistances associated with the drain and source regions of MOSFETs are approximately equal to each other, $R_D \approx R_S$. Therefore, knowing $(R_D + R_S)$, we obtain $R_S \approx R_D \approx (R_S + R_D)/2$. However, this assumption becomes invalid when the drain and source regions of the device are not totally symmetrical. Such an asymmetry results in a difference in the drain and source resistances $(R_D - R_S)$ and can affect considerably the current-voltage characteristics of MOSFETs.

The difference in the drain and source resistances arises mainly from processing, layout, and/or electrical stressing, and it becomes more prominent in the case of deep-submicron devices. This is because the relative importance of the parasitic resistances over the intrinsic components is increased as the geometry of the device shrinks. Previous numerical simulations [57, 60] indicate that the drain and source resistance asymmetry is originated mainly from the difference in the drain and source contact resistances, and not from the gate misalignment, nor from the difference in source and drain doping densities.

An approach frequently used for extracting $(R_D - R_S)$ consist on performing measurements of an MOS device, first connected in the „normal configuration" in which the source and body are grounded, and then measuring it again in the „inverted configuration" in which the source and drain terminals are interchanged, as shown in Figs. 18a and 18b, respectively. It is important to point out that the intrinsic and extrinsic body voltage are related by

$$V_{BS} = V_{bs} - I_d R_S \,. \tag{42}$$

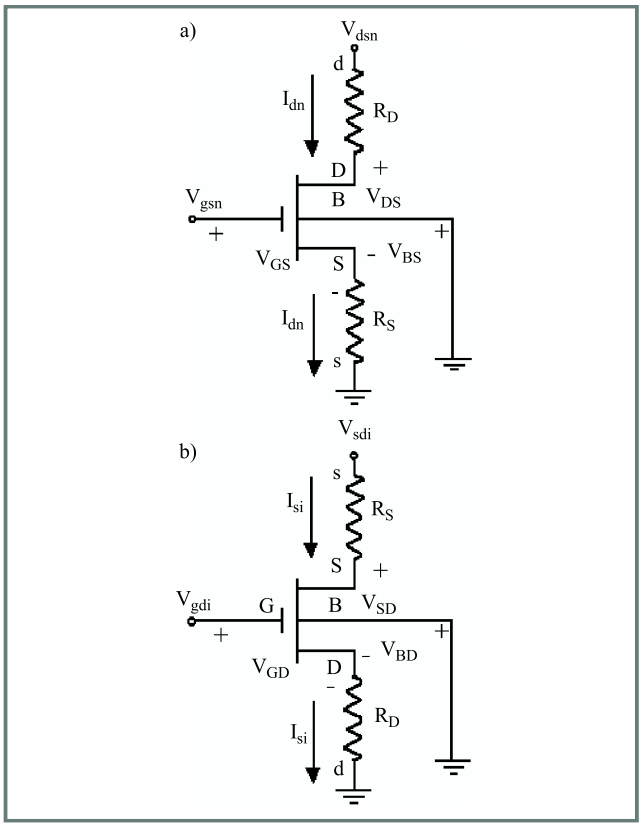

Fig. 18. (a) MOSFET in normal mode of operation with the source and body grounded, and (b) MOSFET in inverse configuration with the drain and body grounded.

Two extraction methods, namely the reciprocal transconductance method and gate-voltage shift method, have been developed based on this approach and are presented below.

5.1. Reciprocal transconductance method

The difference between the drain and source resistances, $(R_D - R_S)$, can be extracted from the extrinsic gate transconductance of a single MOSFET measured under saturation operation at the same drain to source voltage but two different configurations. First, the extrinsic gate transconductance g_{mn} for the normal mode of configuration is measured from the I_{dn} versus V_{gsn} characteristics in the saturation region (i.e., the subscript n represents the normal mode of configuration in which the source and body are grounded (Fig. 18a). This transconductance is given by

$$g_{mn} = \frac{\partial I_{dn}}{\partial V_{gsn}} \,. \tag{43}$$

Second, the gate transconductance g_{mi} for the inverse mode of configuration is measured from the I_{si} vs. V_{gdi} characteristics in the saturation region, (i.e., where subscript i

represents the inverse mode of configuration in which the source and drain functions are interchanged (Fig. 18b). Analogous to Eq. (43), such a transconductance is

$$g_{mi} = \frac{\partial I_{si}}{\partial V_{gdi}} . \tag{44}$$

It should be noted that the intrinsic variables are the same for both modes of configuration, and only R_S and R_D asymmetry is present in the device. After some algebraic manipulations [18, 20, 60–65] we obtain:

$$\left(R_D - R_S\right) = \frac{\dfrac{1}{g_{mi}} - \dfrac{1}{g_{mn}}}{1 + \dfrac{g_{b0}}{g_{m0}}} , \tag{45}$$

where g_{b0} and g_{m0} are the intrinsic body and gate transconductance in the normal mode.

We stress that the body effect has been included in the denominator of Eq. (45) by retaining the intrinsic body transconductance.

We conclude from Eq. (45) that, in addition to measuring the normal and inverse extrinsic gate transconductances in saturation, it is necessary to know the ratio of the intrinsic body transconductance to the intrinsic gate transconductance (i.e., g_{b0}/g_{m0} term in the denominator of Eq. (45)) before $(R_D - R_S)$ can be determined. Three different procedures [18, 20, 61–66] to calculate this term have been developed based on adding external resistances and measuring gate transconductances.

5.2. Gate-voltage shift method

This method is also based on measuring a single transistor when it is connected alternatively in the normal and inverse configurations [20, 64, 65]. The difference is that, instead of measuring the difference between normal and inverse reciprocal gate transconductances, it is based on measuring the shift of the gate voltage needed to maintain the same magnitude of drain current when the device is connected in the inverse and normal configurations. Consider a MOSFET in the normal configuration, with the source and body grounded, and also in the inverse configuration, with the drain and source interchanged. The drain current in the normal configuration, can be expressed as a general function of the intrinsic voltages as

$$I_{dn} = f\left[\left(V_{GS} - V_{Tn}\right), V_{DS}\right] , \tag{46}$$

where f is a function defined by a particular MOSFET model, V_{Tn} is the threshold voltage in the normal configuration, and the body voltage dependence has been implicitly incorporated. The function f does not make any other *a priori* assumptions as to the model describing the relationship between drain current and applied voltages. The intrinsic gate-to-source and drain-to-source voltages can be expressed in terms of their extrinsic counterparts as

$$V_{GS} = V_{gsn} - I_{dn} R_S \tag{47}$$

and

$$V_{DS} = V_{dsn} - I_{dn}\left(R_S + R_D\right) , \tag{48}$$

where V_{gsn} and V_{dsn} represent the extrinsic gate-source and drain-source voltages, respectively, in the normal configuration. In a similar manner, the source current in the inverse configuration is given by

$$I_{si} = f\left[\left(V_{GD} - V_{Ti}\right), V_{SD}\right] , \tag{49}$$

where V_{Ti} is the threshold voltage in the inverse configuration, and V_{GD} and V_{SD} are the intrinsic gate-drain and source-drain voltages, respectively. These voltages can be related to their extrinsic counterparts by

$$V_{GD} = V_{gdi} - I_{si} R_D \tag{50}$$

and

$$V_D = V_{sdi} - I_{si}\left(R + R_D\right) , \tag{51}$$

where V_{gdi} and V_{sdi} are the extrinsic gate-drain and source-drain voltages, respectively, in the inverse configuration. If the device in both configurations is biased with the same source-drain voltage (i.e., $V_{sdi} = V_{dsn}$) and V_{gdi} is adjusted until the source current in the inverse configuration is equal to that in the normal configuration (i.e., $I_{si} = I_{dn} = I_d$), then the normal and inverse intrinsic gate voltage overdrive must be the same:

$$\left(V_{GS} - V_{Tn}\right) = \left(V_{GD} - V_{Ti}\right) . \tag{52}$$

Substituting Eqs. (47) and (50) into Eq. (52) yields

$$I_d\left(R_D - R_S\right) = \left(V_{gdi} - V_{gsn}\right) - \left(V_{Ti} - V_{Tn}\right) . \tag{53}$$

The term $(V_{Ti} - V_{Tn})$ in the above equation is small, when the device is biased in the linear region, because $(V_{DB} + -V_{SB})$ is small. Therefore it can be approximated by the first term of its Taylor series expansion as

$$\left(V_{Ti} - V_{Tn}\right) \approx I_d\left(R_D - R_S\right) \frac{dV_T}{dV_{SB}} . \tag{54}$$

Combining Eq. (53) into Eq. (54) gives

$$\left(R_D - R_S\right) = \frac{\left(\dfrac{V_{gdi} V_{gsn}}{I_d}\right)}{1 + \dfrac{dV_T}{dV_{SB}}} , \tag{55}$$

where the dependence of the threshold voltage on the source-to-body voltage V_{SB} is accounted for by the term $(1 + dV_T / dV_{SB})$ in Eq. (55).

6. Conclusion

We have presented an overview of the modeling of long-channel bulk MOSFET as a particular case of the long-channel SOI. We have reviewed, compared and scrutinized various methods to extract the threshold voltage, the effective channel and the individual values of drain and source resistances. We have stressed the implicit assumptions and limitations of each method and we have proposed variations in order to improve them.

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