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Evolutionary algorithms for global parametric fault diagnosis in analogue integrated circuits

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Abstract. An evolutionary method for analogue integrated circuits diagnosis is presented in this paper. The method allows for global parametric faults localization at the prototype stage of life of an analogue integrated circuit. The presented method is based on the circuit under test response base and the advanced features classification. A classifier is built with the use of evolutionary algorithms, such as differential evolution and gene expression programming. As the proposed diagnosis method might be applied at the production phase there is a method for shortening the diagnosis time suggested. An evolutionary approach has been verified with the use of several exemplary circuits – an oscillator, a band-pass filter and two operational amplifiers. A comparison of the presented algorithm and two classical methods – the linear classifier and the nearest neighborhood method – proves that the heuristic approach allows for acquiring significantly better results.

Key words: analogue integrated circuits, fault diagnosis, localization, identification, evolutionary algorithms.

1. Introduction

A technology of analogue integrated circuits manufacturing has improved greatly in recent years. Analogue and hybrid integrated circuits (AIC) are used in a variety of applications, starting with telecommunication industry, through control and measurement devices, to aeronautics. Quality and reliability of employed AIC perform a requirement for guarantee safety of its users. Hence, it is essential to develop efficient routines of AIC diagnosis at the mass production stage as well as at the prototype stage when it is possible to correct and adjust technological process parameters for the better AIC reliability and improved production yield.

Tools for test generation and fault diagnosis of digital electronic circuits are well-developed, to the point of their full automation. Meanwhile, analogue integrated circuits diagnosis strategies are still evolving. AIC testing is particularly difficult by the following reasons:

- Analogue circuit parameters have continuous values. Under fault, they may assume values within the range from zero to infinity. Moreover, it is necessary to take circuit parameters' tolerances masking effect into account.
- The fault influence is propagated toward both input and output of the circuit.
- Analogue signals are complex and continuous [1–14] in their nature.

There are additional issues that need to be addressed in the IC testing and diagnosis:

- AIC are relatively small (single millimeters) thus the number of and the access to test pads is limited [1–4].
- The character of faults in AIC is different from discrete analogue circuits which results from the manufacturing process. A new kind of faults – multiple and proportional parametric faults (global parametric faults) – is one of the most important issues that needs to be investigated in AIC diagnosis [1, 3, 5].

Traditionally, fault diagnosis of any circuit has three objectives [3, 5]: *fault detection, fault location* and *fault identification*. The first of them provides the answer whether the circuit under test (CUT) meets design specification requirements (GO/NO-GO test). Fault location (isolation) allows for answering the question which of circuit parameters are faulty and the fault identification determines the amount of the deviation (of faulty circuit parameter) from the nominal value. They are very important at the prototype phase of an AIC design and manufacturing. Applying algorithms for a fault location and identification at this stage allows for adjusting each of technological process parameters, thus, for increasing the production yield. This paper addresses the global parametric fault location in AIC problem.

Evolutionary algorithms [15–21] such as differential evolution [15, 16, 19, 20] or gene expression programming [17, 18], are a recognized tool of optimization. Both of utilized in this work algorithms, that is gene expression programming (e.g. [22, 23]) and differential evolution have been applied for analogue circuits diagnosis.

This paper summarized our research. Considering this fact, we decided to organize it in manner reflecting following stages of our work. Global parametric fault model is presented in Sec. 2. There are time domain base features defined. Section 3 covers the application of gene expression programming and differential evolution for the purpose of global parametric fault identification. We present results of our diagnosis method's verification with the use of exemplary circuits in Sec. 4 and the whole article is concluded in Sec. 5.

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2. Terms and definitions

A global parametric fault (GPF) is a multiple and correlated parametric fault affecting a large part of or even a whole chip [5]. The cause of GPF is usually the effect of manufacturing process incorrect parameters, seldom – the effect of process parameters natural variation or other, irregular, causes [24–34].

There is a need of a GPF model for the purpose of the analysis of a GPF influence on the tested circuit [1, 2, 34]. This model has been created with a several assumptions based on the AIC fabrication process character. The most important was presuming that all circuit parameters are manufactured in a single, multistage process [2, 3, 28–31].

2.1. GPF model of integrated circuit. We have assumed that circuit parameters might be grouped according to, e.g. their type, their location on the chip, and the like. Let us assume that the nominal circuit is given with a set:

$$\mathbf{P_{nom}} = \left\{ p^j_{nom,i}; i = 1, \ldots, N^j; j = 1, \ldots, G \right\}, \quad (1)$$

where $p^j_{nom,i}$ denotes a nominal value of an i-th circuit parameter from a j-th circuit parameters' group, N^j – the number of circuit parameters in j-th group and G is the number of groups.

A fabricated integrated circuit may be described with a set:

$$\mathbf{P} = \left\{ p^j_i; i = 1, \ldots, N^j; j = 1, \ldots, G \right\}. \quad (2)$$

Defining the value of real circuit parameters (p^j_i) there is a need of considering manufacturing process deviations. Usually, there are two types of circuit parameters' tolerances taken into account: the absolute and coupling tolerance [28-30]. The former defines the circuit parameters' maximal deviation from the nominal value and the latter specifies the maximum deviation of the relation between correlated circuit parameters' values. The absolute tolerance specifies the influence of manufacturing process' fluctuations on the whole chip, while the coupling tolerance defines effects of fabrication process local wavering [1, 2, 32, 33].

Let us assume that values of absolute tolerances for circuit parameters' group are given with a vector:

$$\mathbf{A_T} = \left\{ \alpha^j; j = 1, \ldots, G \right\} \quad (3)$$

and a vector of coupling tolerances for each o circuit parameters' group:

$$\mathbf{\Xi} = \left\{ \xi^j; j = 1, \ldots, G \right\}. \quad (4)$$

Both coupling and absolute tolerances have been assumed for each of circuit parameters' groups.

A set of faulty circuit parameters is defined with:

$$\mathbf{F} = \left\{ f^j_i : f^j_i = \delta^j_i \cdot p^j_{nom,i}; \; f^j_i \notin \left\langle p^j_{nom,i} \cdot \left(1 - \alpha^j\right),\ p^j_{nom,i} \cdot \left(1 + \alpha^j\right) \right\rangle \right\}, \quad (5)$$

where f^j_i denotes a faulty circuit parameter and δ^j_i is a random variable.

A set of circuit states, e.g. affected by faulty transistor channels widths, is given with:

$$\mathbf{S} = \{ S_s : s = 0, \ldots, \theta \}, \quad (6)$$

where S_0 denotes a non-faulty circuit.

The aim of fault location is classifying CUT to one of the prior assumed circuit states. This task is significantly more complex if circuit parameters tolerances are taken into account. There are several methods addressing this problem [5, 6]. However, one the most commonly used is Monte Carlo analysis [5, 6, 11–14]. Not only it provides means to analyse the influence of circuit parameters values influence in the effective natural way, but also allows for determining ambiguity sets, i.e. sets containing possible circuit states which cannot be distinguished under any conditions [3, 5]. The main disadvantage of Monte Carlo analysis is its high computational cost.

2.2. Circuit response base features. A system for AIC diagnosis is presented in Fig. 1. The testing procedure can be applied in DC, AC, or time domain. Let us consider a time domain stimuli $x(t)$ and an output response evaluation $y(t)$. First order derivative of the output response – $y'(t)$ – can be calculated. The use of the CUT response changes' velocity has been inspired by biomedical signal processing, e.g. [34–38].

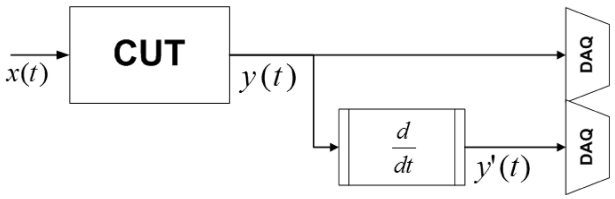


Fig. 1. The diagnosis system

The probed circuit response (**y**) and its first order derivative (**y′**) are defined with equations:

$$\mathbf{y} = \{ y_k : k = 0, \ldots, K-1 \,;\, y_k = y\left(t = k \cdot \Delta t_y\right) \}, \quad (7)$$

$$\mathbf{y'} = \{ y'_k : k = 0, \ldots, K-1;\ y'_k = y'\left(t = k \cdot \Delta t_y\right) \}, \quad (8)$$

where Δt_y is a sampling period.

There are several time response features (e.g. rising time, steady state value, slew rate, overshoot voltage, etc.) applied for AIC diagnosis. In the presented approach, time response's and its derivative's maxima and minima locations have been considered [24].

Maxima and minima form a set of base features that is used in the process of AIC diagnosis:

$$\mathbf{BF} = \left\{ bf^m = \left(bf^m_x, bf^m_y\right); m = 1, \ldots, M \right\}, \quad (9)$$

where $bf^m = \left(bf^m_x, bf^m_y\right)$ are coordinates, i.e. the time of occurring and the value, of each of M extracted base features.

Simple features (SF) are an outcome of transformations of one or two base features and the advanced feature (AF) is an outcome of an transformation of simple features. This feature can be expressed as follows:

$$af = (af_x, af_y). \quad (10)$$

It is possible to present base and advanced features in the Cartesian coordinate system. This possibility of presentation has been utilised in the process of a fault dictionary construction which we describe in the following parts of this paper.

The use of CUT response's derivative might be questioned, especially in the aspect of signal-to-noise ratio. Admittedly, we did not investigate this matter thoroughly. Nonetheless, our research confirm that in certain cases the incorporation of the first order derivative may allow for acquiring additional data. An exemplary circuit presented in the further part of this paper may serve as an example. Its response to a test excitation has been presented in Fig. 2a. Obviously, the CUT response does not allow for extracting satisfactory diagnostics information (Eq. 9). We acquired only one base feature. The use of a first order derivative (Fig. 2b) allowed us to extract and employ additional four base features. Extracted base features have been presented in the Fig. 6.

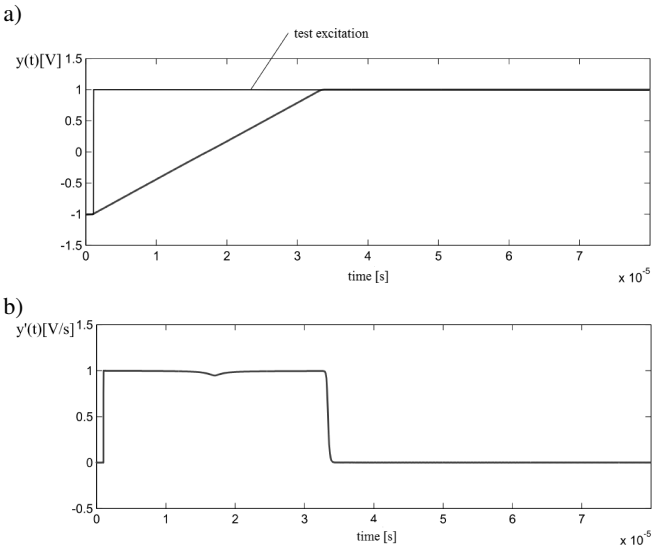


Fig. 2. A μA741 operational amplifier: a) response to a test excitation and b) its first order derivative

3. Global parametric faults classification

3.1. Algorithm outline. The circuit state classifier has been built with the use of *DeGep* and differential evolution developed by authors. *DeGep* is a hybrid of two evolutionary algorithms, i.e. gene expression programming (GEP) [17, 18, 23] and differential evolution (DE) [19].

The block diagram of classifier construction algorithm has been presented in Fig. 3. Below, we will outline functions of the most important blocks of this diagram.

In the beginning of the dictionary construction, a set of circuit states is assumed and all required CUT simulations are performed. Monte Carlo analysis of N_{MC} runs allows for analyzing the circuit parameters tolerances' influence.

The CUT time domain response is measured and then the first order derivative is calculated. It gives the set of M base features (block 2) which are extracted and normalized with respect to non-faulty circuit performance. It ends the preparations for further computation. In the following algorithm's stages the base features are analyzed and employed for the best dictionary-based diagnosis efficiency.

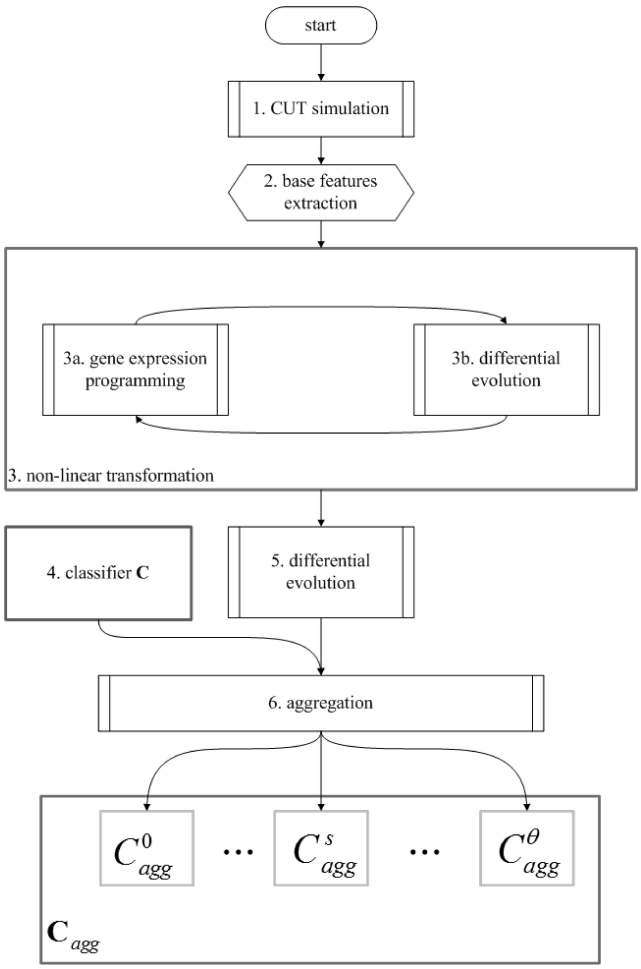


Fig. 3. A single classifier construction method block diagram

Blocks 3 through 6 of the algorithm are discussed in details in sub-chapters 3.2–3.3. Below, we present a brief presentation of these blocks' functions.

Operations presented in block 3 and 4 may be carried independently. A set of classifiers for each of base features is constructed (block 4). This procedure is carefully elaborated in sub-section 3.2. In the block 3, a base features non-linear transformation is applied. The process is automated with the use of author's *DeGep* algorithm. Basically, gene expression programming is used to find a set of non-linear transforming function between measurements and features to improve circuit states separation. Differential evolution has been nested in and applied to find the value of GEP fitness function. Circuit state classifiers are built in DE short. It allows for estimating the circuit states separation level. The effect of classification is used to determine the fitness value (described in the following parts of this paper).

Transformed BFs form an AF which is classified with the use of DE. The algorithm is, generally, the same as in GEP

fitness function. The population size and number of generation, though, are significantly bigger (block 5), e.g. 5 to 10 times. The latter allows for acquiring more accurate results.

The outputs of classifiers built for the AF as well as for all base features (block 4) is then aggregated (block 6), which is also the final step of the classifier construction algorithm. The procedure of aggregation is presented in Subsec. 3.4.

3.2. Circuit state classification with the use of differential evolution. Let us assume classifiers separating considered circuit states. Thus, a set $\mathbf{C}$ of $M+1$ classifiers' groups for each of circuit states is (one for each of extracted base features – block 4 in the Fig. 3):

$$\begin{aligned}\mathbf{C} &= \{\mathbf{C^{m,s}}; m = 1, \ldots, M+1; s = 0, \ldots, \theta\} \\ &= \{f(\cdot)_1^{m,s}; l = 1, \ldots, L\},\end{aligned} \tag{11}$$

is consisted of L grouping inequalities for each of M base features and the advanced feature (hence $M+1$) and for each of $\theta+1$ circuit states. A base feature is representing an s-th circuit state if an only if:

$$\underset{l}{\forall} f\left(bf^m\right)_l^{m,s} < 0. \tag{12}$$

A similar condition must be fulfilled for an advanced feature.

The process of finding the classifier $\mathbf{C}$ is presented in Fig. 4.

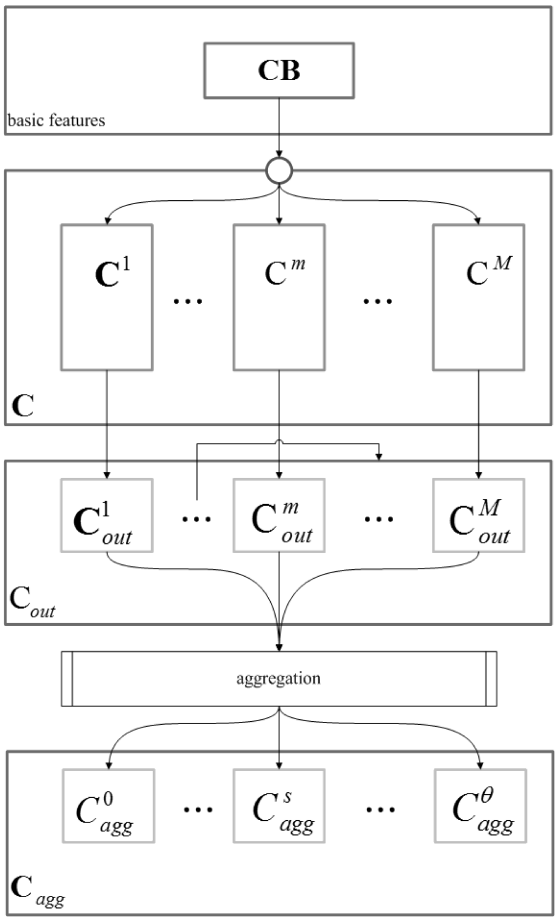


Fig. 4. The fault dictionary construction

Each of base features defines a Cartesian space. The possibility of presenting maxima and minima in rectangular coordinates has been utilized for the purpose of circuit states classification. In our research, we found out that following four dependences ($L = 4$) are sufficient to define a classifier given with Eqs. (11) and (12):

$$x_p^m - bf_x^m < 0, \tag{13}$$

$$bf_x^m - x_k^m < 0, \tag{14}$$

$$\begin{aligned}&\left(a_1^m \cdot \left(bf_x^m\right)^{-1} + b_1^m \cdot \left(bf_x^m\right)^2\right. \\ &\left. + c_1^m \cdot bf_x^m + d_1^m\right) - bf_y^m < 0,\end{aligned} \tag{15}$$

$$\begin{aligned}bf_y^m - &\left(a_2^m \cdot \left(bf_x^m\right)^{-1} + b_2^m \cdot \left(bf_x^m\right)^2\right. \\ &\left. + c_2^m \cdot bf_x^m + d_2^m\right) < 0,\end{aligned} \tag{16}$$

Coefficients $x_{p/k}^m$, $a_{1/2}^m$, $b_{1/2}^m$, $c_{1/2}^m$ and $d_{1/2}^m$ are found with the use of differential evolution. It is possible to approximate (with the area defined with equations (13)–(16)) the distribution of base features for each of the circuit states and each of AIC samples with the use of Monte Carlo analysis. The fitness function constructed for this purpose is given with an equation:

$$F_{fit} = \begin{cases} \sum\limits_{k=1}^{5} w_k^1 \cdot F_k + \sum\limits_{l=1}^{4} P_l & \text{if } F_1 < F_{1\min}, \\ \sum\limits_{k=1}^{6} w_k^2 \cdot F_k + \sum\limits_{l=1}^{4} P_l & \text{if } F_1 > F_{1\min}, \end{cases} \tag{17}$$

where F_1 denotes number of AIC chips classified correctly, $F_{1\min}$ is a minimum acceptable number of correctly classified states, F_{2-5} denote the size of the classifier (given with the distance between x_p and x_k, y_1 and y_2 curves, etc.), F_6 denotes the number of other circuit states classified *incorrectly* with the being determined classifier, P_{1-4} are penalty functions which are expected to remove the invalid individuals (e.g. with too small or too big distance between x_k and x_p) from the population. Weights $w_k^{(\cdot)}$ are chosen empirically for the best algorithm performance.

Classifier $\mathbf{C}$ produces the output matrix of bits:

$$\begin{aligned}\mathbf{C_{out}} &= \{\mathbf{C_{out}^m}\} \\ &= \{C_{out}^{m,s} : m = 1, \ldots, M; s = 0, \ldots, \theta\},\end{aligned} \tag{18}$$

where the bit $C_{out}^{m,s}$ is active, i.e. equals 1, if and only if the input IC sample of m-th base feature has been classified as s-th circuit state. It is possible that a single response's feature is classified as more than a single circuit state, i.e. to an ambiguity set (more than one bit value is 1).

The presented procedure is applied in the 4^{th} block of the flowchart presented in the Fig. 3. We used the same method, with a limited number of generations, to determine the fitness function in *DeGep* algorithm (3^{rd} block in the flowchart, sub-block 3b).

3.3. Circuit state classification with the use of *DeGep* . Let us assume a set of simple features:

$$\mathbf{SF} = \{\mathbf{SF^z} : \mathbf{SF^z} = f_{SF}^z(\mathbf{BF}); f_{SF}^z \in \mathbf{F_{SF}}\}, \tag{19}$$

where $\mathbf{F}_{SF}$ set of base function (see Eq. (23)–(31)) defining simple features:

$$\mathbf{F_{SF}} = \{f_{SF}^{z} : z = 1, \ldots Z\} \tag{20}$$

and f_{SF}^{z} – z-th base function defining a simple feature, **BF** – base features set.

Additionally, let the set **AF** be consisted of advanced circuit response features:

$$\mathbf{AF} = \{\mathbf{AF^r} : \mathbf{AF^r} = f_{\mathbf{AF}}^{r}(\mathbf{SF}) ; f_{\mathbf{AF}}^{r} \in \mathbf{F_{AF}}\}, \tag{21}$$

where $\mathbf{F}_{AF}$ contains base functions used in advanced features calculation:

$$\mathbf{F_{AF}} = \{f_{\mathbf{AF}}^{r} : r = 1, \ldots R\}. \tag{22}$$

Each of advanced features can be presented in Cartesian coordinates system (Eq. (9)).

The aim of computing advanced features is to increase circuit states identification efficiency. In the process of finding advanced features new dependences between base features might be discovered and utilized. Determining the best advanced feature is an NP-hard problem. This process has been automated with author's *DeGep* algorithm.

DeGep algorithm is a hybrid of two evolutionary algorithms – Gene Expression Programming, which is used as the main optimization engine, and Differential Evolution, which is used to determine the fitness function value. This algorithm is used in the block 3 of the flowchart presented in Fig. 3.

The applied base functions could be classified into two groups:

- **Shaping one argument functions** changing the shape of samples distribution.
- **Relations** of two arguments. The aim of applying these functions is to find and incorporate dependences between arguments.

We have decided to use a cellular individuals coding. Sub-ET allowed for finding simple features (A-C in the Fig. 5). In the presented implementations Sub-ETs consisted of one base function and two terminals. The cell have been defining an advanced feature.

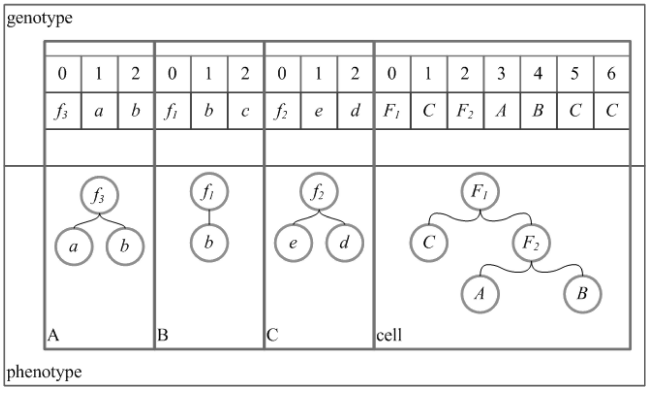


Fig. 5. A GEP cellular individual

There have been following *shaping* functions utilized in both sub-ETs and the cell:

$$\sin\left((\cdot)_{x/y/x,y}\right), \tag{23}$$

$$\left|(\cdot)_{x/y/x,y}\right|, \tag{24}$$

$$\log_{10}\left((\cdot)_{x/y/x,y}\right), \tag{25}$$

$$\sqrt{(\cdot)_{x/y/x,y}} \tag{26}$$

and the following *relations* (i, j denote i-th and j-th simple feature):

$$(\cdot)_{x/y}^{i} + (\cdot)_{x/y}^{j}, \tag{27}$$

$$(\cdot)_{x/y}^{i} - (\cdot)_{x/y}^{j}, \tag{28}$$

$$(\cdot)_{x/y}^{i} \cdot (\cdot)_{x/y}^{j}, \tag{29}$$

$$\frac{(\cdot)_{x/y}^{i}}{(\cdot)_{x/y}^{j}}, \tag{30}$$

$$\left((\cdot)_{x/y}^{i}\right)^{(\cdot)_{x/y}^{j}}. \tag{31}$$

Shaping functions have been defined in three options (over either of dimensions only or over both dimensions) and relations have been defined in two options (over corresponding dimensions or cross-over – x vs. y), e.g. $\frac{\mathbf{BF_x^2}}{\mathbf{BF_y^4}}$ would mean dividing the value x (moment of appearing) of the second base feature by the value y of the fourth base feature (voltage).

There has been an evolutionary fitness function applied in *DeGep* algorithm. The fitness value has been calculated with the use of DE. In a short periods of evolution a set of classifiers is found which allows for estimating of the circuit states separability. The advanced feature have been utilised for the circuit states classification with the algorithm presented in the Subsec. 3.2. The effect of the fault identification have been assessed and used as a fitness value.

The effect of *DeGep* application has been presented in Figs. 6 and 7. In Fig. 6, there are presented base features that have been extracted for one of the exemplary circuits discussed in the following section (an operation amplifier μA741). In Fig. 7, there is presented the effect of the non-linear transformation together with following circuit states classifiers areas.

The advanced feature presented in the Fig. 7 is given with an equation:

$$\mathbf{AF} = \log_{10}\left(\mathbf{BF_{x,y}^3}\right) - \sqrt{\mathbf{BF_x^4}}, \tag{32}$$

where $\mathbf{BF}^3$ and $\mathbf{BF}^4$ are 3^{rd} and 4^{th} extracted base features respectively.

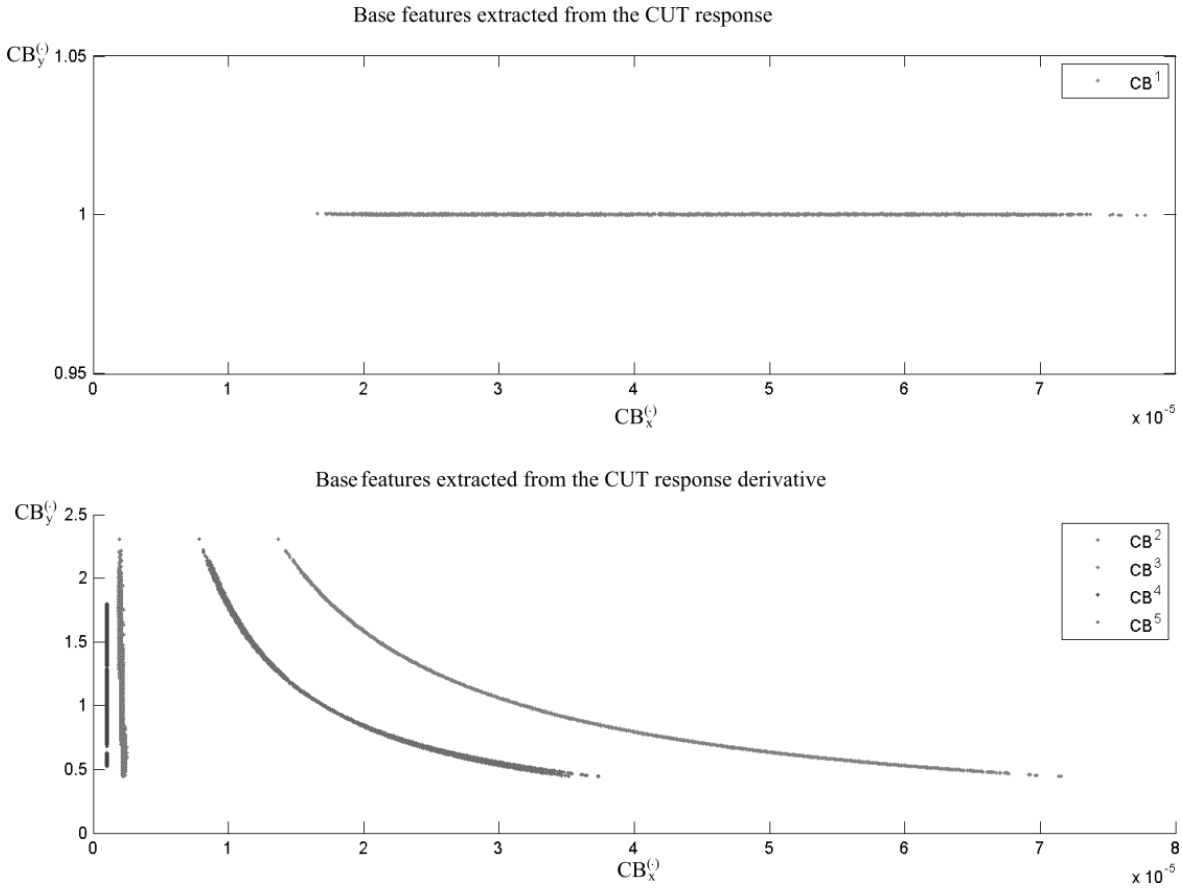


Fig. 6. Extracted and normalised base features for the exemplary μA741 amplifier

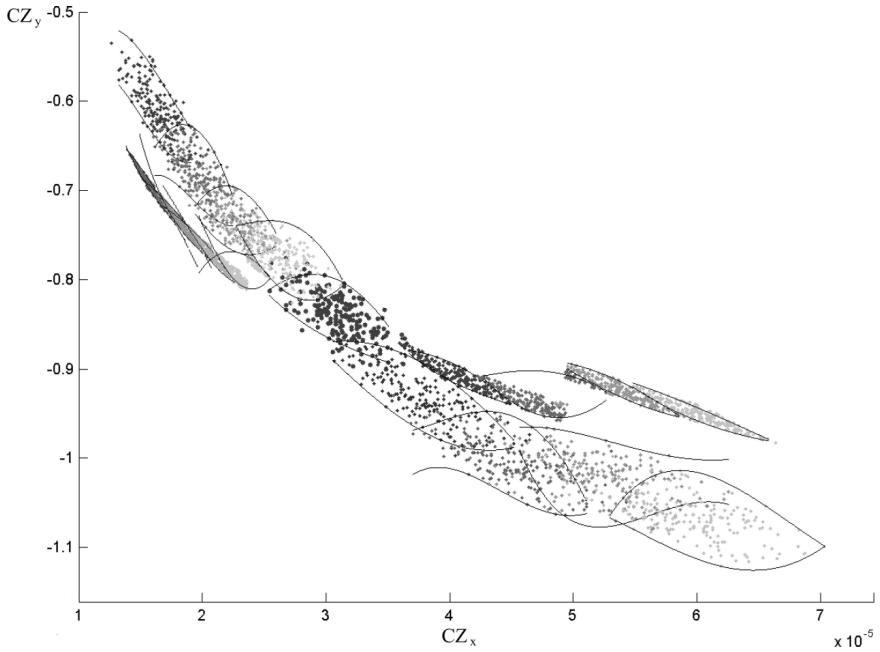


Fig. 7. Calculated advanced feature for the μA741 operational amplifier. For the purpose of increasing the location efficiency additional circuit states have been assumed, i.e. each of global parametric faults have been divided into four sub-ranges

3.4. Aggregation. Procedures given with block 3 and 4 effect with a set of $M+1$ binary vectors. The output vector acquired with the *DeGep* block is concatenated to the $\mathbf{C}_{out}$ set, being its *M+1*-th element. It is necessary to reduce this set to a vector. The aggregation has been applied with the use of differential evolution.

The $\mathbf{C}_{agg}$ vector is given with an equation:

$$\mathbf{C_{agg}} = \sum_{m=1}^{M+1} Q_j \cdot \mathbf{C_{out}^m}, \tag{33}$$

where coefficients Q_j are being found with differential evolution. The fitness function is expected to maximize number of unequivocally and correctly classified IC samples.

The acquired vector requires a normalisation:

$$\text{for } s = 0, \ldots, \theta \quad C_{agg}^s = \left\lfloor \frac{C_{agg}^s}{\max\limits_{s=0,\ldots,\theta} C_{agg}^s} \right\rfloor. \tag{34}$$

3.5. Computation time. Fault dictionary construction time t_{con} is given with an equation:

$$t_{con} = t_{sim} + t_{EA}, \tag{35}$$

where t_{sim} – CUT simulation time (including Monte Carlo analyses), t_{AE} – evolutionary algorithms processing time.

The simulation time depends on the chosen measurement interval, sampling period, complexity of the circuit under test, number of circuit states, number of circuit parameters group, etc. The more complicated the circuit is the longer it takes to perform all required analysis. On the other hand, the whole process is performed only once at the before test stage.

Evolutionary algorithms work time does not depend on the circuit's complexity. It depends only on a number of circuit states, a number of extracted base features, evolutionary algorithm's parameters, and the like.

In the presented paper $t_{sim} > t_{AE}$, which has been few hours for the most complicated exemplary circuit (twelve base features extracted).

4. Examples

We verified the presented diagnosis method with the use of three exemplary circuits, i.e.:

- an operational amplifier μA741 (Fig. 8),
- an integrated CMOS amplifier (Fig. 9),
- a filter (Fig. 10).

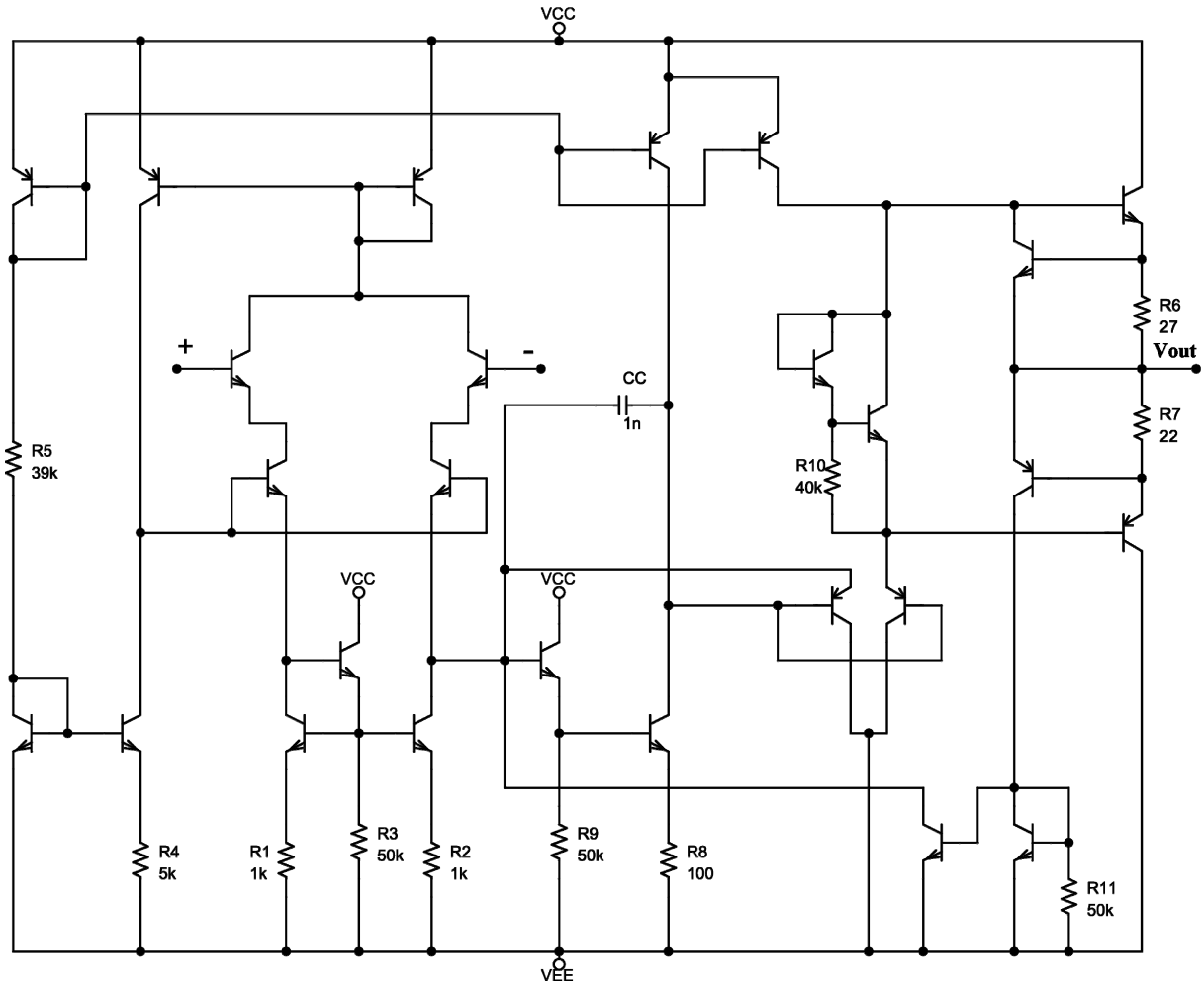
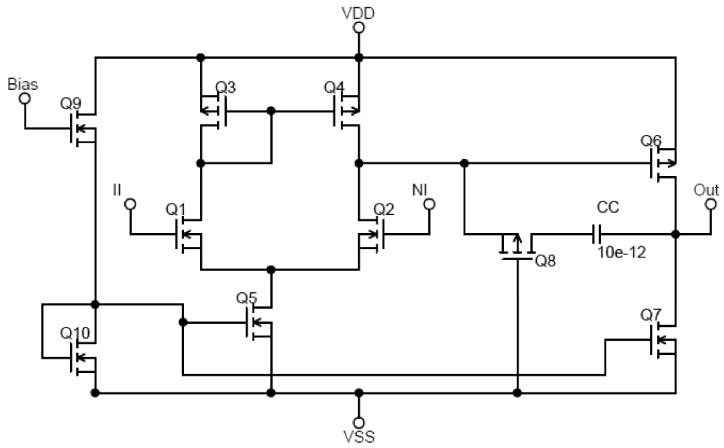


Fig. 8. An exemplary circuit – operation amplifier μA741



	L [1e-6m]	W [1e-6m]
Q1	10	66
Q2	10	66
Q3	10	60
Q4	10	60
Q5	10	54
Q6	10	474
Q7	10	214
Q8	10	10
Q9	10	200
Q10	64	10

Fig. 9. An exemplary circuit – a CMOS operational amplifier. The geometry of transistors is given in the table

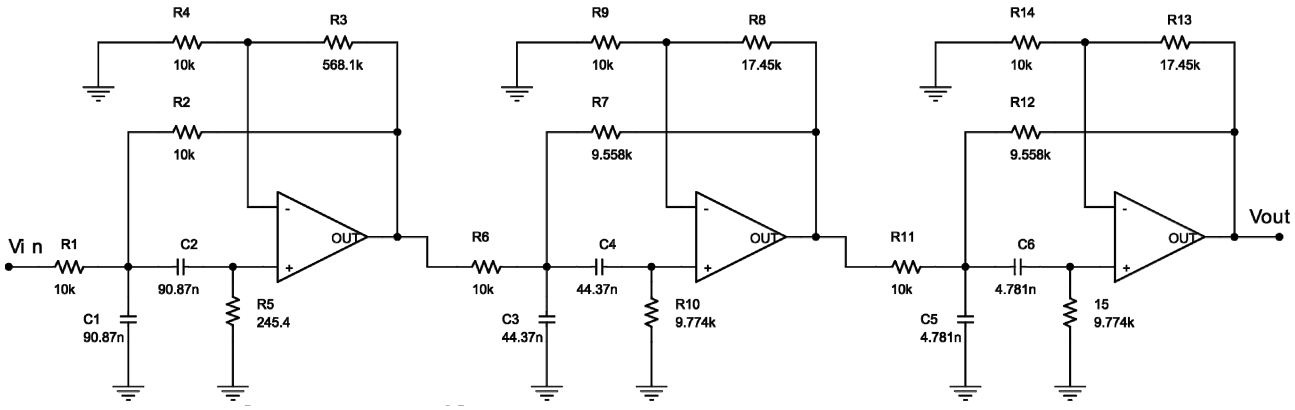


Fig. 10. An exemplary circuit – a filter

4.1. Diagnosis environment. During Monte Carlo analyses we took into account passive circuit parameters (Eqs. (1)–(5)):

- resistances (absolute tolerance $\alpha = 14.0\%$, coupling tolerance $\xi = 1.0\%$),
- capacitances ($\alpha = 19.0\%$, $\xi = 1.0\%$),

and following CMOS transistors' parameters:

- transonductance coefficient ($\alpha = 5.0\%$, $\xi = 0.5\%$),
- oxidation thickness ($\alpha = 5.0\%$, $\xi = 0.5\%$),
- treshold voltage ($\alpha = 5.0\%$, $\xi = 0.5\%$),
- channel length and width ($\alpha = 5.0\%$, $\xi = 0.5\%$).

Passive circuit parameters tolerances have been chosen based on multiple publications, e.g. [1, 2, 25–29, 32, 33].

Operational amplifiers have been tested in the voltage repeater configuration. We assumed the use of the simplest test excitation – a voltage step. We did not analyse the optimal excitation choice.

Monte Carlo analysis has been applied to create two sets: a teaching set (100 samples for each of assumed circuit states) and the validation set (200 samples for each of assumed circuit states).

In each case faults in two circuit parameters groups have been taken into account:

- in resistances and capacitances for μA741 amplifier and the filter,
- in channels' lengths and widths for CMOS amplifier.

The faulty regions were given with ranges:

- $< 50\%,80\% >$ and $< 120\%,150\% >$ of the nominal values for resistors,
- $< 50\%,75\% >$ and $< 125\%,150\% >$ of the nominal values for capacitors,
- $< 50\%,90\% >$ and $< 110\%,150\% >$ of the nominal values for channels widths and lengths.

Effectively, five circuit states have been distinguished (two faults for each of circuit parameters groups and the non-faulty circuit).

4.2. Diagnosis results. Diagnosis results have been presented in the Table 1. For the purpose of a circuit states identification with the use of classical classification techniques, i.e. a linear classifier and Nearest Neighborhood Method classifier, submitted.

Table 1
Diagnosis results

Exemplary circuit	Indicator	Evol. Method	Linear Class.	NNM Class.
μA741	Detection [%]	94.0	80.0	66.0
	False positive [%]	1.2	1.6	1.5
	Located incorrectly [%]	9.6	47.4	58.3
	Not located[%]	0.0	0.0	0.0
	Unequivocal location [%]	87.0	52.6	41.7
	Located correctly (with ambiguity sets) [%]	90.4	52.6	41.7
CMOS operational amplifier	Detection [%]	97.0	81.0	68.0
	False positive [%]	3.0	1.2	1.5
	Located incorrectly [%]	5.2	44.4	55.1
	Not located[%]	0.0	0.0	0.0
	Unequivocal location [%]	94.6	55.6	44.9
	Located correctly (with ambiguity sets) [%]	94.6	55.6	44.9
Filter	Detection [%]	99.0	95.0	10.0
	False positive [%]	1.5	0.5	6.0
	Located incorrectly [%]	19.6	49.5	81.5
	Not located[%]	0.0	0.0	0.0
	Unequivocal location [%]	61.0	50.5	18.5
	Located correctly (with ambiguity sets) [%]	78.9	50.5	18.5

The method presented in this paper has allowed for significantly better faults identification in each of presented examples.

Over 90% of non-faulty circuits have been correctly classified for considered examples. The results are generally better than acquired with the classical method, i.e. the linear classifier and the NNM classifier (4.0% for the filter, up to 16% for the CMOS operational amplifier). High detection rate has not affected the false positive results indicator. 3.0% circuit samples, at most, have been incorrectly classified as non-faulty circuits.

Moreover, the method is characterized by a low level of incorrect classification (between 5.2% and 19.6% for the presented method in comparison with 47.4% and 81.5% for classical methods).

Majority of circuit states (IC samples) have been classified correctly and unequivocally in each of cases (between 61.0% for the filter and 94.6% for the CMOS operation amplifier). The acquired results are, again, significantly better than ones we got with the use of classical classification method.

The unquestionable advantage of the author's diagnosis method is utilization of ambiguity sets. Narrowing possible faults to not more than two element sets has greatly increased the classification efficiency. The effect is the most significant in the analysed filter case (17.2%).

5. Conclusions

The paper describes a new method for global parametric fault diagnosis in AIC. The classification of an AIC states is carried out with the use of time domain response where base, simple and advanced features are considered. The base features come from the IC response, simple and advanced ones are delivered by a set of functions. Authors present heuristic method (DeGep) for the purpose of classifier construction which links differential evolution (De) and gene expression programming (Gep). The classifier consists of four independent functions which surrounds the GPF in AIC, where two of them are linear ones and other two are given with polynomials (Eqs. (13)–(16)). The effectiveness of proposed approach has been verified with a number of examples, three of them are presented in the paper. Comparison to classical methods like the nearest neighborhood method and the linear classifier, the DeGep indicates high detection and location rate of GPF, has been presented. Another big issue is a creation of base and advanced features in order to increase the efficiency of localization and identification of GPF. An application of differential evolution and gene expression programming to GPF diagnosis in AIC is absolutely new and must be considered by test engineers during prototype and production stage of a new AIC.

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