Invited paper

Prospects and Development of Vertical Normally-off JFETs in SiC

Mietek Bakowski

Abstract— This paper reviews the prospects of normally-off (N-*off*) JFET switch in SiC. The potential of selected vertical JFET concepts and all-JFET cascode solutions for N-*off* operation is analyzed using simulations. The performance of analyzed concepts is compared in terms of blocking voltage, specific on-state resistance, maximum output current density and switching performance in the temperature range from 25°C to 250°C. The main objective of the analysis is to ascertain consequences of different design and technology options for the total losses and high temperature performance of the devices.

Keywords— JFET cascode, normally-off, SiC, vertical JFET.

1. Introduction

A voltage-controlled, normally-off (N-*off*) SiC switch with specific on-state resistance of around $1.0\,\mathrm{m\Omega\,cm^2}$ is desired by many applications including the high volume automotive market. During the recent years several concepts including metal oxide semiconductor field effect transistor (MOSFET) and junction field effect transistor (JFET) designs have been developed to realize such an ideal SiC switch [1]–[4]. The SiC MOSFET would be the device of choice as soon as the SiO_2/SiC interface and reliability issues are solved. Meanwhile, SiC JFET designs are becoming more and more interesting, because of their ruggedness and the achievable low on-state resistance.

2. SiC Switch Concepts

The JFET is presently the most mature switch concept in SiC transistor technology. There are historically several factors accounting for that. First of all, the high electric field strength and the reasonably high electron mobility of SiC make unipolar SiC devices interesting for high voltage applications [5]. As a unipolar device the JFET is forgiving with respect to material quality and does not suffer from bipolar instability [6].

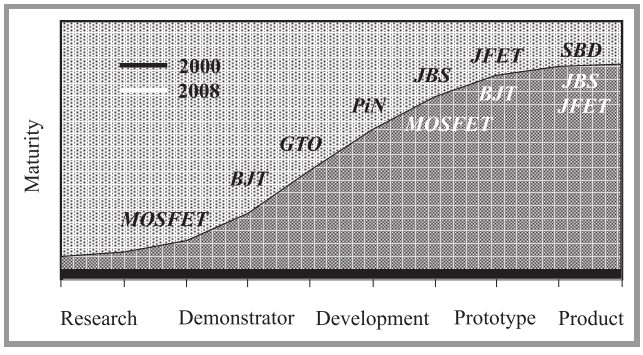


Fig. 1. Maturity of main SiC rectifiers and switches. Explanations: BJT – bipolar junction transistor, GTO – gate turn-off thyristor, PiN – p-i-n rectifier, JBS – junction barrier-controlled Schottky rectifier, SBD – Schottky barrier diode.

In addition, it does not require as high SiO_2/SiC interface quality as that needed in the MOSFET, since it's function depends on the conducting channel situated in the bulk of the device and controlled by the reverse biased p-n junction. Finally, the wide band gap of the SiC material gives SiC JFETs advantage of the high temperature operation and facilitates N-*off* design due to the high value of the build-in voltage.

Figure 1 illustrates schematically the status of SiC switch concepts during the last decade.

3. Advantages of JFET Technology

The JFET can be realized using epitaxial growth for the main voltage controling junctions and for the conduction channel. In this way ion-implantation can be avoided. Ion implantation is in these two cases a performance limiting technology due to excessive damage especially for high doping concentrations. The high quality of the conduction channel and good control of the channel dimensions and doping are crucial for the JFET performance. The normally-on (N-*on*) JFET design is capable of extremely low on-state resistance. Only the SiC BJT has the potential of comparably low on-state voltage due to the even number of p-n junctions configured in such a way that they compensate each other's built-in voltage in saturation. Finally, the JFET does not require the use of an anti-parallel diode reducing the number of semiconductor components in a system [7], [8].

Normally-on JFETs are not easily accepted by the market due to system safety requirements, regardless of their excellent on-resistance. N-*off* JFETs on the other hand require a narrow and relatively low doped channel to ensure the N-*off* performance, and thus pay a penalty in terms of the on-state performance. N-*off* JFETs are also vulnerable to the electromagnetic interference (EMI) noise due to the small range of the gate control voltage. Hence, the gate control circuitry for JFETs requires special attention to ensure reliable operation. In the case of N-*on* JFETs the development of inherently safe gate drivers is particularly desired in order to guarantee the safety of the whole system [9].

4. N-*off* Epitaxial JFET Concepts

This contribution presents the review of the main epitaxial SiC JFET concepts and analyzes their prospects for N-*off* performance based on simulations. The vertical JFET types discussed here are the lateral channel JFET (LCJFET) [1], the buried grid JFET (BGJFET) [2], and the dual gate vertical channel trench JFET (DGTJFET) [3]. Furthermore, the comparison of N-*off* and N-*on* SiC JFET designs of these selected epitaxial concepts in terms of blocking voltage, specific on-state resistance, current density, and switching performance trade-offs and limitations is done.

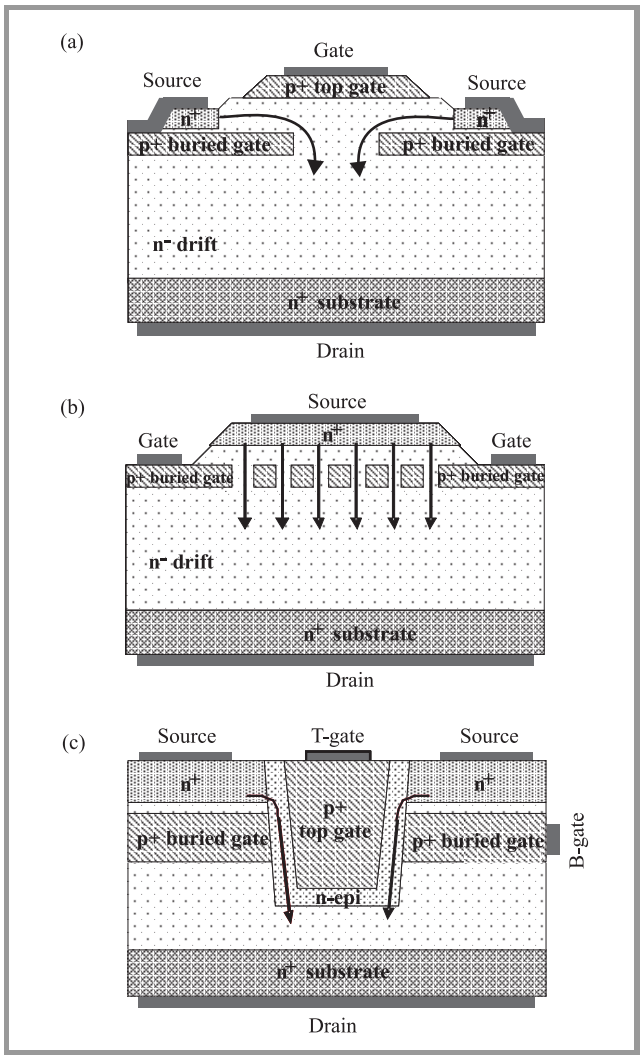


Fig. 2. Schematic drawings of the vertical epitaxial JFET concepts (a) lateral channel JFET, (b) buried grid JFET and (c) double gate vertical channel trench JFET.

The most successful JFET type in terms of voltage and current ratings has been the lateral channel JFET developed by SiCED [10]. A schematic drawing of the LCJFET design is shown in Fig. 2(a). The LCJFET allows optimal control of the channel parameters and offers the largest ease of fabrication compared to other concepts. It also offers the use of the inherent body diode as an anti-parallel diode in switching applications since the buried gate is preferably connected to source. This is necessary in order to reduce the Miller capacitance and thus maintain the high speed of operation as will be shown later in the paper.

The original LCJFET structure uses ion-implantation for the gate and the base region, and planar epitaxial growth for the defect-free channel layer. This leads to advantages in terms of ease of fabrication, freedom of parameter choice due to a wide design window, and small fabrication tolerances. The disadvantage is a relative large specific on-resistance, which is related to the large cell pitch due to the lateral configuration of the channel. In addition, the large cell pitch of 10 to 16 μm makes the use of both gates for the conduction control not feasible due to the prohibitively large gate charge required during switching. The concept is also characterized by relatively low saturation current levels and in order to achieve low on-state resistance, the demonstrated LCJFET designs are typically of N-*on* type.

As will be shown in this paper, the N-*off* design is not feasible with the LCJFET concept. The single gate drive with the buried gate connected to the source is necessary to mitigate the large Miller effect related to the large cell pitch that otherwise dominates the turn-off behavior. The large cell pitch and the single gate drive make the saturation current levels prohibitively low for any power switching application.

A schematic drawing of the BGJFET design is shown in Fig. 2(b). The main advantage of the vertical BGJFET concept is the small cell pitch that makes low specific on-state resistance and high saturation current densities possible. Furthermore, the inherent symmetric gate drive and the wide design window for the channel length, width, and doping make the N-*off* design feasible. The disadvantage is that optimization of the channel doping is not as easy as in the case of the lateral channel growth. Trenches have to be etched in the p-doped grid layer. These etched trenches must be epitaxially refilled to full extent. In the case of an implanted grid the possible use of higher doping in the channel is limited by the necessity to compensate the higher doped n-layer on top of the drift layer by the p-type grid implant. The channel doping in this concept is ultimately limited by the tolerances of the photolithography and trench etching process. Another disadvantage is that the use of the integral gate to drain body diode is not readily available with this concept.

A schematic drawing of the DGTJFET structure suggested by DENSO [3] is shown in Fig. 2(c). The DGTJFET offers high current rating capabilities for N-*off* mode operation. This design combines the advantages of the LCJFET and the BGJFET concepts by using epitaxial regrowth in trenches to define the pitch and the direction of the channel, transforming it from lateral to vertical. The epitaxial channel is grown on the vertical trench walls with the tolerances and the wide design window comparable to the LCJFET.

The DGTJFET is basically the same concept as the LCJFET, but allows a dramatic reduction of the cell pitch

and of the Miller capacitances due to the vertical channel. The low gate to drain capacitance makes fast switching possible even under dual gate driving conditions, while the small cell pitch and the dual gate control results in very low specific on-resistance. The dual gate drive and the wide design window for the channel optimization gives also exceptionally high saturation current levels for N-*off* designs. In addition, the negative temperature dependence of the saturation current is greatly reduced due to the possibility of using highly doped channels. It has thus the advantages of the BGJFET, but it also can surpass its performance due to the larger design window for the channel doping and width. The use of the integral gate to drain body p-n diode is possible in this concept. It is, however, a matter of trade-off with the possible saturation current density as will be shown later in this paper. The disadvantage of this concept is the complex process involving epitaxial regrowth in trenches and planarization techniques.

5. All-JFET Integral Cascodes

Also, the prospects of integral JFET/JFET cascodes are discussed. The integral cascode consisting of a high voltage (HV) N-*on* SiC power JFET and a control low voltage (LV) N-*off* JFET is a powerful concept for a N-*off* SiC switch [8]. The main advantage of the cascode solution is the greatly increased speed of switching due to the fact that the buried gate of the high voltage device, which is connected to the source (ground) of the cascode (source of the LV device), shields the low voltage device, which is driven by the control gate [11]. The gate to drain capacitance is thus reduced. In this way the Miller capacitance is being charged by the main circuit and not by the gate circuit.
Another advantage is the possibility of utilizing the built-in body p-n diode formed between the buried gate of the high voltage N-*on* device and the drain of the cascode as an anti-parallel diode in the switching applications. Two integral cascode concepts considered for analysis are shown in Fig 3. Both are based on a HV BGJFET controlled in first case by a LV N-*off* recessed gate JFET (RGJFET) [8] and in the second case by a LV N-*off* BGJFET. It is of interest to analyze the prospects of these integral cascode solutions for power applications. The hybrid cascode is difficult to optimize, which results in degraded on-state and switching performance [12]. In addition, the cascode configuration with a Si MOSFET compromises the high temperature capability of the SiC JFET [13].
The integral cascode concept allows the optimization of the cascode performance and achieves an on-state voltage comparable to the stand alone N-*on* JFET with equal voltage rating. This is due to several factors. First of all the LV N-*off* JFET can be made less N-*off* by shortening the channel. This is facilitated by the electric field shielding effect due to the buried gate of the HV JFET. The limit is set by the highest tolerated value for the leakage current. It is very important to have as high doping in the channel of the LV JFET as possible since the LV N-*off* JFET

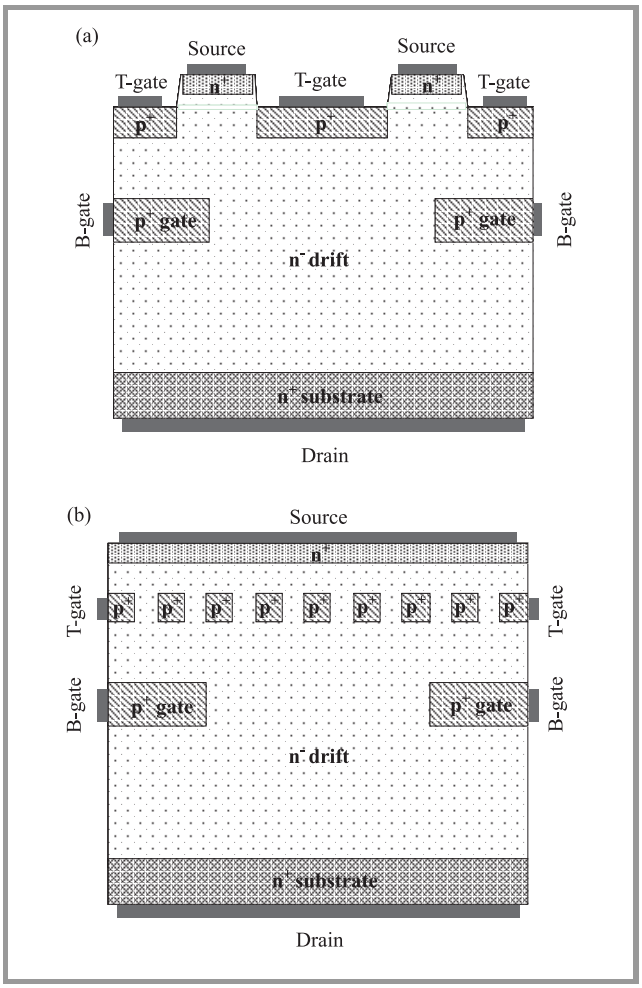


Fig. 3. Schematic drawings of the all-JFET integral cascode concepts (a) recessed gate JFET controlled cascode, (b) buried grid JFET controlled cascode.

determines the current throughput of the whole cascode. Secondly, the HV N-*on* JFET can be made more conductive by increasing the spacing of the buried gate grid. The limit is set by the electric field crowding at the edges of the buried grid when spacing becomes too large.
The grid of the N-*on* HV JFET section must support the full high voltage. This means the grid spacing has to be chosen so that the premature breakdown due to the enhanced electric field at the grid corners is avoided. As a result the cascode with output pentode characteristics may be controlled by a short channel JFET with triode characteristics. In this case the negative bias appearing on the buried gate of the HV JFET is beneficial in obtaining output characteristics with saturation at high current densities and with high value of the saturation current due to the very low on-state voltage of the optimized LV JFET. This will be further exemplified below using the concept from Fig. 3(a). It will be shown furthermore that the cascode optimization potential increases especially with increasing design voltage. This is due to the larger field shielding effect and wider grid spacing range available at lower doping concentrations of the drift region. The on-resistance values lower than those

of the N-*on* JFETs are feasible in the voltage range above 1000 V, as will be shown below.

6. N-*off* Design and High-Temperature Operation Considerations

The JFET is a unipolar device and as such should show a significant increase of the on-resistance with temperature. In the pure case of the resistivity being controlled by the drift region it should follow the relation of mobility degradation with temperature due to the phonon scattering [14].

When operating the JFET at higher junction temperatures one has also to consider the reduction of the built-in potential with temperature. The reduction of the built-in voltage V_{bi} with temperature is shown in Fig. 4, V_{bi} defines the limit of the unipolar operation for the JFET. A reduction of V_{bi} by 0.4 V is observed when increasing the temperature from room temperature to 250°C. For that reason all the values in this article have been calculated with the applied gate voltage of 2.4 V which includes also a 10% margin for the process tolerances.

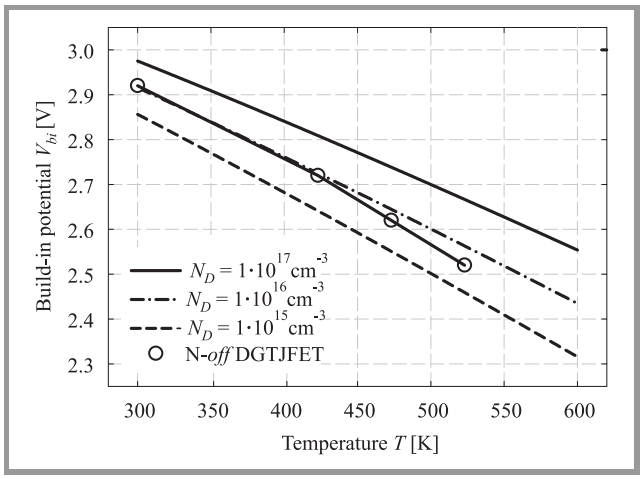


Fig. 4. Built-in potential as a function of the temperature calculated for different channel doping concentrations (see legend) and obtained from simulations (symbols) of the N-*off* DGTJFET.

In order to realize the N-*off* SiC JFET the channel of the device has to be fully depleted by the gate to source potential with no applied voltage. This means that the threshold voltage V_{th} has to be equal or higher than zero ($V_{th} \geq 0$). The potential at a p-n junction at zero applied voltage is equal to the so called built-in voltage V_{bi} being the function of the material band gap E_g and the acceptor and donor doping densities N_A and N_D at both sides of the junction (Eq. (1)):

$$V_{bi} = \frac{\mathrm{k} \cdot T}{q} \cdot \ln\left(\frac{N_A \cdot N_D}{N_V \cdot N_C}\right) + \frac{E_g}{q}. \tag{1}$$

A wide band gap material is characterized by a higher value of V_{bi}. For 4H-SiC V_{bi} is at least 2.5 V as compared to 0.6 V for Si. For JFETs, the highest gate voltage that can be applied in forward direction without entering the bipolar mode of operation is given by the built-in potential of the gate-source junction. The gate-source built-in voltage calculated using Eq. (1) is shown in Fig. 1 for the gate region doping of 10^{19}cm^{-3} and the channel doping of 10^{15}cm^{-3}, 10^{16}cm^{-3}, and 10^{17}cm^{-3}. For comparison the applied gate voltages, obtained from simulations of the N-*off* DGTJFET with a channel doping of $4 \cdot 10^{16}$cm^{-3}, at which a significant injection current in the channel is observed, are included in Fig. 4. A correction of $2\mathrm{k}T/q$ due to the majority carrier distribution tails has been subtracted from the calculated V_{bi} values [15]. The values of other parameters are after [14].

The channel doping and width have to be selected satisfying the following condition for the symmetrical gate configuration

$$V_{th} = V_{bi} - \frac{q \cdot N_D \cdot T_{ch}^2}{2 \cdot \varepsilon \cdot \varepsilon_0}, \tag{2}$$

where: V_{th} is the threshold voltage, N_D is the channel doping and T_{ch} is the half-width of the channel. The second term in Eq. (2) is the so called pinch-off voltage as obtained from the Poisson equation in the case of an abrupt asymmetrical junction.

In this case the gate doping concentration is much higher than that of the channel region. Partial derivation and normalization of Eq. (2) yields:

$$\frac{\Delta V_{th}}{V_{th}} = \frac{\Delta N_D}{N_D} + \frac{2 \cdot \Delta T_{ch}}{T_{ch}}, \tag{3}$$

where: ΔN_D and ΔT_{ch} are technological tolerances of channel doping and channel width.

Since the N-*off* operation requires $V_{th} \geq 0$, it is clearly seen from Eq. (3) that the current handling capability of the N-*off* device is by necessity derated due to process tolerances. A design with smaller doping and channel width compared to the one with maximized channel conductivity has to be used to realize a stable N-*off* device (see Eq. (4)).

In a similar way it can be shown that the choice of the highest possible channel doping is beneficial for compensating the resistivity degradation with temperature caused by phonon scattering. The channel conductivity is proportional to three temperature dependant parameters, the electron mobility μ_n, the electron concentration in the channel assumed to be equal to the ionized doping concentration N_D^+, and the active channel width $2(T_{ch} - w_n)$:

$$\sigma \sim \mu_n \cdot N_D^+ \cdot 2\left(T_{ch} - w_n\right). \tag{4}$$

Derivation and normalization of Eq. (4) gives:

$$\frac{\Delta \sigma}{\sigma_{RT}} = \frac{\Delta \mu_n}{\mu_{n,RT}} + \frac{\Delta N_D^+}{N_{D,RT}^+} - \frac{\Delta w_n}{T_{ch} - w_{n,RT}}, \tag{5}$$

where: σ_{RT}, $\mu_{n,RT}$, $N_{D,RT}$, $w_{n,RT}$ are the room temperature (27°C) values of the conductivity, the electron mobility, the donor density, and the space charge width, respec-

tively, $\Delta\sigma$, $\Delta\mu_n$, ΔN_D^+, Δw_n are the differences of the temperature dependent parameters with respect to their room temperature values.

The sensitivity of the channel resistivity to the listed parameters can now be evaluated using the following temperature dependencies:

$$\mu_n \sim T^{-2.15}, \tag{6a}$$

$$N_D^+ = N_D \cdot \left[1 - \frac{N_D}{N_c(T)} \cdot \exp\left(\frac{0.065}{\mathrm{k}T}\right)\right], \tag{6b}$$

and

$$w_n \sim \sqrt{\frac{V_{bi}(T) - V_G}{N_D}}. \tag{6c}$$

The temperature dependent parameters electron mobility $\mu_n(T)$, density of states of the conduction band $N_C(T)$, density of states of the valence band $N_V(T)$, band gap $E_g(T)$ and donor activation energy $E_d = 0.065$ eV are after [14] and $V_{bi}(T)$ is given by Eq. (1). Incomplete ionization applies in the channel region only and in the space charge region 100% ionization is assumed.

Equation (5) has been evaluated for the gate region doping of $10^{19}\mathrm{cm}^{-3}$ and the channel doping of $10^{15}\mathrm{cm}^{-3}$, $10^{16}\mathrm{cm}^{-3}$, and $10^{17}\mathrm{cm}^{-3}$ with $V_G = 2.4$ V. The relative change of the channel resistivity with temperature normalized to the room temperature value is shown in Fig. 5. The compensating effect of the high donor density becomes significant in lowering the temperature degradation of the channel resistance for donor densities above $10^{16}\mathrm{cm}^{-3}$. This is because the effect of incomplete ionization becomes more significant at high doping densities. The contribution of the last term in Eq. (5) can be neglected.

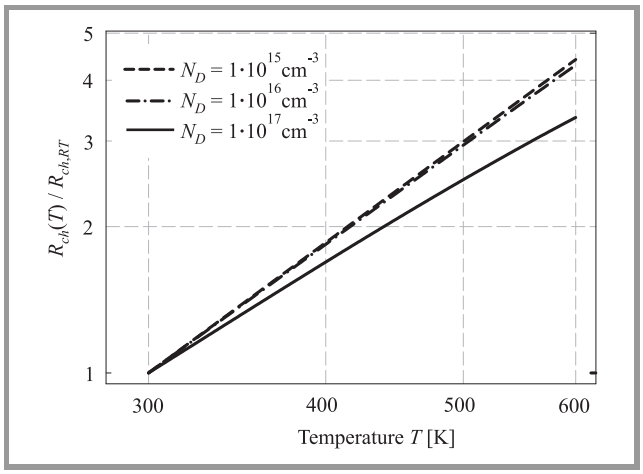


Fig. 5. Channel resistance $R_{ch}(T)$ normalized to the room temperature value $R_{ch,RT}$ as a function of the temperature calculated for different channel doping concentrations (see legend) using Eq. (5).

Low on-resistance and high output current density are two critical demands for a N-*off* design. Both require channel doping and width, and gate control voltage as high as possible. The maximum allowed control gate voltage value is however compromised by the maximum operating temperature of the device according to Eq. (1). Maximization of both the channel width and the channel doping is not possible with respect to the V_{th} condition (Eq. (2)). The optimization of the channel width and doping must be performed with respect to R_{on} and V_{th} as discussed later in this paper. At the same time the optimal choice of the doping and of the width of the channel is compromised by the actual process tolerances given by the selected technology according to Eqs. (2) and (3).

7. Simulation Study of N-*off* JFETs and All-JFET Cascodes

We have analyzed the potential for N-*off* operation of selected epitaxial vertical JFET concepts using simulations. The breakdown voltages, the specific on-state resistance, the maximum controllable current value at the applied drain voltages of 1.0 V and 10 V have been used as evaluation parameters in the temperature range from room temperature (27°C) to 250°C. The simulated structures are of both N-*on* and N-*off* type and cover the design voltage range from 600 V to 4500 V. When it comes to N-*off* behavior,

Table 1
Summary of design parameters of simulated N-*on* and N-*off* JFET and cascode structures with state of the art dimensions

Device type	B_V [V]	L_{ch} [μm]	$2T_{ch}$ [μm]	N_{ch} [cm^{-3}]	Cell pitch [μm]	N_D [cm^{-3}]	W_D [μm]
N-*off* JFETs							
DGTJFET	850	1.8	0.4	$4\cdot10^{16}$	3.6	$7.5\cdot10^{15}$	7.5
	1900	1.8	0.4	$4\cdot10^{16}$	3.6	$7.5\cdot10^{15}$	12
BGJFET	600	1.0	0.27	$4\cdot10^{16}$	2.69	$4\cdot10^{16}$	6
	1200	2.0	0.6	$1.5\cdot10^{16}$	3.0	$1.5\cdot10^{16}$	7.5
	2500	2.0	0.75	$3\cdot10^{15}$	3.15	$3\cdot10^{15}$	12.5
LCJFET1	750	1.0	0.6	$1.2\cdot10^{16}$	10	$4\cdot10^{16}$	7
10 μm	1350	1.0	0.6	$1.2\cdot10^{16}$	10	$1.5\cdot10^{16}$	7
pitch	3000	1.0	0.6	$1.2\cdot10^{16}$	10	$3\cdot10^{15}$	15
LCJFET2	750	2.0	0.6	$1.2\cdot10^{16}$	16	$4\cdot10^{16}$	7
16 μm	1350	2.0	0.6	$1.2\cdot10^{16}$	16	$1.5\cdot10^{16}$	7
pitch	3000	2.0	0.6	$1.2\cdot10^{16}$	16	$3\cdot10^{15}$	15
Cascodes							
RGJFET	all	0.35	0.35	$7\cdot10^{15}$	4.8	$7\cdot10^{15}$	2.4
BGJFET	550	0.6	2.4	$4\cdot10^{16}$	4.8	$4\cdot10^{16}$	6.4
	1250	0.6	2.4	$1.5\cdot10^{16}$	4.8	$1.5\cdot10^{16}$	11.4
	4200	0.6	2.4	$4\cdot10^{15}$	4.8	$4\cdot10^{15}$	31.4
N-*on* JFETs							
BGJFET	600	1.0	1.0	$4\cdot10^{16}$	4.0	$4\cdot10^{16}$	6
	1200	2.0	2.0	$1.5\cdot10^{16}$	5.0	$1.5\cdot10^{16}$	7.5
	2500	2.0	3.0	$3\cdot10^{15}$	5.5	$3\cdot10^{15}$	12.5
	4500	2.0	3.0	$2\cdot10^{15}$	6.0	$2\cdot10^{15}$	30

each JFET concept has its own limitations depending on the applied design and process technologies. First a number of idealized N-*off* BGJFET, DGTJFET, LCJFET and cascode structures with possibly wide and practically achievable channel dimensions have been designed and evaluated. The cascode structure is based on a HV BGJFET controlled by a short channel LV RGJFET (see Fig. 3(a)).

The design parameters of these structures are summarized in Table 1. Secondly the stand alone BGJFET and RGJFET structures are optimized by adjusting the channel doping separately from the drift region doping and by reducing the channel dimensions in the submicron region. The optimized stand alone JFET structures are compared to the corresponding cascode concept presented in Fig 3.

The optimization procedure is explained with reference to Fig. 6 showing the case of the N-*on* BGJFET with $V_{th} = -10$ V [16]. In general a lower channel doping density means that the potential barrier can be formed with a lower negative gate bias. This will however result in higher specific on-resistance for the structure. On the other hand too high channel doping results in reduced blocking voltage capability. This means that the optimum N_{ch} value for a given W_{ch} is the highest doping density giving full blocking voltage at specified threshold voltage, which can be seen in Fig. 6. The optimization of the integral cascodes, on the other hand, involves the selection of the largest possible spacing for the high voltage grid and of the shortest possible channel length for the low voltage JFET.

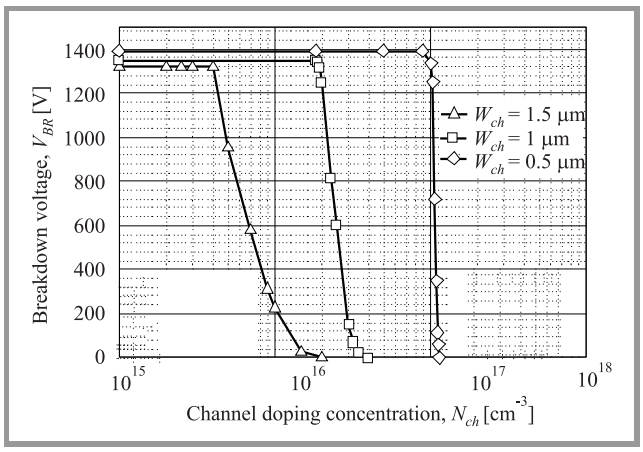


Fig. 6. Reverse blocking voltage, V_{BR} as a function of channel doping concentration, N_{ch} for N-*on* BGJFET with $V_{th} = -10$ V at 250°C.

In Fig. 7 the specific on-resistance is shown as a function of the channel length (a) for the 600 V stand alone RGJFET and RGJFET controlled cascode and (b) for the 600 V stand alone BGJFET and BGJFET controlled cascode for different channel widths. The calculations are done at 250°C and all the structures have the optimal channel doping as explained above.

The design parameters of this second set of structures are summarized in Table 2. All simulated structures satisfy the condition of the leakage current being well below 1 μA/cm^2 at zero applied gate voltage and 250°C.

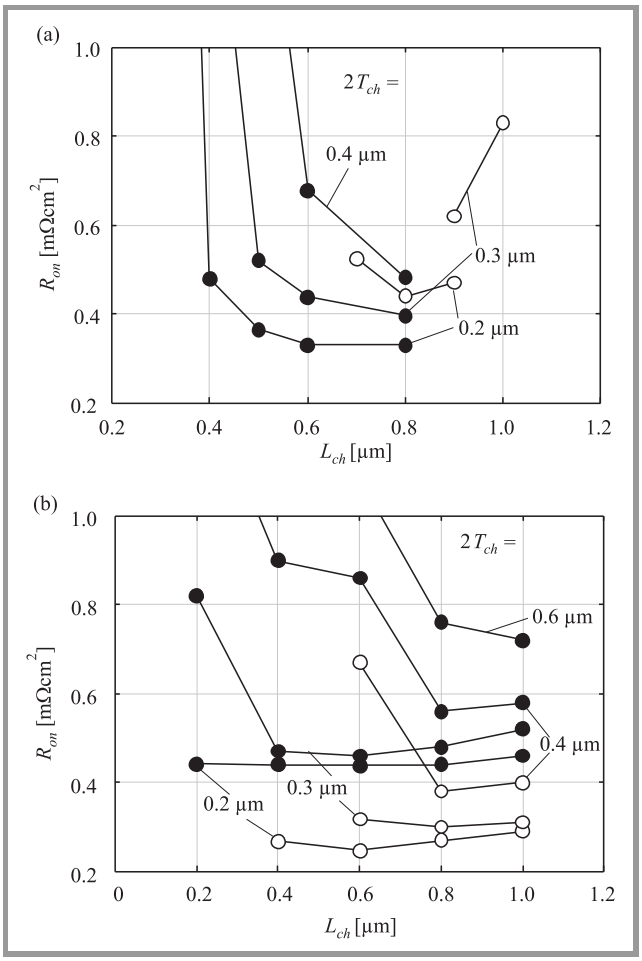


Fig. 7. Specific on-resistance for (a) the stand alone 600 V RGJFET (empty symbols) and RGJFET controlled cascode (filled symbols) and (b) the stand alone 600 V BGJFET (empty symbols) and BGJFET controlled cascode (filled symbols) as a function of channel length, L_{ch} at 25°C with channel width, $2T_{ch}$, as a parameter.

The specific on-resistance values for the state of the art structures are presented in Fig. 8 and for the submicron channel-length structures in Fig. 9.

The maximum controllable current density values are summarized in Tables 3 and 4, respectively. Only dual gate data are shown in Table 3 for LCJFETs, since the saturation current density values for all investigated LCJFET structures with 16 μm cell size and single gate drive are below 10 A/cm^2. The corresponding single gate drive current density values for the structures with 10 μm cell pitch are lower than 270 A/cm^2 and 150 A/cm^2 at 27°C and 250°C, respectively. These prohibitively low current density values make the single gate N-*off* LCJFETs not useful for power switching applications.

As can be seen in Fig. 8 the N-*off* designs have a weaker temperature dependence compared to the N-*on* designs. The on-state resistance of the N-*off* structures is to a large extent dominated by the channel resistance. The drift region resistance dominates in the high voltage N-*on* structures where the ideal phonon scattering related type of tem-

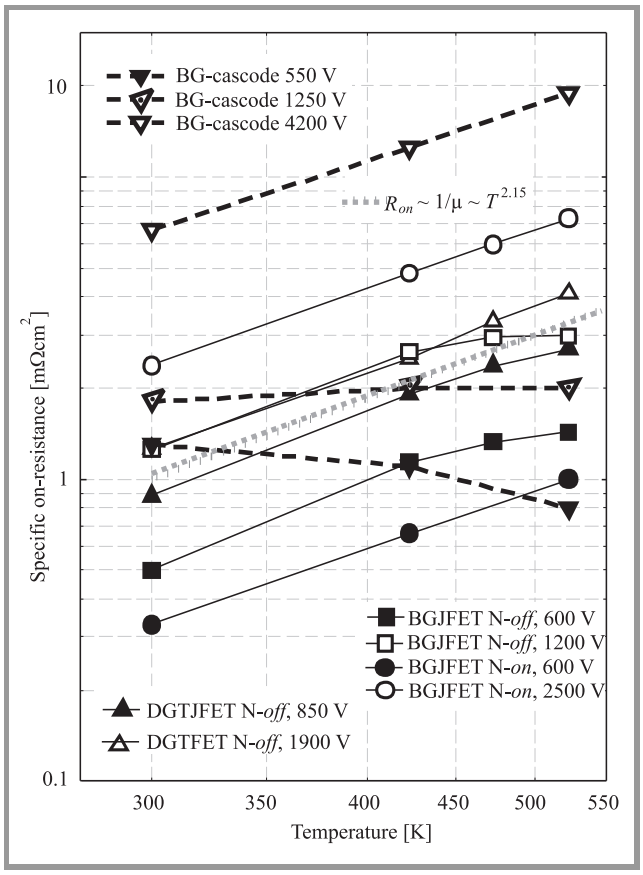


Fig. 8. Temperature dependence of the specific on-resistance for different JFET structures as described in Table 1. The on-resistance based on the phonon scattering limited carrier mobility is shown as dotted line.

Table 2
Summary of design parameters of optimized N-*off* JFET and cascode structures with submicron dimensions

Device type	B_V [V]	L_{ch} [μm]	$2T_{ch}$ [μm]	N_{ch} [cm^{-3}]	Cell pitch [μm]	N_D [cm^{-3}]	W_D [μm]
N-*off* JFETs							
RGJFET	600	0.8	0.2	$9 \cdot 10^{16}$	2.4	$4 \cdot 10^{16}$	7.0
	1200	0.8	0.2	$9 \cdot 10^{16}$	2.4	$1.5 \cdot 10^{16}$	10.0
	3000	0.8	0.2	$9 \cdot 10^{16}$	2.4	$3 \cdot 10^{15}$	15.0
BGJFET	600	0.6	0.2	$1.5 \cdot 10^{17}$	3.6	$4 \cdot 10^{16}$	7.0
	1200	0.6	0.2	$1.5 \cdot 10^{17}$	3.6	$1.5 \cdot 10^{16}$	10.0
	3000	0.6	0.2	$1.5 \cdot 10^{17}$	3.6	$3 \cdot 10^{15}$	15.0
Cascodes							
RGJFET	all	0.6	0.2	$9 \cdot 10^{16}$	2.4	$9 \cdot 10^{16}$	1.4
BGJFET	600	1.0	1.4	$4 \cdot 10^{16}$	2.4	$4 \cdot 10^{16}$	7.0
	1200	1.0	2.0	$1.5 \cdot 10^{16}$	3.0	$1.5 \cdot 10^{16}$	10.0
	3000	1.0	2.8	$3 \cdot 10^{15}$	3.8	$3 \cdot 10^{15}$	15.0
RGJFET	all	0.4	0.2	$1.6 \cdot 10^{17}$	3.6	$1.6 \cdot 10^{17}$	1.0
BGJFET	600	1.0	1.4	$4 \cdot 10^{16}$	3.6	$4 \cdot 10^{16}$	7.0
	1200	1.0	2.0	$1.5 \cdot 10^{16}$	3.6	$1.5 \cdot 10^{16}$	10.0
	3000	1.0	2.8	$3 \cdot 10^{15}$	3.6	$3 \cdot 10^{15}$	15.0

perature dependence is observed. The contribution of the highly doped substrate is not included in the data of Figs. 8 and 9. The substrate will dominate at lower voltage levels and reduce the temperature dependence due to the ionisation of dopants in the same way as demonstrated for high channel doping in Fig. 5. It is interesting to note that the simulated cascode structures show a negative temperature dependence of the on-resistance up to the design voltage of about 1200 V. This behavior is related to the potential barrier present in the case of short and relatively low doped channel in recessed gate JFET.

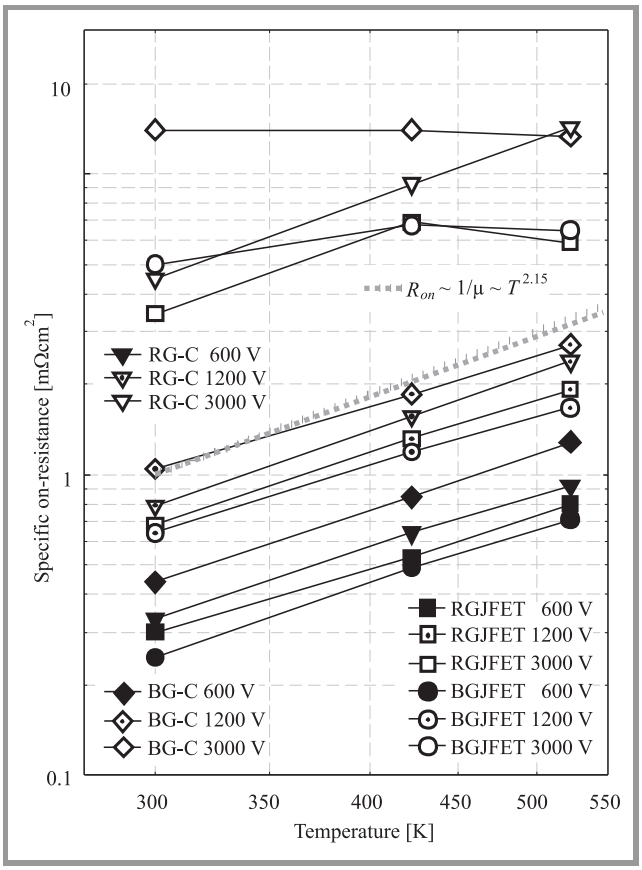


Fig. 9. Temperature dependence of the specific on-resistance for different JFET structures as described in Table 2. The on-resistance based on the phonon scattering limited carrier mobility is shown as dotted line.

The current flow in the presence of such a potential barrier is strongly temperature dependent and has a positive temperature coefficient thus compensating the resistivity increase due to the phonon scattering mechanism. Temperature dependence of the current flow over the 2D potential barrier is similar to that of the current flow through a p-n junction. The reason for the change in behavior with the increasing design voltage is the competition between the negative temperature dependence of the on-resistance due to the lowering of the potential barrier present in the channel of the recessed gate LV JFET and the positive temperature dependence due to the mobility degradation in the drift region.

Table 3
The output current densities of simulated N-*on* and N-*off* JFET and cascode structures with state of the art dimensions at drain voltages of 1 V and 10 V for different temperatures

Device type	Gate drive V_{GS} (2.4 V)	B_V [V]	27°C		150°C		250°C	
			J_{DS} $V_{DS}=1$ V [A/cm^2]	J_{DS} $V_{DS}=10$ V [A/cm^2]	J_{DS} $V_{DS}=1$ V [A/cm^2]	J_{DS} $V_{DS}=10$ V [A/cm^2]	J_{DS} $V_{DS}=1$ V [A/cm^2]	J_{DS} $V_{DS}=10$ V [A/cm^2]
N-*off* JFETs								
DGTJFET	DG	850	1000	2600	1000	2600	350	1000
	DG	1900	760	2600	500	2600	250	980
BGJFET	SG	600	1330	2000	830	1400	500	800
		1200	625	1100	430	750	230	380
		2500	200	285	90	150	60	190
LCJFET	DG	750	210/70	460/80	130/44	220/60	120/44	190/60
$10/16\,\mu$m		1350	190/60	270/70	120/40	190/50	110/40	170/50
pitch		3000	110/50	230/70	60/30	160/50	50/30	150/50
Cascode	SG	550	450	2000	650	2200	800	2400
JFET		1250	390	1800	440	1950	500	2000
		4200	150	1000	80	750	60	650
N-*on* JFETs								
BGJFET	SG	600	1000	1300	600	950	490	800
		1200	1200	9000	600	4500	400	3000
		2500	420	1000	200	1600	140	3200
		4500	90	700	40	350	30	250

Table 4
The output current densities of optimized N-*off* JFET and cascode structures with submicron dimensions at drain voltages of 1 V and 10 V for different temperatures

Device type	Gate drive V_{GS} (2.4 V)	B_V [V]	27°C		150°C		250°C	
			J_{DS} $V_{DS}=1$ V [A/cm^2]	J_{DS} $V_{DS}=10$ V [A/cm^2]	J_{DS} $V_{DS}=1$ V [A/cm^2]	J_{DS} $V_{DS}=10$ V [A/cm^2]	J_{DS} $V_{DS}=1$ V [A/cm^2]	J_{DS} $V_{DS}=10$ V [A/cm^2]
N-*off* JFETs								
RGJFET	SG	600	2600	4900	1600	3900	1200	3400
		1200	1380	3700	730	2900	600	2500
		3000	290	2400	145	1300	110	900
BGJFET	SG	600	3200	7700	1900	5700	1300	4700
		1200	1500	7000	800	4900	550	3900
		3000	210	2300	145	1300	125	910
Cascodes								
RGJFET/	SG	600	2650	7400	1500	5600	1000	4250
BGJFET		1200	1200	5500	6250	4000	410	3000
		3000	220	1750	105	920	75	600
BGJFET/	SG	600	2100	8200	1120	5600	760	4400
BGJFET		1200	880	5300	510	3500	360	2500
		3000	90	630	90	620	70	520

The drift region mobility degradation dominates for voltage designs above 1200 V while the channel barrier lowering dominates at lower design voltages. This is further illustrated by the output characteristics shown in Fig. 10.

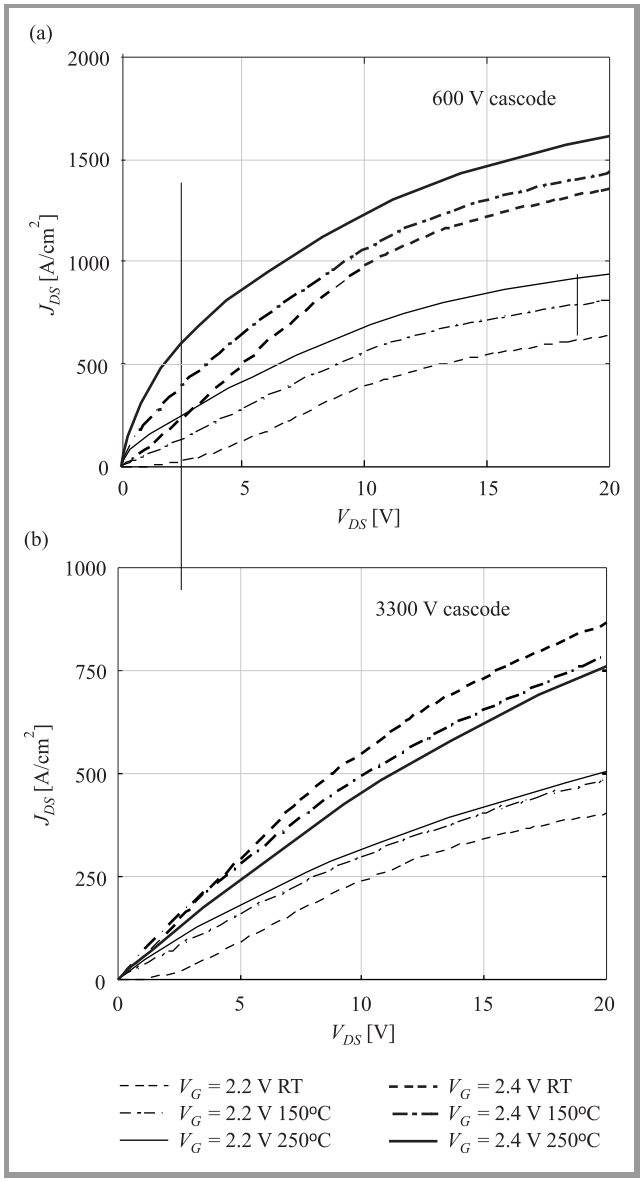


Fig. 10. Output characteristics of (a) 600 V and (b) 3.3 kV integral cascodes based on the high voltage BGJFET and controlled by low voltage RGJFET.

It can be seen that the cascode devices display a triode like type of the current voltage behavior at lower current densities, which begins to resemble pentode like output at higher current densities. The tendency towards the triode like characteristic is also more pronounced at lower temperatures and the transition to the pentode like characteristics is promoted by increased temperature. This behavior is consistent with the existence of the potential barrier in the channel of the LV RGJFET substructure. The transition to the pentode behavior is due to the biasing of the gate of the HV JFET by on-state voltage generated in the upper part of the structure.

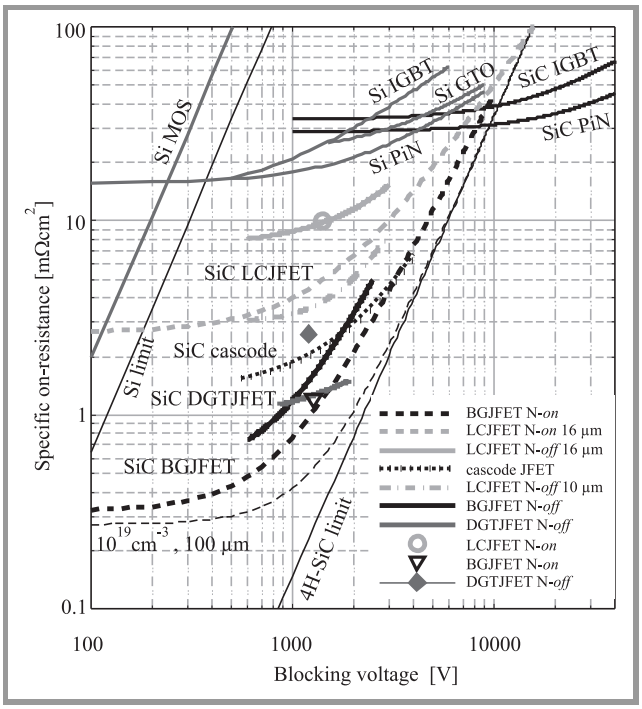


Fig. 11. Simulated and experimental (symbols) specific on-resistance versus blocking voltage for various N-*on* and N-*off* JFET and cascode structures with state of the art dimensions.

In Fig. 11 the specific on-resistance values for state of the art structures including contribution of the thinned 100 μm thick substrate are shown versus blocking voltage together with best published experimental data for LCJFET [13],

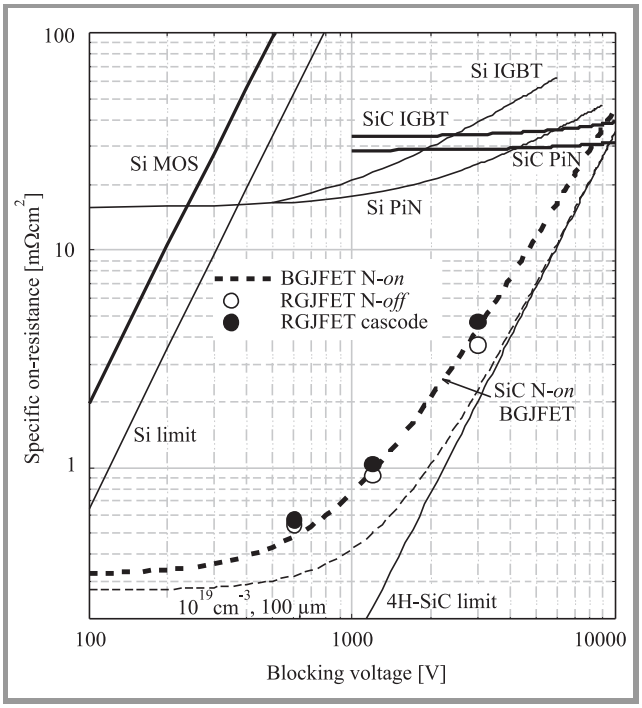


Fig. 12. Simulated specific on-resistance versus blocking voltage for stand-alone N-*off* RGJFET and RGJFET controlled cascode structures with submicron dimensions.

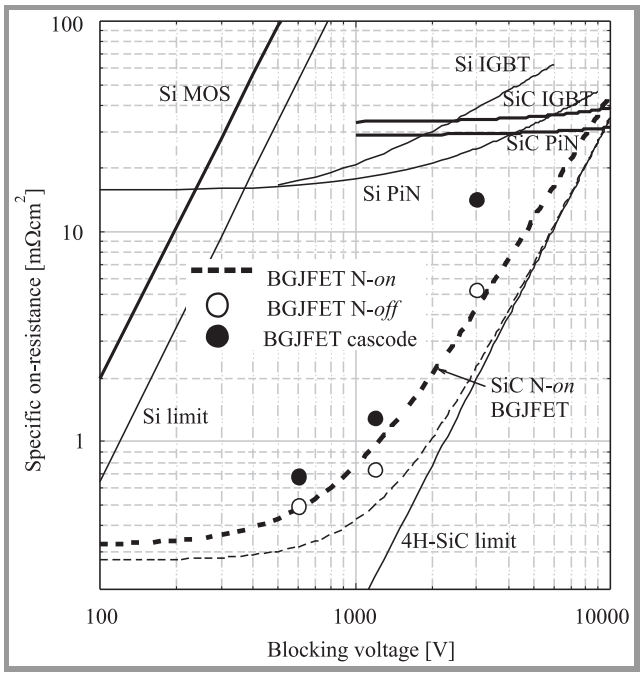


Fig. 13. Simulated specific on-resistance versus blocking voltage for stand-alone N-*off* BGJFET and BGJFET controlled cascode structures with submicron dimensions.

BGJFET [17], and DGTJFET [18] and theoretical curves for N-*on* LCJFET and BGJFET structures with threshold voltage of -50 V [5]. Finally, in Figs. 12 and 13 the specific on-resistance values for optimized N-*off* RGJFET and RGJFET controlled cascode and N-*off* BGJFET and BGJFET controlled cascode are shown versus blocking voltage. It is demonstrated that on-resistance values lower than those for the N-*on* BGJFET with $V_{th} = -50$ V are feasible for optimized N-*off* stand alone RGJFET and BGJFET structures. It can also be seen that on-resistance values comparable to those for the N-*on* BGJFET with $V_{th} = -50$ V are feasible for optimized integral cascodes of both investigated types especially in the voltage range above 1.0 kV.

8. N-*off* Design and Switching Considerations

The JFET concepts containing both the buried gate and the top gate have the possibility of single gate or double gate operation. In the first case only one gate is utilized for device control while the other is connected to source (ground). In the second case both gates are connected to the gate unit and used in parallel. In the case when the buried gate is connected to the source the devices have the ability to utilize the internal body diode removing the necessity of an external anti-parallel diode in many inverter and converter applications. This capacity is also inherent to the cascode concept [8].

Connecting the buried gate to the source makes switching much faster and reduces both the charge supplied by the gate unit and turn-off losses since the charge necessary to charge the Miller capacitance is supplied by the main circuit and not by the gate drive unit. The effect can be understood as a buried grid shielding of the top gate contact so that the Miller capacitance seen by the gate unit is greatly reduced.

The comparison of the turn-off switching characteristics of the single gate and the dual gate switching in the case of the N-*on* LCJFET structure is shown in Fig. 14. The gate charge Q_g and the turn-off losses E_{off} are $3.3 \cdot 10^{-6}$ C and $8.3 \cdot 10^{-2}$ J for the top gate control and $2.1 \cdot 10^{-7}$ C and $3.5 \cdot 10^{-3}$ J for the double gate control case, respectively. The driving conditions are the same. The conclusion from Fig. 14 is that the N-*off* LCJFET will necessarily suffer from slow switching speed since it requires dual gate control in order to pass reasonable forward currents as can be seen in Table 3.

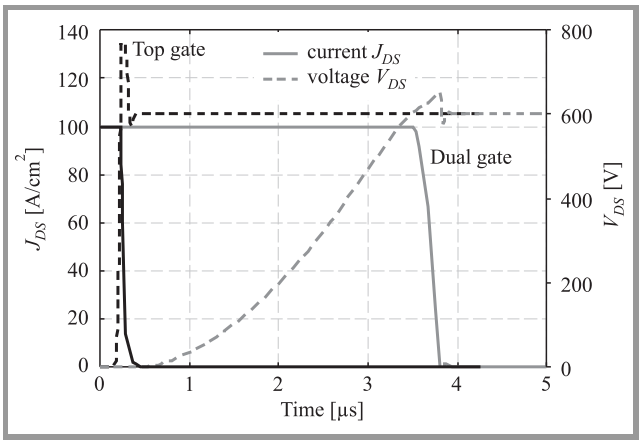


Fig. 14. A comparison of the top gate and double gate switching characteristics of the N-*on* LCJFET structure with $V_{th} = -50$ V and 16 μm cell pitch. Turn-off in inductive circuit with $R_G = 50\ \Omega$.

In Fig. 15 the same comparison is done for the N-*off* DGTJFET structure and N-*off* LCJFET structure with cell pitch of 10 μm. The channel length is 1.0 μm in both cases. The gate charge Q_g and the turn-off losses E_{off} are $1.6 \cdot 10^{-6}$ C and $7.5 \cdot 10^{-3}$ J for the DGTJFET with buried gate control, $1.2 \cdot 10^{-6}$ C and $1.3 \cdot 10^{-2}$ J for the DGTJFET with top gate control, $2.5 \cdot 10^{6}$ C and $2.2 \cdot 10^{-2}$ J for the DGTJFET with buried and top gate control, and $3.3 \cdot 10^{-6}$ C and $8.3 \cdot 10^{-2}$ J for the N-*off* LCJFET with dual gate control under the same driving conditions. It shows that the sacrifice of the switching speed is much less severe in the case of the DGTJFET structure due to the much smaller cell pitch and thus the smaller Miller capacitance attributed to both the buried and top gates.

The turn-on of N-*off* JFET devices tends to be slow depending on the very low voltage swing between the threshold voltage and the maximum allowed gate voltage given by the V_{bi} available for charging the gate. Due to the low charging voltage the channel resistance plays a crucial role in controling the speed of the turn-on process as well as the RC constant of the device. Based on numerical simulations, the increase of the channel doping in the range

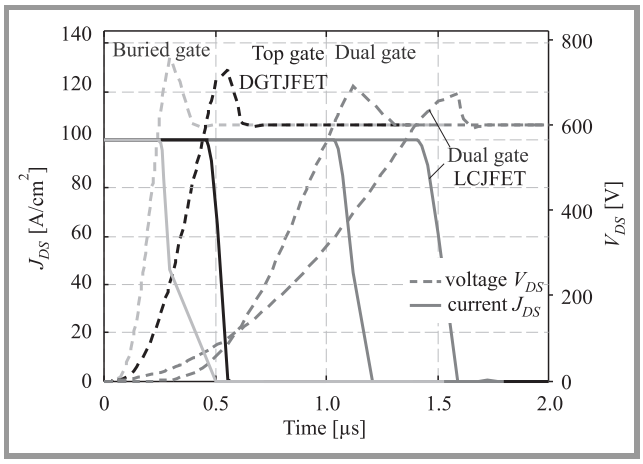


Fig. 15. A comparison of the switching characteristics of the N-*off* DGTJFET using the buried gate, the top gate and both gates with a N-*off* LCJFET with 10 μm cell pitch and double gate control. Turn-off in inductive circuit with $R_G = 2\ \Omega$.

$1 \cdot 10^{16}\,\mathrm{cm}^{-3}$ to $1 \cdot 10^{17}\,\mathrm{cm}^{-3}$ reduces the turn-on time (and turn-on losses) during inductive switching of the DGTJFET by one order of magnitude [18]. The effect of the channel doping on the top gate capacitance and turn-off switching is opposite, however the influence of the increased gate capacitance due to the increased channel doping on the turn-off time and turn-off losses is much smaller [19]. The requirement of maximizing the channel doping for the increased turn-on speed of the N-*off* device coincides with the requirements for the improved high temperature operation as discussed earlier.

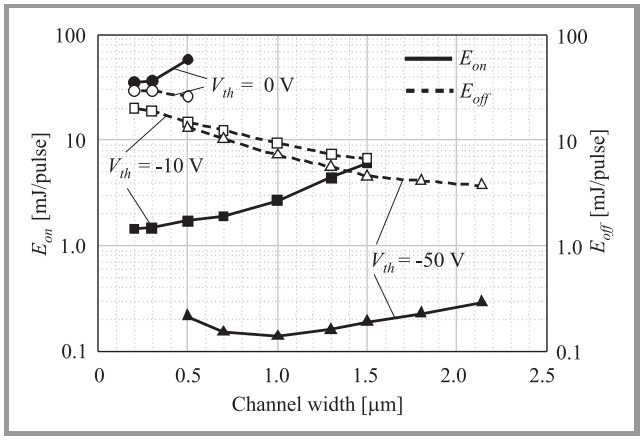


Fig. 16. Turn-on and turn-off energy for N-*on* and N-*off* 1.2 kV BGJFET structures with $I_{DS} = 100\ \mathrm{A/cm}^2$, $V_{DS} = 600$ V and $R_G = 1\ \Omega$ as a function of the channel width at 250°C.

The example of switching energy dependence on the device design is given in Fig. 16. The turn-on and turn-off energy is shown for 1.2 kV N-*on* BGJFET designs with threshold voltage values of $V_{th} = -50$ V and -10 V and for N-*off* BGJFET design ($V_{th} = 0$ V) as a function of channel width at switching conditions 100 A/cm^2, 600 V with $R_G = 1\ \Omega$ at 250°C [16]. The devices have a channel length of 1.6 μm. Switching properties and switching losses E_{on} and E_{off} are related to channel doping concentration, N_{ch} and channel width, W_{ch} as discussed above. In addition, with conventional gate drive, the charging time of JFET capacitances depends strongly on the available gate driving voltage which is related to the V_{th} value. Because of that the N-*on* BGJFET devices will have significantly lower turn-on and turn-off losses compared to the N-*off* design. The difference in the turn-on losses is especially large and more than two orders of magnitude between the N-*on* device with $V_{th} = -50$ V and N-*off* device. The difference in turn-off losses is at the same time about a factor of two.

9. Summary and Conclusions

Prospects of N-*off* SiC JFET switch are studied by simulation. Several possible epitaxial switch designs are reviewed and compared. The influence of the device design on the conduction and switching performance is investigated in the wide range of N-*on* to N-*off* designs with the threshold voltage values from -50 V to 0 V. The advantages of the epitaxial JFET designs for high voltage high temperature operation in the voltage and temperature range of 0.6 kV to 3.0 kV and 25°C to 250°C, respectively, are demonstrated.

The relative merits and limitations of LCJFET, BGJFET and DGTJFET concepts are clearly demonstrated. The stand alone RGJFET and BGJFET concepts are compared to the integral cascode solutions. It is shown that integral cascodes can be optimized to be competitive with and superior to stand-alone switches. It is furthermore demonstrated that the utilization of the N-*off* JFET and JFET cascode switch requires development of efficient gate driving methods to overcome the limitation of slow turn-on.

References

[1] P. Friedrichs, H. Mitlehner, K. O. Dohnke, D. Peters, R. Schörner, U. Weinert, E. Baudelot, and D. Stephani, "SiC power devices with low on-resistance for fast switching applications", in *Proc. 12th Int. Symp. Pow. Semicond. Dev. ICs*, Toulouse, France, 2000, p. 213.

[2] Y. Tanaka, M. Okamotu, A. Takatsuka, K. Arai, T. Yatsuo, K. Yano, and M. Kasuga,"700 V 1.0 m$\Omega \cdot$cm^2 buried gate SiC-SIT (SiC-BGSIT)", *IEEE Electron Dev. Lett.*, vol. 27, no. 11, pp. 908–910, 2006.

[3] R. K. Malhan, Y. Takeuchi, M. Kataoka, A.-P. Mihaila, S. J. Rashid, F. Udrea, and G. A. J. Amaratunga, "Normally-off trench JFET technology in 4H silicon carbide", *Microelectron. Eng.*, vol. 83, iss. 1, pp. 107–110, 2006.

[4] S. Krishnaswami, A. Agarwal, S. H. Ryu, C. Capell, J. Richmond, J. Palmour, S. Balachandran, T. P. Chow, S. Bayne, B. Gail, K. Jones, and C. Scozzie, "1000 V, 30 A 4H-SiC BJTs with high current gain", *IEEE Electron Dev. Lett.*, vol 26, no. 3, pp. 175–177, 2005.

[5] M. Bakowski, "Status and prospects of SiC power devices", *IEEE Trans. Ind. Appl.*, vol. 126, no. 4, pp. 391–399, 2006.

[6] R. K. Malhan, H. Nakamura, S. Onda, D. Nakamura, and K. Hara, "Impact of SiC structural defects on the degradation phenomenon of bipolar SiC devices", *Mater. Sci. Forum*, vol. 433–436, pp. 917–920, 2003.

[7] B. Ållebrand and H.-P. Nee, "On the possibility to use SiC JFETs in power electronic circuits", in *Proc. 9th Conf. Pow. Electron. Appl., EPE'2001*, Graz, Austria, 2001.

[8] M. Bakowski and U. Gustafsson, "Unipolar and bipolar SiC integral cascoded switches with MOS and junction gate – simulation study", *Mater. Sci. Forum*, vol. 389–393, pp. 1321–1324, 2002.

[9] M. L. Heldwein and J. W. Kolar, "A silicon carbide JFET gate driver circuit allowing short commutation times for sparse matrix converter applications", in *Proc. Nineteenth Ann. IEEE Appl. Pow. Electron. Conf. Expos.*, Anaheim, USA, 2004, vol. 1, pp. 116–121.

[10] P. Friedrichs, H. Mitlehner, K. W. Bartsch, O. Dohnke, R. Kattschmidt, U. Weinert, B. Weis, and D. Stephani, "Static and dynamic characteristic of 4H-SiC JFETs designed for different blocking categories", *Mater. Sci. Forum*, vol. 338–342, pp. 1243–1246, 2000.

[11] M. Bakowski, "Analysis of unipolar and bipolar SiC cascoded switches with MOS gate", *Mater. Sci. Forum*, vol. 433–436, pp. 801–804, 2003.

[12] V. Veliadis, T. McNutt, M. Snook, H. Hearne, P. Potyraj, J. Junghans, and C. Scozzie, "Large area silicon carbide vertical JFETs for 1200 V cascode switch operation", *Int. J. Pow. Manag. Electron.*, vol. 2008, art. id. 523721, 8 p., 2008.

[13] D. Stephani and P. Friedrichs, "Silicon carbide junction field effect transistors", *Int. J. High Speed Electron. Syst.*, vol. 16, no. 3, pp. 825–854, 2006.

[14] M. Bakowski, U. Gustafsson, and U. Lindefelt, "Simulation of SiC high power devices", *Phys. Stat. Sol. A*, vol. 162, pp. 421–440, 1997.

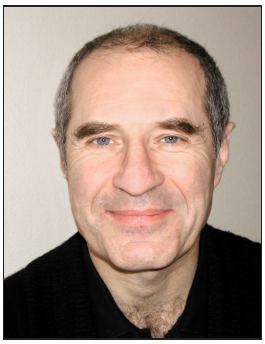
[15] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1981.

[16] J. K. Lim and M. Bakowski, "Analysis of 1.2 kV SiC buried grid VJFETs" (to be published in *Phys. Scripta T*, 2009).

[17] Y. Tanaka, K. Yano, M. Okamoto, A. Takatsuka, K. Arai, and T. Yatsuo, "1270 V, 1.21 mΩcm^2 SiC buried gate static induction transistors (SiC-BGSITs)", *Mater. Sci. Forum*, vol. 600–603, pp. 1071–1074, 2009.

[18] R. K. Malhan, M. Bakowski, Y. Takeuchi, N. Sugiyama, and A. Schöner, "Design, process, and performance of all-epitaxial normally-off SiC JFETs", *Phys. Stat. Sol. A*, vol. 206, iss. 10, pp. 2308–2328, 2009.

[19] R. K. Malhan, S. J. Rashid, M. Kataoka, Y. Takeuchi, N. Sugiyama, F. Udrea, G. A. J. Amaratunga, and T. Reimann, "Switching performance of epitraxially grown normally-off 4H-SiC JFET", *Mater. Sci. Forum*, vol. 600–603, pp. 1067–1070, 2009.



Mietek Bakowski was born in Bydgoszcz, Poland, in 1946. He completed M.Sc. studies at the Faculty of Electronics, Warsaw University of Technology, in 1969. He received his Ph.D. and the Assistant Professor competence from the Chalmers University of Technology, Gothenburg, Sweden, in 1974 and in 1981, respectively, and works presently as a senior expert at the Acreo AB, Kista, Sweden. He has worked with the development of silicon bipolar and BiMOS power devices and since 1994 with the design, simulation and electrical evaluation of SiC power devices. In 2000–2003 he has been appointed Adjunct Professor at the Royal Institute of Technology, KTH, Kista.
e-mail: mietek.bakowski@acreo.se
Acreo AB
Electrum 236
SE-164 40 Kista, Sweden