Paper

# The influence of yield model parameters on the probability of defect occurrence

Michał Rakowski and Witold A. Pleskacz

**Abstract—This paper describes the analysis of the influence of yield loss model parameters on the calculation of the probability of arising shorts between conducting paths in IC's. The characterization of the standard cell in AMS 0.8 $\mu$m CMOS technology is presented as well as obtained probability results and estimations of yield loss by changing values of model parameters.**

***Keywords—yield model parameters, spot defect, probability of defect occurrence, critical area.***

## 1. Introduction

Contemporary digital circuits become more complex making their testing and diagnostics more difficult. Having an accurate defect model is therefore essential. Since the model affects the efficiency of defect detection, it should be tuned as well as possible to reflect the reality. On the other hand, however, excessive complication of the model could result in many practical difficulties. The time of running the defect detection procedure should be acceptable, especially for large VLSI circuits.

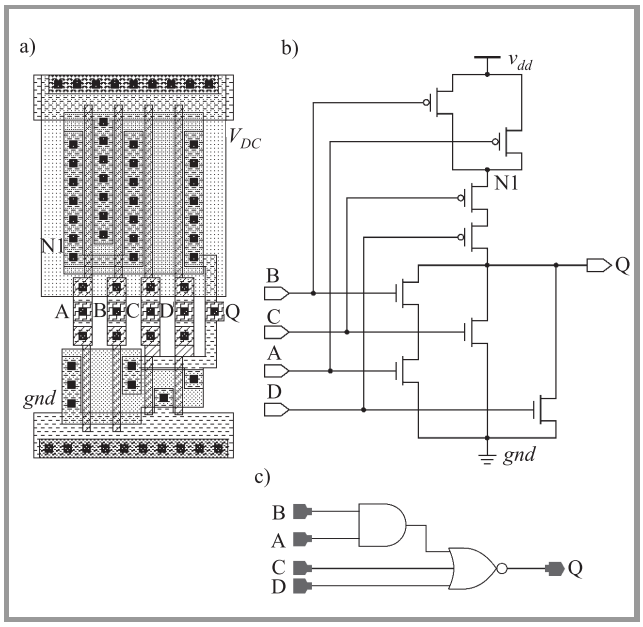


***Fig. 1.*** The AN3 complex gate: (a) the layout; (b) schematic diagram; (c) logic diagram.

Spot defects in ICs still cause many functional and catastrophic faults [1–3]. The degree of the influence of spot defects, such as shorts or opens, on IC manufacturability is determined by the sensitivity of the layout to these defects. It is believed that only full layout analysis enables one to proceed with complex estimation of defect-occurrence probabilities and yield calculations [4].

In this work we use a quite efficient and easy-to-implement model of critical area that enables the probability of different catastrophic faults caused by spot defects to be estimated. The model is used to calculate the probability of shorts and opens between two conductive paths on a circuit layout, as well as to estimate yield.

The analysis of the model parameters is limited in this paper only to the defects cause by shorts. A standard AN3 complex gate from 0.8 $\mu$m CMOS industrial library (see Fig. 1) has been used as a testing circuit.

## 2. Probabilistic yield model

A short is a piece of extra conducting material that connects a pair of separate conducting regions in the integrated circuit. This affects the connectivity of the circuit: two separate electrical nets become connected. It is intuitively obvious that probabilities of shorts depend on the layout of the circuit. Conducting regions that are adjacent to one another are more susceptible to shorts than regions that are separated by a large distance. We assume that every defect that results in a short can be approximated by a circle. To estimate the probabilities of shorts between pairs of nodes we use the concept of critical area for shorts [3]. The critical area for shorts is such a region in the circuit that, if the center of a defect of a given radius $R$ is located anywhere inside the critical area, a short between two adjacent conducting paths occurs (see Fig. 2).

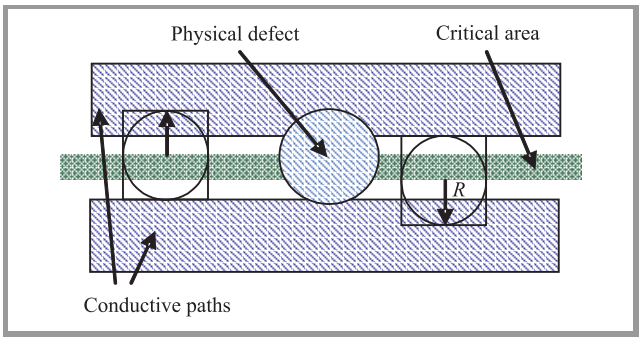


***Fig. 2.*** The concept of critical area.

The probability that two electrical nodes will be shorted by a physical defect is given by the following formula derived from Poisson-based yield model:

$$Y = \prod_{i=1}^{N} Y_i;\ Y_i = \exp\Big[ - \int_0^{+\infty} Acr_i(r) \cdot D_i(r)\, dr \Big], \qquad (1)$$

where: $Y$ – defect-related yield for an IC, $N$ – number of defect types, $Y_i$ – defect-related yield for defect type "i", $r$ – defect radius random variable, $Acr_i(r)$ – critical area function, $D_i(r)$ – defect size distribution.

The defect size distribution can be calculated from the formula [2, 3]:

$$D_i(r) = D_{oi}(r) \cdot f_{ri}(r), \qquad (2)$$

where: $D_{oi}(r)$ – density of spot defect of type "i", $f_{ri}(r)$ – size distribution function for defect of type "i" given by [2, 3]:

$$f_{ri}(r) = \begin{cases} \dfrac{2(p_i - 1)\, r}{(p_i + 1) X_{oi}^2} & \text{for} \quad 0 < r \le X_{oi}, \\ \dfrac{2(p_i - 1) X_{oi}^{p_i - 1}}{(p_i + 1) r^{p_i}} & \text{for} \quad X_{oi} < r \end{cases}. \qquad (3)$$

The size distribution function has two parameters: $X_{oi}$ (which is modeled to be very small compared to the minimum feature size of a given manufacturing process) and parameter $p_i$. In our calculation of the probability of shorts the most important three conductive layers – polysilicon, metal1 and metal2 were taken into account.

Parameter $D_{oi}$ is the density of physical defects and $p_i$ and $X_{oi}$ are model parameters. $P_i$ is set to 3, $X_{oi}$ to 20% of the minimum distance between the shapes of a given conducting layer, and $D_o$ to 10 defects/cm$^2$ [3, 4].

## 3. Experimental results

The analysis of parameter influence on manufacturing yield as well as probability of shorts between conducting paths was perfomed by means of variation of each parameter within a predefined range. The analyzed range of the variation of the examined parameters is compared to the corresponding nominal values in Table 1.

Table 1
Analyzed range of variation of the yield model parameters

| Description | Layers | Parameters | | | |
|---|---|---|---|---|---|
| | | $p$ | $D_o$ [cm$^{-2}$] | $X_o$ [%] | |
| Nominal value | Poly1 | 3 | 10 | 20 | 0.2 |
| | Met1 | | | | 0.2 |
| | Met2 | | | | 0.24 |
| Range of changes | All | $<2-5>$ | $<5-15>$ | $<5-40>$ | |
| Step | All | 0.5 | 2.5 | 5 | |

The probability analysis was performed using the extracted layout of AN3 complex gate resulted in a list of faults for shorts with non-zero probability. To extract critical areas and calculate the probability of shorts we used our tool [5] *Critical Areas* written in the SKILL language. By running geometrical operations on the conducting layers of the layout the tool extracts the critical area function $Acr_i(r)$, which is further used to carry out the probability calculation and yield estimation.

We calculated the probability of shorts between all possible pairs of two electrical nodes for complex gate AN3 (see Table 2). The obtained calculations were taken as the basis for further analysis of model parameters.

Table 2
Distribution of probabilities of faults for AN3 gate

| AN3 | | $Y$ | $P_{sh} = 1 - Y$ | $P_{sh}/P_{sh}(sum)$ |
|---|---|---|---|---|
| Conductive layers | | 0.999998718 | $1.28 \cdot 10^{-6}$ | |
| For all pair of nets | | | | |
| No. | Fault | $Y$ | $P_{sh} = 1 - Y$ | $P_{sh}/P_{sh}(sum)$ |
| 1 | B/C | 0.999999796 | $2.04 \cdot 10^{-7}$ | 0.124693127 |
| 2 | C/D | 0.999999796 | $2.04 \cdot 10^{-7}$ | 0.124693127 |
| 3 | N1/$v_{dd}$! | 0.999999853 | $1.47 \cdot 10^{-7}$ | 0.089854335 |
| 4 | D/Q | 0.999999864 | $1.36 \cdot 10^{-7}$ | 0.083128754 |
| 5 | Q/*gnd*! | 0.999999875 | $1.25 \cdot 10^{-7}$ | 0.076285516 |
| 6 | A/B | 0.999999913 | $8.74 \cdot 10^{-8}$ | 0.053516526 |
| 7 | B/D | 0.999999913 | $8.74 \cdot 10^{-8}$ | 0.053516526 |
| 8 | Q/$v_{dd}$! | 0.999999940 | $5.96 \cdot 10^{-8}$ | 0.036462936 |
| 9 | C/Q | 0.999999942 | $5.83 \cdot 10^{-8}$ | 0.035677684 |
| 10 | N1/B | 0.999999945 | $5.51 \cdot 10^{-8}$ | 0.033746016 |
| 11 | A/C | 0.999999949 | $5.10 \cdot 10^{-8}$ | 0.031200232 |
| 12 | N1/A | 0.999999949 | $5.08 \cdot 10^{-8}$ | 0.031091017 |
| 13 | N1/Q | 0.999999957 | $4.26 \cdot 10^{-8}$ | 0.026086434 |
| 14 | N1/C | 0.999999959 | $4.07 \cdot 10^{-8}$ | 0.024884915 |
| 15 | A/*gnd*! | 0.999999965 | $3.46 \cdot 10^{-8}$ | 0.021187114 |
| 16 | B/Q | 0.999999966 | $3.40 \cdot 10^{-8}$ | 0.020800155 |
| 17 | A/D | 0.999999969 | $3.15 \cdot 10^{-8}$ | 0.019256726 |
| 18 | B/*gnd*! | 0.999999973 | $2.74 \cdot 10^{-8}$ | 0.016744255 |
| 19 | C/*gnd*! | 0.999999974 | $2.58 \cdot 10^{-8}$ | 0.015772579 |
| 20 | N1/D | 0.999999978 | $2.20 \cdot 10^{-8}$ | 0.013441077 |
| 21 | B/$v_{dd}$! | 0.999999979 | $2.14 \cdot 10^{-8}$ | 0.013084317 |
| 22 | D/*gnd*! | 0.999999979 | $2.13 \cdot 10^{-8}$ | 0.013054676 |
| 23 | A/$v_{dd}$! | 0.999999981 | $1.87 \cdot 10^{-8}$ | 0.011463841 |
| 24 | C/$v_{dd}$! | 0.999999985 | $1.49 \cdot 10^{-8}$ | 0.009137585 |
| 25 | A/Q | 0.999999987 | $1.31 \cdot 10^{-8}$ | 0.007990456 |
| 26 | D/$v_{dd}$! | 0.999999989 | $1.06 \cdot 10^{-8}$ | 0.006487213 |
| 27 | N1/*gnd*! | 0.999999993 | $7.27 \cdot 10^{-9}$ | 0.004451322 |
| 28 | *gnd*!/$v_{dd}$! | 0.999999996 | $3.74 \cdot 10^{-9}$ | 0.002291538 |

The analysis of each parameter was conducted with nominal values of the remaining parameters. Every parameter has a significant influence on defect size distribution.

The increase of parameter $p$ causes that maximum value of defect size distribution to increase (see Fig. 3). Moreover,

for higher values of defect radii the probability of shorts becomes smaller. The parameter $X$ changes the defect size distribution slightly in different way.

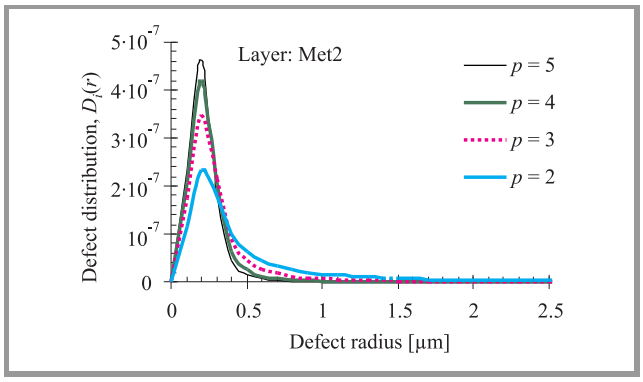


***Fig. 3.*** Defect size distribution for different values of parameter $p$ ($D = 10$ cm$^{-2}$, $X = 0.24$).

The density of the probability reamains constant, but the maximum shifts towards higher values of defect radii with increasing $X$ (see Fig. 4).

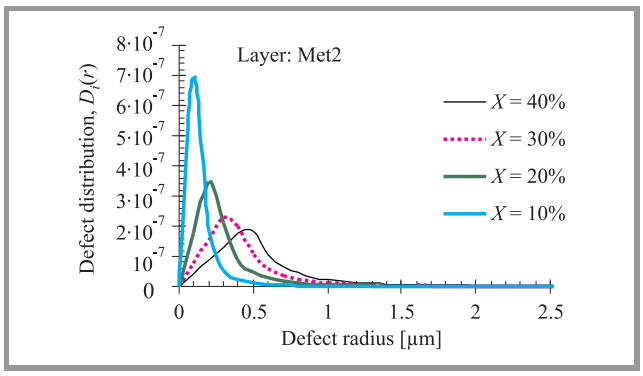


***Fig. 4.*** Defect size distribution for different values of parameter $X$ ($D = 10$ cm$^{-2}$, $p = 3$).

Parameter $D$ can only change the density of probability of short occurrences (see Fig. 5).

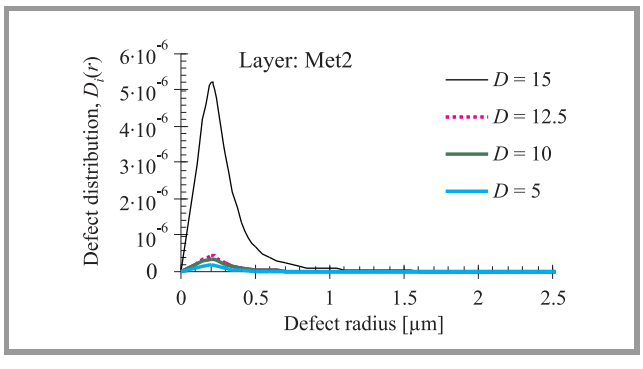


***Fig. 5.*** Defect size distribution for different values of parameter $D$ ($X = 0.24$, $p = 3$).

The parameter $p$ seems to have the most significant influences on the obtained results. The probability does not change in the same way for all critical nets because with the increase of $p$ the probability of fault decreases for radii higher than the one determined by the parameter $X$. In this way the biggest probability changes are observed for the least critical pair of nets and their significance increases with the growth of $p$.

In Table 2 pairs of critical paths have been listed in the order of decreasing probability of short occurrence. We have noticed, however, that this order depends on the value of $p$. This fact may be very important for the generation of test vectors. The efficiency of test vector components in detection of catastrophic faults for the circuit is changing with the parameter $p$.

The probability of manufacturing yield (lack of occurrence catastrophic fault) for three masks, as well as the total probability of manufacturing yield for all layers is shown in Fig. 6 as a function of the parameter $p$. Probability values are normalized to nominal ones obtained at $p = 3$.

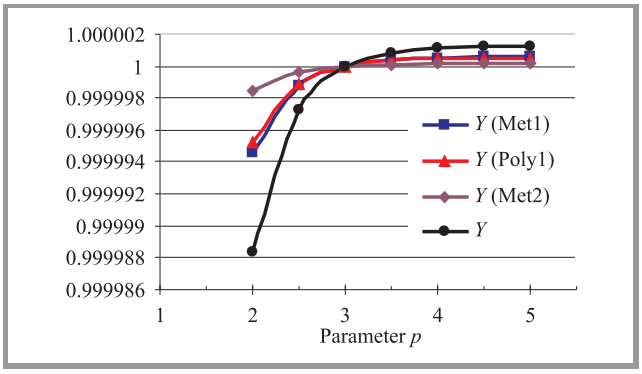


***Fig. 6.*** Defect-related yield normalized to that obtained at nominal value of parameter $p$ ($D = 10$ cm$^{-2}$, $X = 20\%$).

Parameters $X$ and $D$ seem to be less important, but each may strongly affect the probability of fault occurrences, especially parameter $D$. Its changes have an exponential influence on the yield estimation. In contrast to parameter $p$, probability values change in the same way with parameters $X$ and $D$ for all critical pairs. As a result the list of the most significant pairs of critical nets stays unchanged.

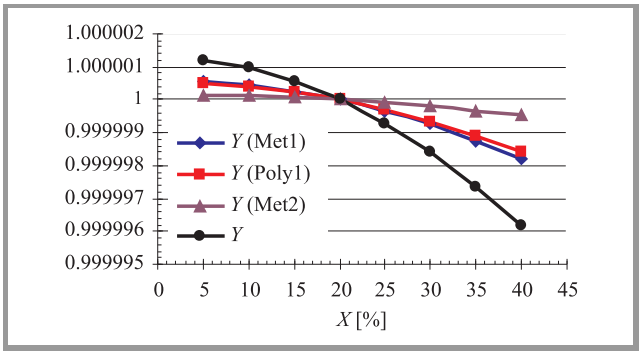


***Fig. 7.*** Defect-related yield normalized to that obtained at nominal value of parameter $X$ ($D = 10$ cm$^{-2}$, $p = 3$).

The probability of manufacturing yield for three conductive layers and total probability of manufacturing yield for all layers are shown as a function of parameter $X$ and $D$

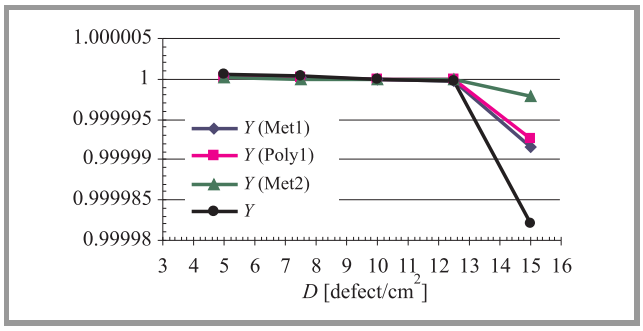


***Fig. 8.*** Defect-related yield normalized to that obtained at nominal value of parameter $D$ ($X = 20\%$, $p = 3$).

in Figs. 7 and 8, respectively. The probability values are normalized to those obtained at nominal value of each parameter.

## 4. Conclusions

We analyzed the sensitivity of the obtained probability on the yield model parameters. Our investigations indicate that:

- the changes of parameter $p$ have the most influence on the calculated probabilities of fault;
- parameter $p$ causes changes the order of the list of the most critical pair of nets;
- with the growth of parameter $p$ the yield is decreasing exponentially;
- the changes of parameters $X$ and $D$ have the same influence on all critical pairs of nets in a circuit;
- with the growth of parameters $X$ and $D$ the probability of fault in a circuit is increasing (for parameter $D$ the growth of this function is exponential).

## Acknowledgement

This work has been supported in part by the Polish State Committee for Scientific Research (project no. 4 T11B 023 24).

## References

[1] R. Ubar, W. Kuzmicz, W. Pleskacz, and J. Raik, "Defect-oriented fault simulation and test generation in digital circuits", in *Proc. ISQED Conf.*, San Jose, USA, 2001, pp. 365–371.

[2] M. Blyzniuk, W. A. Pleskacz, M. Lobur, and W. Kuzmicz, "Estimation of the usefulness of test vector components for detecting faults resulting from shorts in standard cells", in *Proc. 7th Int. Conf. MIXDES*, Gdynia, Poland, 2000, pp. 527–532.

[3] W. A. Pleskacz, D. Kasprowicz, T. Oleszczak, and W. Kuzmicz, "CMOS standard cells characterization for defect based testing", in *Proc. IEEE Int. Symp. DFT'01*, San Francisco, USA, 2001, pp. 384–392.

[4] W. A. Pleskacz and W. Maly, "Improved yield model for submicron domain", in *Proc. IEEE Int. Symp. DFT'97*, Paris, France, 1997, pp. 2–10.

[5] M. Rakowski, "Szybki ekstraktor obszarów krytycznych na zwarcia w dużych układach VLSI", Master's thesis, Warsaw University of Technology, 2006 (in Polish).

**Michał Rakowski** received the B.Sc. and M.Sc. degrees in electronic engineering (with honors) from the Warsaw University of Technology, Poland, in 2006. Since then, he has been pursuing the Ph.D. degree in electronic engineering at the same university, the Institute of Microelectronics and Optoelectronics.

e-mail: M.Rakowski@elka.pw.edu.pl
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Koszykowa st 75
00-662 Warsaw, Poland

**Witold A. Pleskacz** was born in Warsaw, Poland. He received the M.Sc. degree and the Ph.D. degree (with honors) in electronic engineering from the Warsaw University of Technology, Poland, in 1983 and 1995, respectively. Since 1984, he has been with the Institute of Microelectronics and Optoelectronics, at the same university. He spent 18 months as a Post Doctoral Researcher in electrical and computer engineering at Carnegie Mellon University, Pittsburgh, USA. He has authored and co-authored several conference and journal papers. His research interests include: computer-aided design methods and algorithms, layout-oriented manufacturing yield modeling, defect-based approaches to fault modeling, design for manufacturability of ICs.

e-mail: W.Pleskacz@imio.pw.edu.pl
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Koszykowa st 75
00-662 Warsaw, Poland