Paper

Charge-pumping characterization of SOI devices fabricated by means of wafer bonding over pre-patterned cavities

Grzegorz Głuszko, Lidia Łukasiak, Valeriya Kilchytska, Tsung Ming Chung, Benoit Olbrechts, Denis Flandre, and Jean-Pierre Raskin

Abstract—The quality of the silicon-buried oxide bonded interface of SOI devices created by thin Si film transfer and bonding over pre-patterned cavities, aiming at fabrication of DG and SON MOSFETs, is studied by means of charge-pumping (CP) measurements. It is demonstrated that thanks to the chemical activation step, the quality of the bonded interface is remarkably good. Good agreement between values of front-interface threshold voltage determined from CP and *I-V* measurements is obtained.

Keywords— charge-pumping, electrical characterization, interface traps, SOI, wafer bonding, Si layer transfer.

1. Introduction

Silicon-on-insulator (SOI) technology, and especially double-gate (DG) transistors, offers well-known advantages for device operation, such as reduction of short-channel effects (SCE). While in single-gate SOI, improved SCE (in comparison to bulk devices) is reduced due to film thickness, in the case of double-gate devices, short-channel effects may be further lowered thanks to increased vertical electrical control [1].

The aim of this paper is to investigate the quality of SiO_2-Si interface in devices fabricated by a novel process developed in the Université Catholique de Louvain (UCL). This new fabrication process aims at obtaining planar DG and silicon-on-nothing (SON) MOSFETs by the transfer and bonding of a thin Si film on a substrate patterned with cavities and by the subsequent alignment of the device active area and gate definitions over the cavities [2]. Here the quality of the bonded interface is assessed using charge-pumping (CP) measurements on single-gate PIN diodes fabricated simultaneously with the DG SON MOSFETs.

2. Device processing

The devices investigated in this paper were obtained using a novel fabrication method [2] schematically shown in Fig. 1. More details about bonding process can be found in [2]. One of the process critical step, particularly important for the present study, is surface activation prior to bonding, since it plays a major role in the bonded interface quality. Activation using oxygen plasma (which is usual in wafer bonding process) has shown to be detrimental for

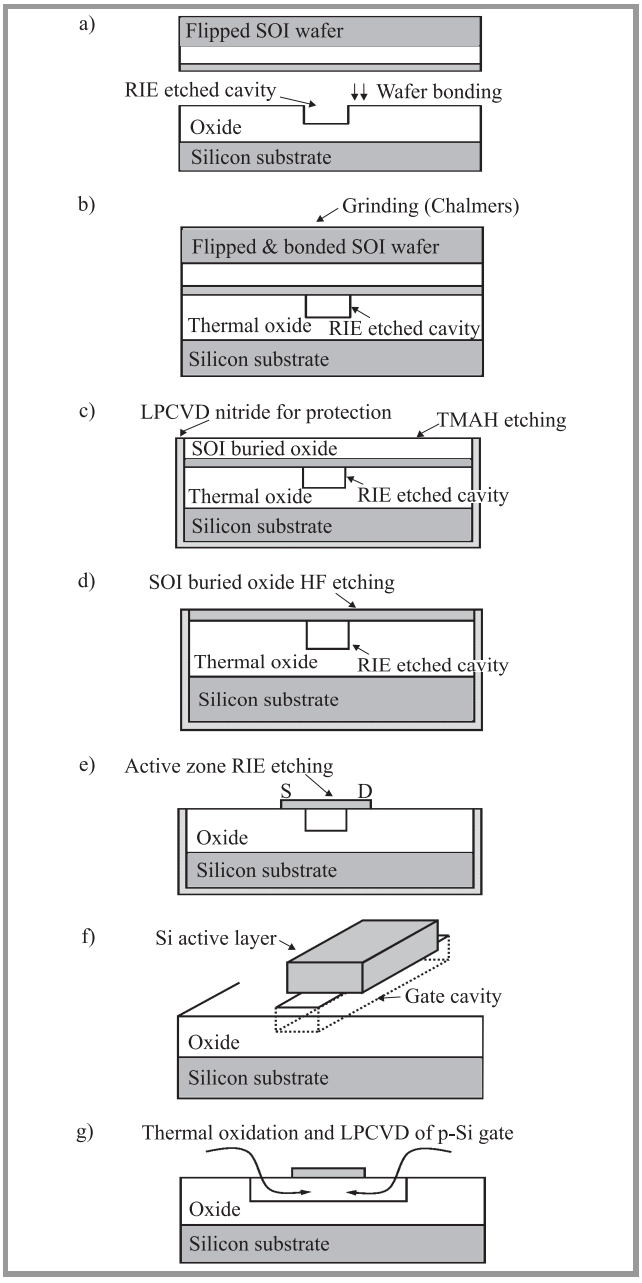


Fig. 1. Novel fabrication method: (a) oxidation of handle wafer, reactive ion etching (RIE) and wafer bonding; (b) SOI substrate thinning via grinding; (c) LPCVD nitride deposition and TMAH etching; (d) BHF etching of SOI BOX; (e) patterning of silicon islands by RIE etching; (f) 3D view of Si island; (g) MOS oxidation and CVD of polysilicon gate.

the electrical properties: high density of interface states and reduced mobility. To assure the good electrical quality of the bonded interface, which is especially important in DG devices, since conduction will take place at this interface,

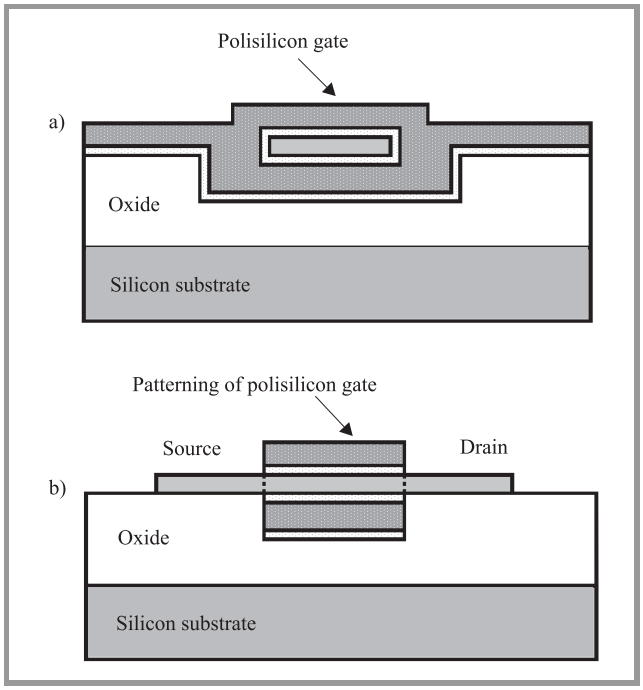


Fig. 2. Cross-section of a DG MOSFET: (a) transversal; (b) longitudinal.

chemical activation has been used. Warm nitric acid has been proven to be a good activation agent [3] and hence in this process we performed activation in nitric acid 70% at 70°C during 10 minutes [2]. Transversal and longitudinal cross-sections of a DG transistor are presented in Fig. 2. A photo of a final device is shown in Fig. 3.

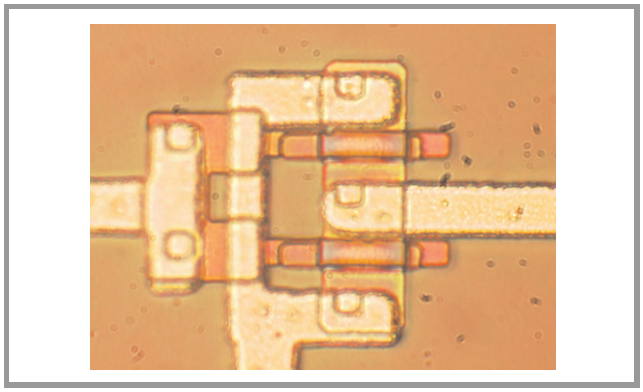


Fig. 3. Photo of a final working double-gate transistor.

Characterization results were compared to those obtained from reference devices. These devices were fabricated using the standard UCL process described in [4] on commercially available UNIBOND® SOI substrates. Otherwise, processing conditions were the same for both device types.

3. Charge-pumping measurements

Since single and double gate fully-depleted transistors had no contact to the body, PIN gated diodes were chosen for charge-pumping measurements using the approach first presented in [5]. Thus the two investigated SiO_2-Si interfaces were the front-gate interface and the back interface between the buried oxide (BOX) and body (Fig. 4). The latter interface is a measure of wafer-bonding quality.

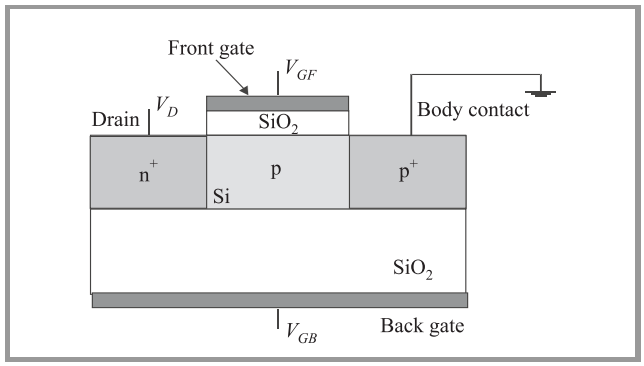


Fig. 4. Schematic cross-section of a SOI PIN diode.

The investigated devices were SG PIN diodes with gate oxide thickness $t_{ox} = 30$ nm, body thickness $t_{Si} = 80$ nm and BOX ≈ 600 nm (400 nm in the reference devices). The effective body doping is approximately $N_A = 10^{15}$ cm^{-3}. Gate dimensions ($W \times L$) of PIN diodes are 570 μm $\times$ 10 μm, 758 μm $\times$ 5 μm and 852 μm $\times$ 3 μm.

Charge-pumping current measured at front-gate interface of a PIN diode fabricated using the novel process flow is plotted as a function of gate base voltage in Fig. 5 for back-gate bias of 0 V and –20 V, respectively. The amplitude of the gate signal (parameter of the family of curves in the diagram) was changed from 2 V to 5 V (solid lines) and then the whole measurement sequence was repeated (squares). The fact that the results of both experiments are very close indicates that no visible generation of interface traps was caused during measurements. Similar results obtained from the back interface are presented in Fig. 6 for front-gate bias of 0 V and –2 V, respectively. In this case, the back gate-signal amplitude was changed between 10 and 30 V and again, no visible degradation due to the applied voltages was observed. The CP curves presented in Fig. 6b do not saturate, it is visible, however, that with increasing amplitudes the increase of maximum charge-pumping current becomes weaker. We believe, therefore, that the maximum charge-pumping current obtained at gate voltage amplitude of 30 V can serve as a good indication of the total density of interface traps at the back interface. Unfortunately, higher amplitudes would damage the structures permanently.

Analysis of CP curves presented above yields a total density of interface traps N_{it}, as well as threshold V_T and flat-band V_{FB} voltage. The obtained results are listed in Table 1.

Table 1
Results of CP characterization performed on PIN diodes fabricated using the novel process flow

Interfaces		$W \times L$ = 570 μm × 10 μm			$W \times L$ = 758 μm × 5 μm			$W \times L$ = 852 μm × 3 μm		
		V_{FB} [V]	V_T [V]	N_{it} [cm^{-2}]	V_{FB} [V]	V_T [V]	N_{it} [cm^{-2}]	V_{FB} [V]	V_T [V]	N_{it} [cm^{-2}]
Front	$V_{GB} = 0$ V	–0.8	–0.2	$3.1 \cdot 10^{10}$	–0.7	–0.2	$2.6 \cdot 10^{10}$	–0.7	–0.2	$2.9 \cdot 10^{10}$
	$V_{GB} = -20$ V	–0.7	0.3	$2.2 \cdot 10^{10}$	–0.5	0.5	$1 \cdot 10^{10}$	–0.5	0.5	$0.7 \cdot 10^{10}$
Back	$V_{GF} = 0$ V	–5	–2.5	$2.6 \cdot 10^{10}$	–8	–3	$2.2 \cdot 10^{10}$	–8	–3	$2.5 \cdot 10^{10}$
	$V_{GF} = -2$ V	3	12	$1.3 \cdot 10^{10}$	7	12	$0.7 \cdot 10^{10}$	6	12	$0.4 \cdot 10^{10}$

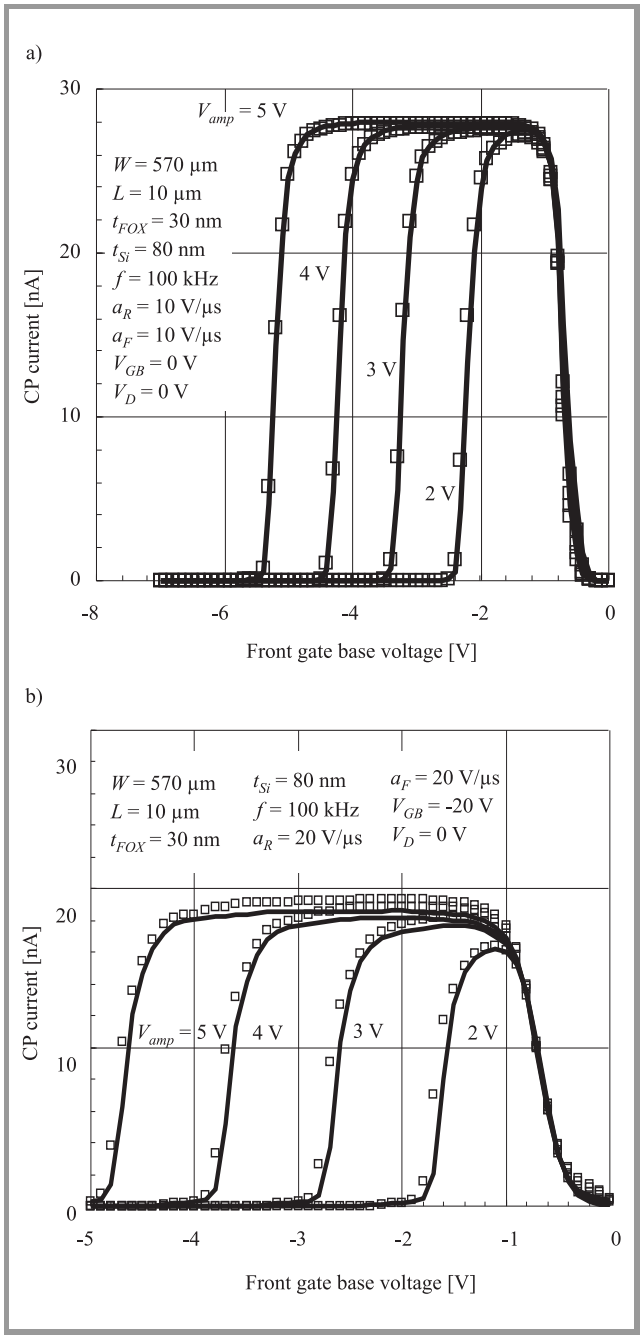


Fig. 5. Charge-pumping current as a function of top-gate base voltage for different amplitudes of the top-gate signal: (a) $V_{GB} = 0$ V; (b) $V_{GB} = -20$ V.

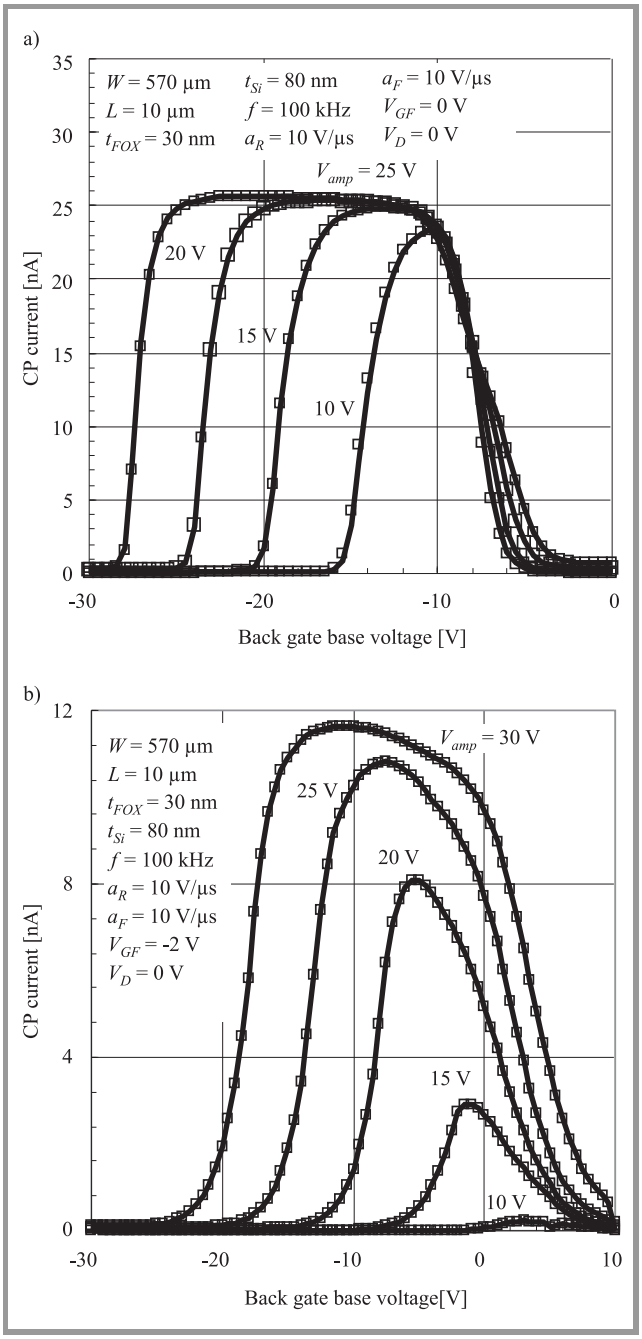


Fig. 6. Charge-pumping current as a function of back-gate base voltage for different amplitudes of back-gate signal: (a) $V_{GF} = 0$ V; (b) $V_{GF} = -2$ V.

It may be seen that interface-trap density is unexpectedly low at both interfaces indicating very good quality of both front-gate oxidation process and additional wafer bonding. The threshold voltage of the front interface obtained at back-gate bias of 0 V is in excellent agreement with that extracted from *I-V* characteristics of single-gate transistors. Threshold voltage was extracted from the intersection of straight lines approximating the log-lin $I_D = f(V_{GS})$ characteristics in the subthreshold and strong inversion regions (Fig. 7) (e.g., [6]).

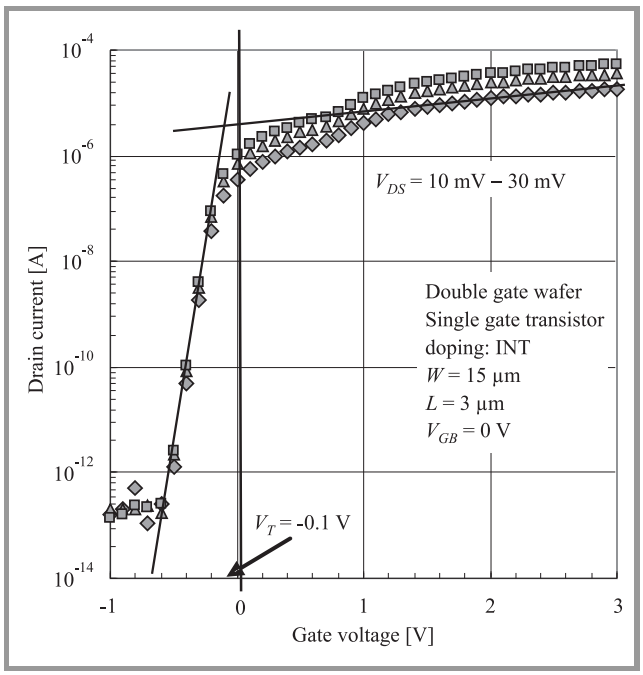


Fig. 7. Transfer characteristics of a single-gate transistor ($V_{GB} = 0$ V).

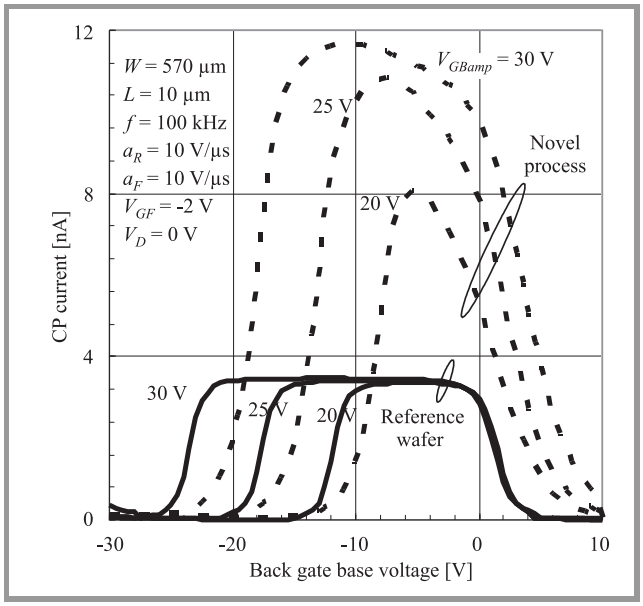


Fig. 8. Comparison of CP measurements performed on novel (dashed line) and reference (solid line) structures.

A comparison with CP measurements performed on back-interface of reference PIN diodes fabricated on a standard UNIBOND® wafer is presented in Fig. 8. The interface trap density at the back interface is slightly lower ($N_{it} = 0.4 \cdot 10^{10}$ cm^{-2}) for reference devices than for those fabricated using the novel process flow ($N_{it} = 1.3 \cdot 10^{10}$ cm^{-2}), which indicates that additional bonding used in our experimental DG SON process only slightly worsens the BOX-Si film interface quality when compared to a commercial well-established UNIBOND® process, in which bonded interface is placed at BOX-substrate interface [7].

4. Conclusions

Thanks to chemical activation of the bonded interface, the density of interface traps is remarkably low at both interfaces of structures fabricated using the novel technique described in [2]. The reliability of CP measurements is confirmed by a very good agreement between the values of front-interface threshold voltage determined by means of CP and *I-V* techniques. Further studies are needed to eliminate potential inaccuracies of the obtained results.

Acknowledgements

This work was partly funded by the 6th Framework Programme of the European Union under contract no. 506844 SINANO (Silicon-based nanodevices), Polish Ministry of Science and Higher Education under project no. 3 T11B 012 28 and Warsaw University of Technology.

References

[1] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-gate silicon-on-insulator MOSFET with volume inversion", *IEEE Electron Dev. Lett.*, vol. 8, pp. 410–412, 1987.

[2] T. M. Chung, B. Olbrechts, U. Södervall, S. Bengtsson, D. Flandre, and J.-P. Raskin, "Planar double-gate SOI MOS devices: fabrication by wafer bonding over pre-patterened cavities and electrical characterization", *Solid-State Electron.*, vol. 51, no. 2, pp. 231–238, 2007.

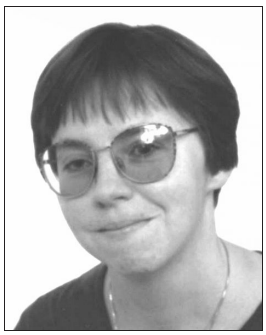
[3] S. I. Lai, H. Y. Lin, and C. T. Hu, "Effects of surface treatment on wafer direct bonding process", *Mater. Chem. Phys.*, vol. 83, pp. 265–272, 2004.

[4] D. Flandre *et al.*, "Fully depleted SOI CMOS technology for heterogeneous micropower, high-temperature or RF microsystems", *Solid-State Electron.*, vol. 45, pp. 541–549, 2001.

[5] T. Ouisse *et al.*, "Adaptation of the charge pumping technique to gated PIN diodes fabricated on silicon on insulator", *IEEE Trans. Electron Dev.*, vol. 38, pp. 1432–1444, 1991.

[6] A. Jakubowski, W. Marciniak, and H. M. Przewłocki, *Diagnostic Measurements in LSI/VLSI Integrated Circuits Production*. Singapore: World Scientific, 1991.

[7] M. Bruel, "Silicon on insulator material technology", *Electron. Lett.*, vol. 31, pp. 1201–1202, 1995.



Lidia Łukasiak graduated from the Faculty of Electronics, Warsaw University of Technology (WUT), Poland, in 1988 and joined the Institute of Microelectronics and Optoelectronics the same year. She received the Ph.D. and D.Sc. degrees from Warsaw University of Technology in 1994 and 2002, respectively. In 1995 she received Prime Minister's Award for a distinguished Ph.D. thesis. Her research interests include modeling and characterization of semiconductor devices, as well as microprocessor techniques.

e-mail: L.Lukasiak@imio.pw.edu.pl
Institute of Microelectronics and Optoelectronics
Warsaw University of Technology
Koszykowa st 75
00-662 Warsaw, Poland

Valeriya Kilchytska received M.Sc. degree in solid-state electronics and Ph.D degree in semiconductors and dielectrics physics, from Kiev University in 1992 and in 1997, respectively. Her Ph.D. work was devoted to the electrical and radiation properties of SOI structures. Until 2001 she was with the Institute of Semiconductor Physics, where she was involved in the wide bias and temperature range characterization of SOI devices. Since 2002 she is with the Microelectronics Laboratory of the Université catholique de Louvain, Louvain-la-Neuve, Belgium. Her current research interest is focused on the room- to high-temperature characterization and simulation of the advanced deep sub-0.1 μm devices.

e-mail: lerka@dice.ucl.ac.be
Microelectronics Laboratory (DICE)
Université catholique de Louvain (UCL)
Place du Levant 3
B-1348 Louvain-la-Neuve, Belgium

Tsung Ming Chung was born in Kuala Lumpur, Malaysia, in 1976. He graduated with a Bachelor in material science and engineering from the University of Science, Malaysia, in 1999. He pursued his studies later on at Delft University of Technology and graduated with an international Master of science in materials science. He is currently finishing his Ph.D. thesis carried out at the Université catholique de Louvain, Louvain-la-Neuve, Belgium. The main topic of research for his Ph.D. was SOI MOSFET novel devices, with emphasis on the electrical characteristics in both the analog and dynamic region. The research was carried out with the support of EuroSOI.

e-mail: tsungming88@gmail.com
Microwave Laboratory (EMIC)
Université catholique de Louvain (UCL)
Place du Levant 3
B-1348 Louvain-la-Neuve, Belgium

Benoit Olbrechts received the electrical engineering degree from the Université catholique de Louvain (UCL), Louvain-la-Neuve, Belgium, in 2003. He currently works at Microwave Laboratory, UCL. His research activities concern the study of wafer bonding mechanisms in the frame of thin film transfer and 0-level packaging applications. Another part of his work deals with the development of sensors on thin SOI membranes, particularly gas and pressure sensors.

e-mail: benoit.olbrechts@uclouvain.be
Microwave Laboratory (EMIC)
Université catholique de Louvain (UCL)
Place du Levant 3
B-1348 Louvain-la-Neuve, Belgium

Denis Flandre received the E.E., the Ph.D. and the post-doctoral thesis degrees from the Université catholique de Louvain (UCL), Louvain-la-Neuve, Belgium, in 1986, 1990, and 1999, respectively. His doctoral research was on the modeling of SOI MOS devices for characterization and circuit simulation. His post-doctoral thesis was on a systematic and automated synthesis methodology for MOS analog circuits. Since 2001, he is a full-time Professor at UCL. He is involved in the research and development of SOI MOS devices, digital and analog circuits, as well as sensors and MEMS, for special applications, i.e., high-speed, low-voltage low-power, microwave, rad-hard and high-temperature electronics and microsystems. He is a co-founder of CISSOID S.A., a spin-off company of UCL focusing on SOI circuit design services.

e-mail: Flandre@dice.ucl.ac.be
Microelectronics Laboratory (DICE)
Université catholique de Louvain (UCL)
Place du Levant 3
B-1348 Louvain-la-Neuve, Belgium

Jean-Pierre Raskin was born in Aye, Belgium, in 1971. He received the industrial engineer degree from the Institut Supérieur Industriel d'Arlon, Belgium, in 1993, and the M.Sc. and Ph.D. degrees in applied sciences from the Université catholique de Louvain (UCL), Louvain-la-Neuve, Belgium, in 1994 and 1997, respectively. From 1994 to 1997, he was a research engineer at the Microwave Laboratory, Université catholique de Louvain, Belgium. He worked on the modeling, characterization and realization of MMIC's in silicon-on-insulator (SOI) technology for low-power, low-voltage applications. In 1998, he joined the EECS Department of The University of Michigan, Ann Arbor, USA. He has been involved in the development and characterization of micromachining fabrication techniques for microwave and millimeter-wave circuits and microelectromechanical transducers/amplifiers working in hard environments. Since January 2000, he is Associate Professor at the Microwave Laboratory of the Université catholique de Louvain, Louvain-la-Neuve, Belgium. His research interests are the modeling, wideband characterization and fabrication of advanced SOI MOSFETs as well as micro- and nanofabrication of MEMS/NEMS sensors and actuators. He is a IEEE Senior Member, EuMA Associate Member and Member of the Research Center in Micro and Nanoscopic Materials and Electronic Devices of the Université catholique de Louvain. He is author or co-author of more than 250 scientific articles.

e-mail: pierre.raskin@uclouvain.be
Microwave Laboratory (EMIC)
Université catholique de Louvain (UCL)
Place du Levant, 3
B-1348 Louvain-la-Neuve, Belgium

Grzegorz Głuszko – for biography, see this issue, p. 8.