Paper

The influence of annealing (900°C) of ultra-thin PECVD silicon oxynitride layers

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Abstract—This work reports on changes in the properties of ultra-thin PECVD silicon oxynitride layers after high-temperature treatment. Possible changes in the structure, composition and electrophysical properties were investigated by means of spectroscopic ellipsometry, XPS, SIMS and electrical characterization methods (*C-V*, *I-V* and charge-pumping). The XPS measurements show that SiO_xN_y is the dominant phase in the ultra-thin layer and high-temperature annealing results in further increase of the oxynitride phase up to 70% of the whole layer. Despite comparable thickness, SIMS measurement indicates a densification of the annealed layer, because sputtering time is increased. It suggests complex changes of physical and chemical properties of the investigated layers taking place during high-temperature annealing. The *C-V* curves of annealed layers exhibit less frequency dispersion, their leakage and charge-pumping currents are lower when compared to those of as-deposited layers, proving improvement in the gate structure trapping properties due to the annealing process.

Keywords—ultra-thin dielectrics, silicon oxynitride, PECVD, CMOS.

1. Introduction

According to the ITRS roadmap [1] SiO_2 gate dielectric will have to be replaced with by layers exhibiting higher dielectric constants. Ultra-thin silicon oxynitride (SiO_xN_y) seems to be a promising candidate as gate dielectric in future CMOS IC's (e.g., [2, 3]).

However, during standard CMOS self-aligned technology the implantation of source/drain regions is followed by a high-temperature annealing aiming at electrical activation of the implanted dopants. These processes occur after gate dielectric fabrication and may obviously influence its electrophysical properties.

This work reports on changes in properties of ultra-thin plasma enhanced chemical vapour deposition (PECVD) silicon oxynitride layers after high-temperature treatment. Possible changes in the structure, composition and electrophysical properties were investigated by means of spectroscopic ellipsometry, XPS, SIMS and electrical characterization.

2. Experimental

Non-self-aligned Al gate NMOS technology was used to fabricate test structures on 2" p-type ⟨100⟩ Si wafers. Oxynitride layers were deposited in a PlasmaLab System 80+ of Oxford plasma technology. The parameters of the PECVD process were optimized to allow repeatable formation of gate dielectrics. Split experiments with annealing of the obtained layers in argon at 900°C for 30 minutes were done. Process parameters are shown in Table 1.

Table 1
Process parameters allowing formation of ultra-thin silicon oxynitride layers

Parameters	Values
SiH_4 (2%): N_2 [sccm]	150
N_2O [sccm]	16
NH_3 [sccm]	32
Pressure [mTr]	500
Power [W]	10
Time [s]	20
Temperature [°C]	350
Time of annealing [min]	30
Temperature of annealing [°C]	900

The properties of the obtained layers were examined by means of: optical, electrical, XPS and SIMS measurements.

The thickness of the oxynitride layers was measured using a J. A. Wollam spectroscopic ellipsometer.

The X-ray photoelectron spectroscopy (XPS) analysis and ultra-low-energy-secondary ion mass spectroscopy (ULE-SIMS) profiles were used to observe the changes in chemical composition and component profiles due to the high-temperature treatment.

The XPS measurements were performed at the undulator beamline U49/2-PGM-2 supplying photons in the energy range of 80 eV – 1500 eV with a resolution above 7000 ($E/\Delta E$). An EA125 electron analyser (Omicron NanoTechnology GmbH) with a resolution of ∼200 meV was used.

The SIMS measurements were done using SAJW-05 system equipped with 06-350E Physical Electronics Ar^+ gun (ultra-low energy 880 eV Ar^+ beam) and Balzers QMA-410 quadrupole mass spectrometer. Quantitative atomic concentration of nitrogen and oxygen was calculated based on Si_2N^+, Si_2O^+ and Si_2^+ secondary ion currents.

Electrical measurements were performed with Hewlett-Packard 4061A Semiconductor Component Test System (*C-V* characteristics) and Keithley SMU (*I-V* characteristics). The metal-insulator-semiconductor (MIS) capacitors with gate area of $A = 1.7 \cdot 10^{-5}$ cm^2 were used to determine the basic electrophysical properties of the investigated layers. Moreover, charge-pumping currents of MISFETs ($W \times L = 10\ \mu\text{m} \times 10\ \mu\text{m}$) were measured to evaluate interface-trap density.

3. Results and discussion

Changes in the structure and composition of PECVD silicon oxynitride layers due to high-temperature annealing were studied by XPS measurements. To get the information about chemical bonds present in SiO_xN_y the measured spectra were analysed using line deconvolution. Every single line was attributed to the particular compound, due to its unique binding energy in the ultra-thin dielectric layer. Figure 1 shows a comparison of the chemical composition of the dielectric layers before and after annealing (expressed in terms of thickness and referred to the thickness obtained from the ellipsometric measurements) as determined from the Si2p line.

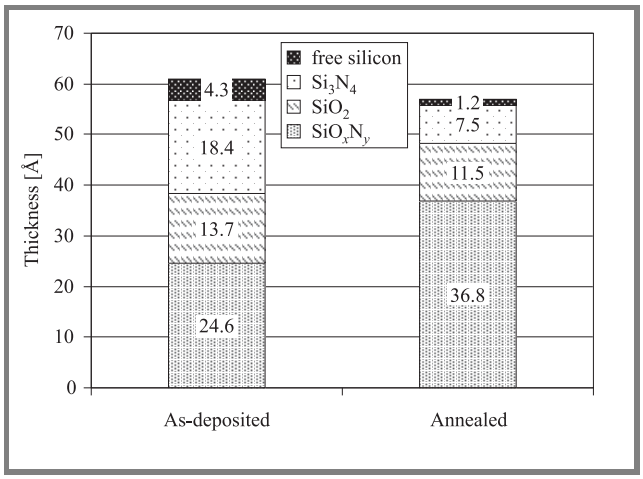

Fig. 1. Composition of PECVD ultra-thin silicon oxynitride layers (expressed as thickness), as determined from the Si2p line analysis.

From Fig. 1 a number of conclusions can be drawn. First – SiO_xN_y is the dominant phase in both as-deposited and annealed layers. Second – high-temperature annealing causes the amount of all phases other than oxynitride to decrease. These phases include oxide, silicon and, particularly significant, nitride (decreasing by almost 60%). It seems reasonable to expect that the growth of oxynitride takes place at the expense of nitride and oxide, while the decrease of the amount of free silicon resulting from annealing is probably due to the saturation of silicon dangling bonds during this high-temperature process. Third – the ultra-thin oxynitride layer can be considered thermally stable in terms of the total layer thickness, as no significant change in this parameter is observed after annealing at high temperatures. This is very important for application of such oxynitride layers in the self-aligned CMOS technology since post implantation high-temperature annealing must not result in any significant changes of the layer thickness. Such changes would obviously be detrimental to the overall integrity of the gate stack.

The SIMS profiles obtained for the same layers are shown in Fig. 2. It should be noticed that despite comparable physical thickness (as determined by ellipsometric measurements), sputtering of annealed dielectric layers during the measurement is much slower than that of as-deposited ones. Consequently, the location of the silicon/layer interface on the sputtering time scale is quite different for as-deposited and annealed layers (see Fig. 2). This difference in etching

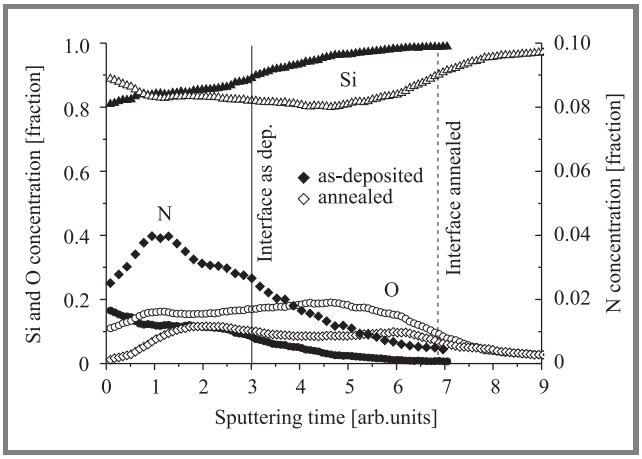

Fig. 2. The SIMS profiles of as-deposited and annealed silicon oxynitride layers.

rate has to be attributed to changes in physical and chemical properties (e.g., saturation of dangling bonds, densification of the layer) that must have taken place during high-temperature annealing of the oxynitride layers. A similar result has been observed during wet etching of ultra-thin oxynitride layers during formation of transistor gate. The wet etching time increased 18 times (from 10 seconds for as-deposited layers to 3 minutes for annealed ones)!

These observations indicate that annealed layers should exhibit better electrophysical properties than as-deposited ones. In fact, these expectations have been confirmed by the analysis of electrical properties of the studied ultra-thin dielectric/silicon system. The results of this analysis are presented below.

Another observation resulting from SIMS profiles is that nitrogen and oxygen are distributed more homogeneously in annealed layers than in as-deposited ones. In the case of the latter the maximum nitrogen concentration is located well within the layer (neither close to the top surface, nor to the interface).

The capacitance-voltage characteristics obtained from the test structures are shown in Fig. 3. It is clear that *C-V* curves of MIS capacitors with annealed oxynitrides exhibit smaller frequency dispersion in all regions (inversion,

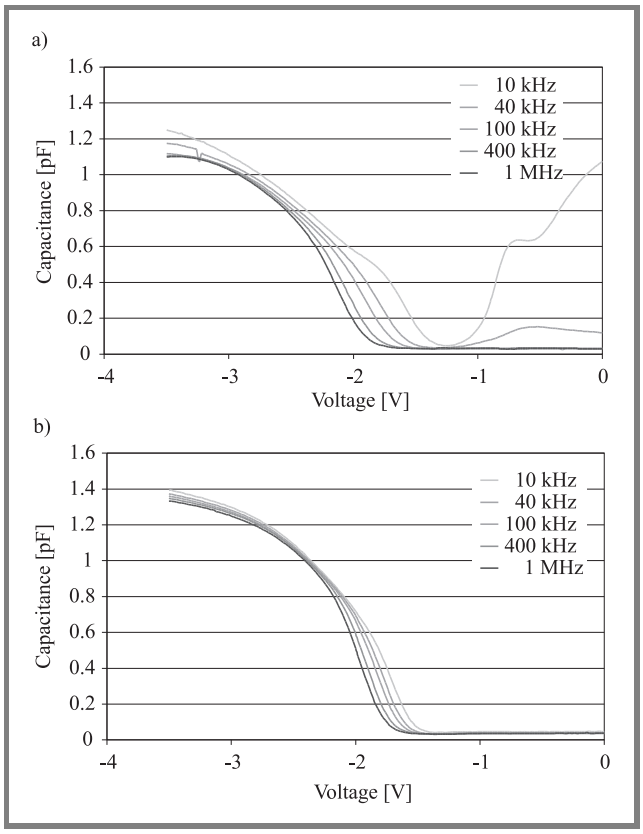

Fig. 3. Comparison of *C-V* characteristics of MIS structures with (a) as-deposited and (b) annealed silicon oxynitride layers.

depletion and accumulation). Moreover, the maximum capacitance $C_{\max}$ is higher in annealed structures. Since the total layer thickness (determined by ellipsometric measurements) is comparable for both annealed and as-deposited layers and $C_{\max}$ is stable over a wide voltage range we can conclude that the dielectric constant is increased as a result of annealing. The parameters presented in Table 2 confirm this assumption.

Table 2
Optical thickness and basic electrophysical properties of PECVD SiO_xN_y layers

Parameters	As-deposited	Annealed
Thickness [Å]	61	57
EOT [Å]*	50	42
Q_{eff}/q [cm^{-2}]**	$4.75 \cdot 10^{12}$	$4.82 \cdot 10^{12}$
D_{it} [cm^{-2}ev^{-1}]***	$1.2 \cdot 10^{13}$	$7.2 \cdot 10^{12}$
* EOT stands for equivalend oxide thickness (determined from *C-V* measurements), ** evaluated from *C-V* measurements, *** evaluated from *C-P* measurements.		

Table 2 compares the thickness and basic electrophysical parameters of the oxynitride layers, determined by means of spectroscopic ellipsometry, *C-V* and charge-pumping (CP).

The equivalent oxide thickness (EOT) is lower than physical thickness by 16% in the case of as-deposited layers and by 26% in the case of annealed ones. This is due to the fact that the dielectric constant of annealed layers is higher than that of as-deposited ones. The effective charge (as determined from *C-V* measurements) does not seem to be affected by annealing but the trap density determined from CP measurements is almost twice lower for annealed layers. It may be thus concluded that annealed oxynitride exhibits better electrophysical properties.

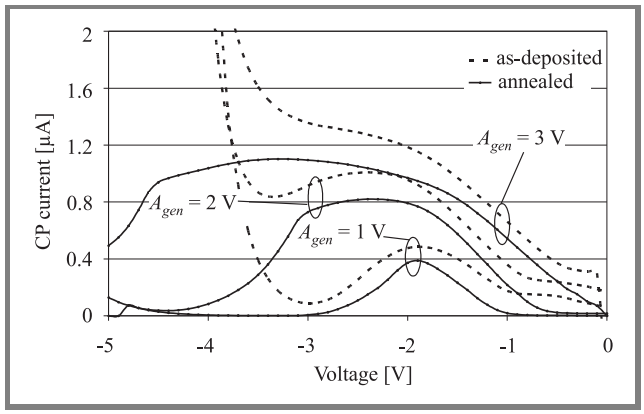

Fig. 4. Comparison of CP currents of MISFETs ($W \times L = 10\ \mu\text{m} \times 10\ \mu\text{m}$).

As seen in Fig. 4 only CP characteristics of MISFETs with annealed layers demonstrate classical behavior. Significantly higher CP currents of MISFETs with as-deposited layers at higher gate voltages are probably caused by higher leakage current (see Fig. 5) [4]. Additionally, CP currents of the MISFETs with annealed gate dielectric are clearly lower than these of as-deposited layers. This indicates that annealed layers have lower trap density (see Table 2).

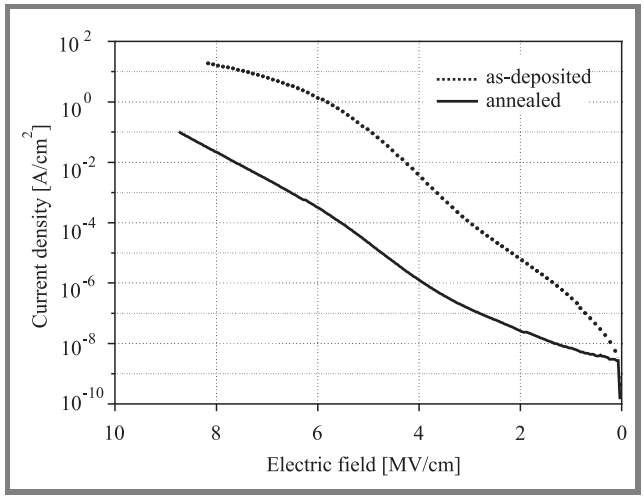

Fig. 5. Current density versus mean electric field within the dielectric layer.

The current-voltage characteristics were also measured in this study. To facilitate a comparison of the insulating properties of the investigated layers, these characteristics are

presented in Fig. 5 as current density versus mean electric field within the SiO_xN_y layer. It is clear that oxynitride layers exposed to high-temperature treatment show much better insulating properties – at intermediate electric fields current density of as-deposited layers is almost four orders of magnitude higher than that of annealed ones.

4. Conclusions

Ultra-thin PECVD silicon oxynitride layers were investigated by means of spectroscopic ellipsometry, XPS, SIMS and electrical characterization.

Ultra-thin PECVD silicon oxynitrides undergo complex changes in chemical composition due to thermal treatment (e.g., decreasing amount of oxide and nitride and increasing amount of SiO_xN_y). The amount of free silicon is lower in annealed layers – probably due to the saturation of free dangling bonds caused by annealing.

Oxygen and nitrogen are distributed more homogenously throughout annealed layers than as-deposited ones. In as-deposited oxynitride layers a maximum of nitrogen concentration is visible between the two interfaces.

Annealed silicon oxynitrides have better insulating properties (as evidenced by significantly lower leakage current). Additionally, annealed SiO_xN_y/Si system has better electrical parameters – lower frequency dispersion and lower interface traps density.

In view of all these results it is justified to conclude that high-temperature annealing improves electrophysical properties of silicon oxynitride layers. Moreover, oxynitride is thermally stable in terms of the total layer thickness, therefore high-temperature annealing may be applied (e.g., dopant activation after the implantation process) following the formation of the gate dielectric in self-aligned CMOS technology.

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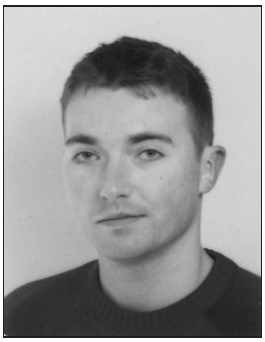

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