

Evaluation of MOSFETs with crystalline high- k gate-dielectrics: device simulation and experimental data

Florian Zaubert, Ralf Endres, Yordan Stefanov, and Udo Schwalke

Abstract— The evaluation of the world's first MOSFETs with epitaxially-grown rare-earth high- k gate dielectrics is the main issue of this work. Electrical device characterization has been performed on MOSFETs with high- k gate oxides as well as their reference counterparts with silicon dioxide gate dielectric. In addition, by means of technology simulation with TSUPREM4, models of these devices are established. Current-voltage characteristics and parameter extraction on the simulated structures is conducted with the device simulator MEDICI. Measured and simulated device characteristics are presented and the impact of interface state and fixed charge densities is discussed. Device parameters of high- k devices fabricated with standard poly-silicon gate and replacement metal gate process are compared.

Keywords— crystalline high- k gate dielectric, rare-earth oxide, praseodymium oxide, gadolinium oxide, damascene metal gate, CMP, CMOS process, TSUPREM4, MEDICI, interface state density, carrier mobility, remote coulomb scattering.

1. Introduction

One of the key challenges of modern MOS technologies is engineering of the gate stack. Lateral dimensions have to be further reduced to the deca-nanometer region in order to continue with the superior performance improvement of CMOS circuits. However, the thickness of the gate dielectric is the main limiting factor at present. Scaling down for sub 32 nm technologies will require an equivalent oxide thickness (EOT) well below 1 nm.

In order to replace SiO₂, mainly amorphous and polycrystalline high- k materials, such as HfO₂ and ZrO₂, have been investigated as alternative gate dielectrics. However, a major drawback of these materials is the need of a SiO₂ buffer layer between the silicon surface and the high- k dielectric, which increases the equivalent oxide thickness and eliminates the chance to achieve an EOT well below 1 nm. Therefore epitaxially-grown crystalline dielectrics with a lattice constant near to silicon have been proposed as alternatives. Praseodymium oxide (Pr₂O₃) was the first epitaxially grown rare-earth material to be investigated as gate dielectric [1, 2]. Fully functional MOSFETs have been fabricated for the first time by our group [3, 4] using conventional poly-silicon gate electrodes. Electrical properties and discussion of device properties can be found in [5–9]. Very recently, devices manufactured using a replacement gate process have been successfully fabricated

with crystalline gadolinium oxide (Gd₂O₃) as dielectric and metal gate electrodes [10, 11]. Metal gate electrodes do not suffer from gate depletion, like poly-silicon electrodes, thus remote coulomb scattering (RCS) is eliminated and carrier mobility is expected to improve. However, metal gates seem to introduce other undesirable effects that nullify the advantages associated with the elimination of RCS. In [12] compressive strain in the channel induced by the metal gate and surface roughness is proposed to describe this behavior.

In this work, MOS device properties associated with the implementation of crystalline rare-earth oxides as gate dielectrics in MOS transistors are discussed. Measurements and simulated device characteristics of replacement gate MOSFETs with crystalline rare-earth high- k dielectric and metal gate are presented and compared to high- k devices manufactured with poly-silicon gate. This includes detailed measurements, including charge-pumping results [10] of prototype devices as well as comprehensive process and device simulation of these structures. By comparison of the fabricated devices with quasi-ideal simulated structures, a better understanding of the impact of high- k material on device properties is obtained. One key issue of this work is to investigate the cause of the low surface mobility of MOSFETs manufactured with high- k dielectrics and to study the impact of gate stack processing, i.e., conventional poly-Si gate versus metal gate damascene technology.

2. Device fabrication and structure

Metal gate damascene NMOSFETs have been fabricated with the replacement-gate technique [10, 11]. The gate stack contains a tungsten electrode and a dielectric composed of Gd₂O₃. A brief outline of the replacement gate process is given in Fig. 1. According to the EXIT-GATE (i.e., gate first) approach [13], dummy gate structures are formed on blank silicon wafers covered with a nitride/poly-Si/nitride sandwich. After source/drain implantation, a SiO₂ layer is deposited by means of plasma enhanced chemical vapour deposition (PECVD) and the ion implantation is activated by a brief RTA-annealing step at 1000°C, which also stabilises the top nitride layer against the following chemical mechanical polishing (CMP) step. Then the CVD oxide is polished down to the top of the dummy gate using a CMP process. The dummy gate is removed completely by wet etching and all harsh pro-

cess steps (RIE, high-temperature anneals) are done. Now, the final gate stack with either high- k oxide or SiO_2 reference dielectric is manufactured. Molecular beam epitaxy (MBE) is used for growing epitaxially a thin Gd_2O_3 layer and subsequent in situ metal deposition (tungsten) is performed. Metal damascene Gd_2O_3 MOSFETs with two different EOTs (53 Å and 21 Å) have been fabricated. Finally, a standard back-end metallization process completes the MOSFET fabrication.

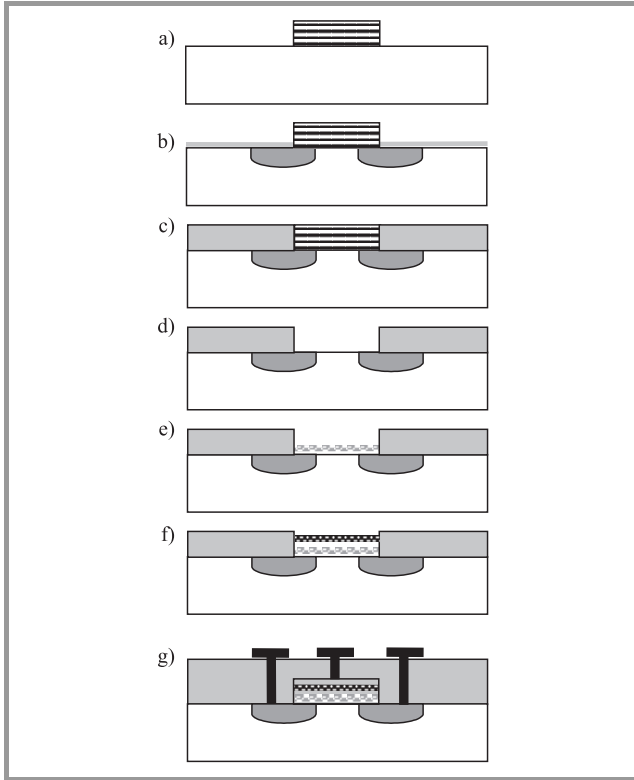


Fig. 1. Outline of the CMP-based metal gate damascene fabrication process: (a) dummy gate stack formation; (b) source/drain formation; (c) alignment oxide formation; (d) dummy gate stack removal; (e) gate dielectric growth; (f) metal gate formation; (g) back-end processing.

The SiO_2 reference devices were also manufactured in replacement-gate technology, having tungsten-titanium electrodes instead and a nitrided RTO- SiO_2 dielectric thickness of $t_{ox} = 50$ Å. Except for the gate dielectric, the reference devices are expected to be largely comparable to the Gd_2O_3 -devices with an EOT of 53 Å, because the tungsten-titanium electrodes have almost the same work function of about 4.55 eV as pure tungsten [14]. Accordingly, there should be no significant difference in threshold voltage or other parameters generated by the gate electrodes. Their main difference between both structures is expected to originate from the different gate dielectric, which may affect the silicon-insulator interface and the channel region close to this interface.

Previously, Pr_2O_3 high- k NMOSFETs have been fabricated using a conventional poly-silicon gate process technology [3] with a k -value of approx. 30, corresponding

to an EOT of about 20 Å–25 Å. These devices are also used for comparison. Further details on the fabrication of the Pr_2O_3 high- k NMOSFETs can be found in [3] and [4].

3. Evaluation methodology

All devices examined in this work have nominal gate lengths of $L = 4$ μm and a gate width of $W = 100$ μm. Due to the relatively long gates, it is guaranteed, that short channel effects do not influence device properties. The measurements include standard characterization methods for determination of the carrier mobility, sub-threshold slope, threshold voltage and transconductance. Carrier mobility of MOSFETs is derived using two different methods. First, by calculating the effective mobility μ_{eff} from the channel conductance at low drain voltage ($V_{ds} = 50$ mV) using Eq. (1). Secondly, by operating the MOSFET in saturation condition ($V_{gs} = V_{ds}$) and using Eq. (2)

$$\mu_{eff} = \frac{L}{W} \frac{g_d}{C_{ins}(V_{gs} - V_T)} \quad \text{with } g_d = \frac{\partial I_d}{\partial V_{ds}}, \quad (1)$$

$$\mu_{sat} = \frac{L}{W} \frac{2I_d}{C_{ins}(V_{gs} - V_T)^2} \quad (2)$$

with L and W channel length and width, channel conductance g_d and the area-independent gate capacitance C_{ins} .

The saturation mobility μ_{sat} is slightly lower than the effective mobility μ_{eff} , because of the presence of the vertical electric field which degrades the carrier mobility in the channel, when driving the MOSFET in saturation. Hence, the effective mobility derived from the channel conductance is usually preferred to describe device mobility, although even here some simplifications have to be made, especially in the estimation of the charge density in the channel [15–17]. Threshold voltage V_T is derived from the channel conductance curves, using Eq. (3)

$$V_T = V_{gs} - \frac{g_d}{K} \frac{L}{W} \quad (3)$$

with $K = \mu C_{ins}$.

The saturation method was used additionally, yielding slightly different values, as discussed above. With Eq. (4) one can calculate the threshold voltage from the saturation curve:

$$V_T = V_{gs} - \sqrt{\frac{2I_d}{K} \frac{L}{W}}. \quad (4)$$

To compare the simulation data with the measured curves one-to-one, it is necessary to implement the same evaluation procedures, i.e., the simulated device results and experimental data are evaluated using the same methods as described above.

With the technology simulator TSUPREM4 the structures for high- k and reference MOSFETs have been implemented referring to the original process parameters. In Figs. 2 and 3 the simulation mesh and the structure of the devices, respectively, are shown. Subsequent to the process simulation,

the electrical evaluation is performed on these computer-generated structures with the device simulator MEDICI.

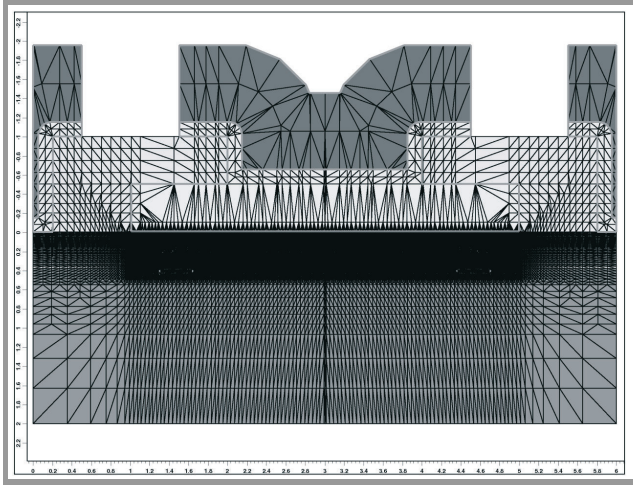


Fig. 2. Example of the simulation mesh of 4 μm n-channel MOSFET with damascene metal gate.

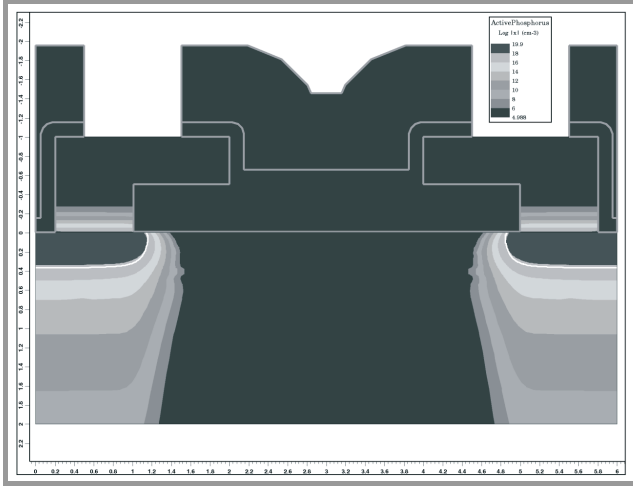


Fig. 3. Example of the simulated MOSFET cross-section with source/drain doping profiles (phosphorus).

It is found, that the selection of the mathematical mobility model is the key parameter, which has the strongest impact on the MOSFET characteristics. The main challenge is to combine several models that are needed for different regions of the semiconductor material. For the semiconductor bulk, a standard analytical model is used in this work, which is based on empirical data [18] and fitting parameters [19]:

$$\mu_{eff} = \mu_{\min} + \frac{\mu_{\max} \left(\frac{T}{300} \right)^{\nu} - \mu_{\min}}{1 + \left(\frac{T}{300} \right)^{\xi} \left(\frac{N(x, y)}{N_{ref}} \right)^{\alpha}}, \quad (5)$$

where μ_{\min} and μ_{\max} are the minimum and maximum carrier mobilities used by the model, $N(x, y)$ is the local impurity concentration, N_{ref} a given reference concentration

and T the absolute temperature, again, α , ν and ξ are fitting parameters.

However, to describe the insulator-semiconductor interface region in detail, appropriate surface models are still required for taking into account scattering effects at impurity atoms and interface roughness:

$$\mu_{S, \perp} = G_{surf} \frac{\mu_{eff} \left(\frac{T}{300} \right)^{-EX_0}}{1 + \left(\frac{E_{eff \perp}}{E_{ref}} \right)^{EX}}, \quad (6)$$

where μ_{eff} is the calculated mobility of the analytical model, $E_{eff \perp}$ is the vertical electric field created by the gate voltage and E_{ref} a reference value, the factor G_{surf} is used to describe effects like surface roughness and crystal strain, which are not included analytically, EX and EX_0 are fitting parameters, the parameter used for modification of the surface mobility μ_S in this work was only G_{surf} .

Furthermore, a model is used to include carrier velocity saturation in the presence of high parallel electric fields. Equation (7) clarifies the correlation between parallel electric field and carrier mobility [18]

$$\mu_{S, \parallel} = \frac{\mu_{eff}}{\left(1 + \left(\frac{\mu_{eff} E_{\parallel}}{v_{sat}} \right)^{\beta} \right)^{\beta^{-1}}} \quad (7)$$

with E_{\parallel} being the parallel field generated by the drain voltage, v_{sat} the saturation velocity [20], μ_{eff} the low field mobility and a fitting parameter β .

Since the sub- V_T slope is affected by the density of interface states, the first attempt was made to adjust the simulated curves to the measured ones, by varying the interface state density in the simulation. This is done by matching the simulated sub- V_T slope to the measured slope. With the sub- V_T slopes being identical, the corresponding interface state density is recorded and is cross-checked with experimental data from charge-pumping measurements.

With this value fixed, the next step in the calibration flow is the adjustment of the carrier mobility in the channel. The mobility, obtained by electrical measurements, is so low that it can only be explained by a high interface-state density. In order to obtain measured mobility values consistent with the simulation, interface roughness and surface scattering have to be included. Because no universal analytical model describing all the above mentioned effects consistently is available to us, the parameter G_{surf} , is used to adjust the surface quality to the experimental conditions.

The last step of the iteration process comprises the fine tuning of the threshold voltage. Especially for the high- k devices in this work, an increased threshold voltage due to the high interface-state density is observed. In addition to the interface-state density, the fixed charges in the dielectric and the gate electrode work function also have an impact on the threshold voltage. For a given metal the value of the work function can vary some tenths of an electronvolt

depending on the manner of depositing the electrode layer on the dielectric and the contact properties between metal and insulator. The alteration of parameters has to be done carefully, because a change in a single device parameter does not only affect one device property. For example, changing the interface state density has an effect on both threshold voltage and sub-threshold slope of the devices. Usually, several adjustment cycles are needed to fix all parameters with a reasonable accuracy.

4. Results

The results provided by the simulations with default parameters show much higher carrier mobility and better sub-threshold slopes than the experimental data of the fabricated devices. Obviously, these very first prototype devices do not feature ideal characteristics and possess substantial potential for improvement.

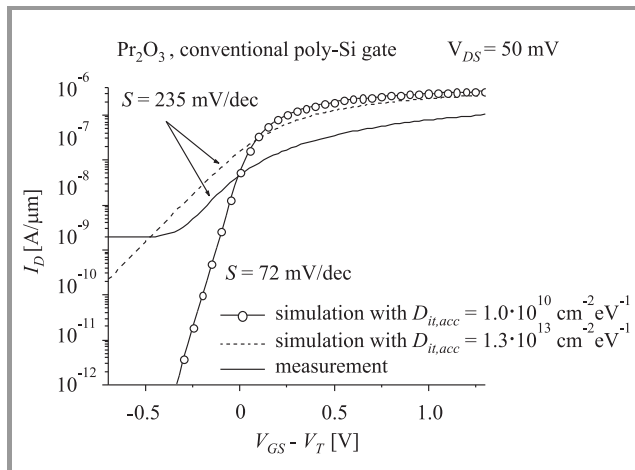


Fig. 4. Comparison of measured and simulated sub-threshold characteristic of MOSFET with Pr_2O_3 dielectric.

As can be seen in Fig. 4, MOSFETs with Pr_2O_3 -dielectric exhibit a sub-threshold slope $S = 235$ mV/dec, which coincides with the simulation data, when assuming an acceptor interface-state density of about $D_{it,acc} = 1.3 \cdot 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$, which is a rather high value. Without interface states the simulation yields a much better sub-threshold slope of $S = 72$ mV/dec. The interface-state density also influences the mobility of the device as derived from the channel conductance curves, as shown in Fig. 5. From device measurements a value of $\mu_{eff} = 40 \text{ cm}^2/\text{Vs}$ is obtained, which is too low to be explained only by interface states. Simulations with the above interface-state density lead to mobilities of $\mu_{eff} = 130 \text{ cm}^2/\text{Vs}$. As mentioned previously, in order to achieve consistent mobility values between measurements and simulation, the G_{surf} parameter has to be adjusted.

Figure 6 compares sub-threshold slopes of the measured metal-gate SiO_2 reference devices with the simulation data for two different cases. Again, the slope of the simu-

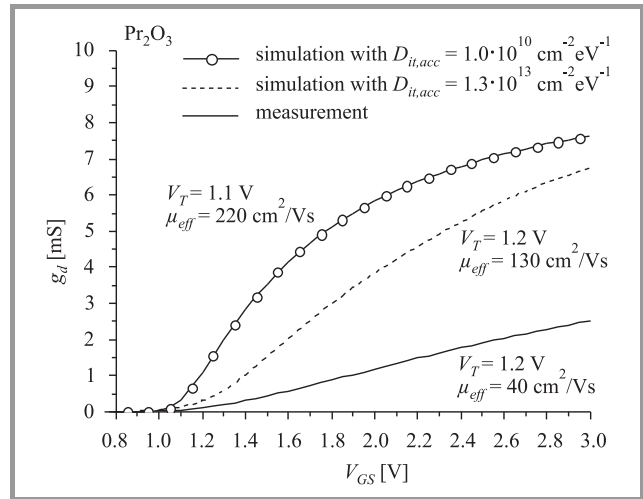


Fig. 5. Comparison of measured and simulated threshold voltage and mobility of Pr_2O_3 -MOSFET.

lated device with ideal interface is much better than that of the measured one. The simulated reference devices exhibit a sub-threshold slope close to the theoretical limit of 60 mV/dec. Adjustment of the interface-state density of the simulated device, makes its sub-threshold slope become

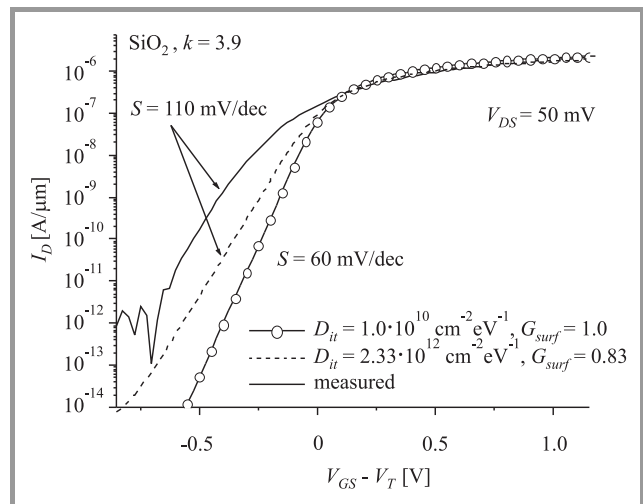


Fig. 6. Comparison of sub-threshold slopes of measurement data and simulated curves with ideal and degraded interfaces for the silicon dioxide reference devices.

very close to the measured one. However, a sub-threshold slope of 110 mV/dec corresponds to a high interface-trap density in the range of $10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, which is unexpected for SiO_2 . Currently, we investigate whether the metal gate blocks H-atoms from penetrating to the Si-SiO₂ interface to cure interface traps during the forming gas anneal. Interestingly, when looking at Fig. 7 a very similar situation can be found for the Gd_2O_3 high- k devices regarding interface trap density. The simulation identifies the theoretical feasible optimal value for the sub-threshold slope of 80 mV/dec, whereas the real devices

posses slopes of 150 mV/dec. To which extent forming gas anneal is beneficial also for Gd₂O₃ high-*k* devices is currently under investigation. Unfortunately, degraded leakage properties have been reported [21] after forming gas anneal, therefore this approach may not be feasible.

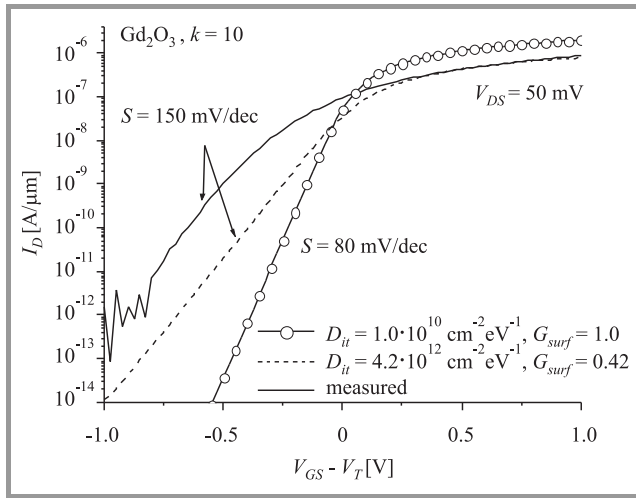


Fig. 7. Comparison of sub-threshold slopes of measurement data and simulated curves with ideal and degraded interfaces for the high-*k* devices.

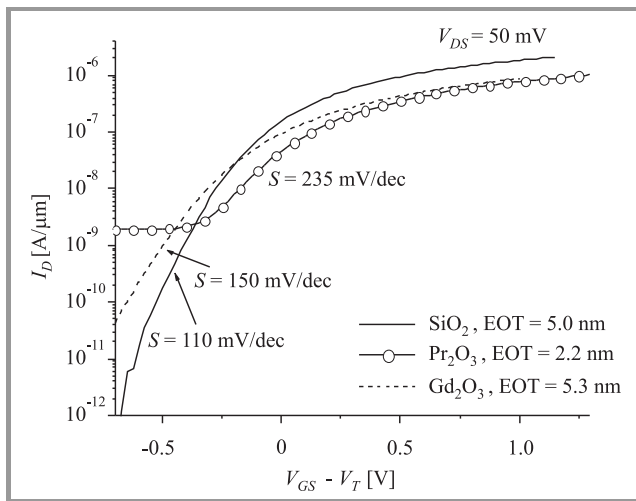


Fig. 8. Measured sub-threshold characteristics of fabricated Pr₂O₃-, Gd₂O₃- and SiO₂ devices.

On the other hand, when comparing the metal gate damascene Gd₂O₃ devices to the conventionally processed poly-silicon gate Pr₂O₃ NMOSFETs, a much better sub-threshold slope (Fig. 8) and mobility value (Fig. 9) is observed. Obviously, for the replacement gate devices the interface quality is improved and/or less process damage has occurred than in the case of the devices manufactured with the conventional poly-Si CMOS process. This may result from the “gentle”, CMP-based gate formation process of the metal gate devices, where the gate dielectric is not exposed to damaging process steps like reactive

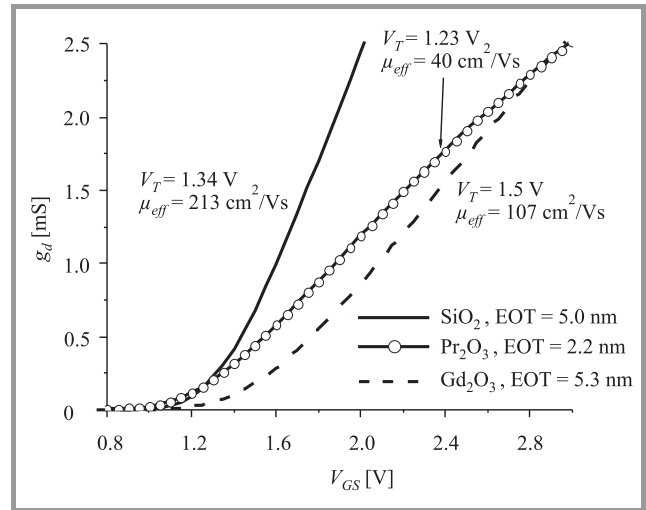


Fig. 9. Measured transconductance and extracted mobility values of fabricated Pr₂O₃-, Gd₂O₃- and SiO₂ devices.

ion etching (RIE) and high-temperature anneals as in the conventional CMOS process. From the adjusted simulated curves the density of interface acceptor states is determined to be $D_{it}(\text{SiO}_2) = 2.33 \cdot 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ and $D_{it}(\text{Gd}_2\text{O}_3) = 4.2 \cdot 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. These values are consistent with the results obtained from energy resolved charge-pumping measurements [10].

Figure 10 compares the channel conductivity of measured and simulated Gd₂O₃ devices. Devices with ideal and degraded interfaces are simulated as can be seen in Fig. 10. Devices with ideal interfaces possess a 2.7-times

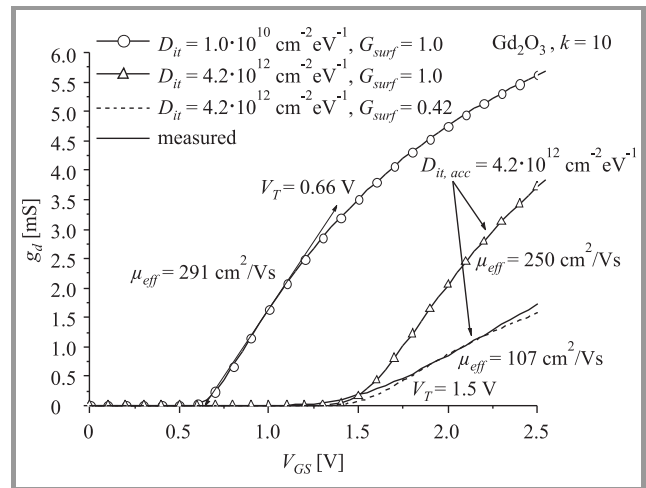


Fig. 10. Comparison of channel conductivities, threshold voltages and carrier mobility of measured data and simulated curves of Gd₂O₃-devices illustrating the effect of ideal and degraded interfaces by simulation.

higher carrier mobility than the measured ones. One factor, which degrading mobility is interface-state density, as mentioned above. However, even for interface-state density of $D_{it} = 4.2 \cdot 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ a mobility of $\mu_{eff} = 250 \text{ cm}^2/\text{Vs}$

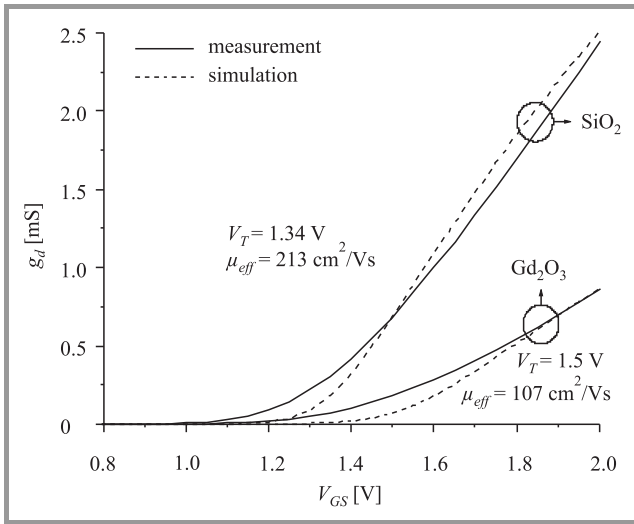


Fig. 11. Comparison of channel conductivities, threshold voltages and carrier mobility of SiO_2 reference and Gd_2O_3 high- k devices.

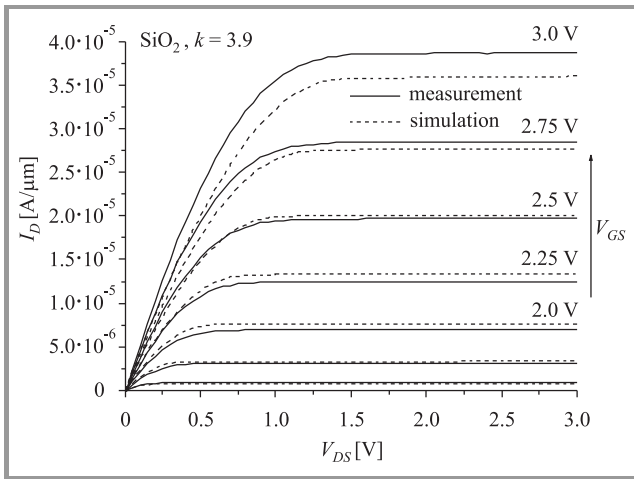


Fig. 12. Measured and simulated output characteristics of reference MOSFETs with SiO_2 gate dielectric.

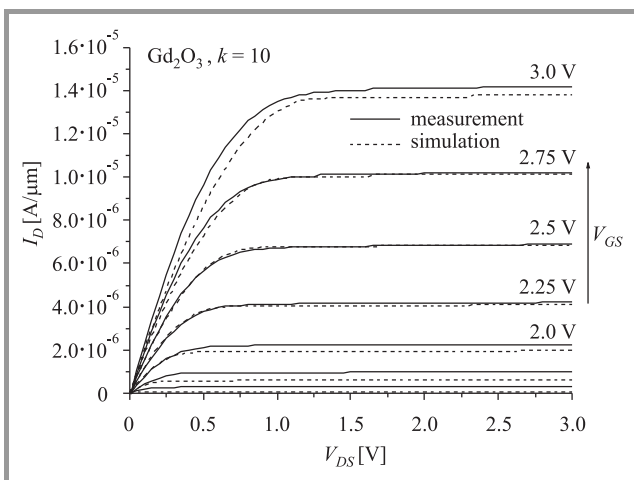


Fig. 13. Measured and simulated output characteristics of MOSFETs with Gd_2O_3 high- k gate dielectric.

is deduced from simulation with otherwise perfect Si-surface, i.e., $G_{surf} = 1$. To obtain the measured mobility value of $\mu_{eff} = 107 \text{ cm}^2/\text{Vs}$, the surface quality needs to be degraded, additionally by lowering G_{surf} to 0.42. From Fig. 11 the threshold voltage and effective mobilities for the high- k devices are extracted from the slopes of the curves using Eqs. (1) and (3) to $V_T = 1.5 \text{ V}$ and $\mu_{eff} = 107 \text{ cm}^2/\text{Vs}$, respectively. It is apparent that the mobility of the high- k devices is only half of that of the reference devices with SiO_2 dielectric of $\mu_{eff} = 213 \text{ cm}^2/\text{Vs}$. Worse interface quality arising from the manufacturing process may be the reason. One major advantage of the thermal oxidation of silicon is the fact that the Si- SiO_2 interface has never been in contact with the outside world, because of the silicon dioxide growing into the bulk material during the oxidation step. This is in contrast to the high- k devices, where the crystalline high- k material is grown on top of the original silicon surface by MBE. To improve the carrier mobility, the interface state density and surface quality, such as roughness or crystal strain [12], have to be improved.

After adjusting all important parameters output characteristic are simulated with the parameters from above and the plots are depicted in Figs. 12 and 13. Because of the considerable gate length, almost no channel length modulation is noticeable as expected. The agreement between simulation and measurement is very reasonable for the high- k devices. However, for the SiO_2 reference devices a deviation at higher gate voltages can be seen. A possible explanation for this behavior may be related to the surface mobility model used for simulation. The mobility model is limited to a dedicated range of electrical fields via Eq. (6). It can be adapted with the factor G_{surf} , when the field is altered over a large range and higher accuracy is required. This issue is subject to further investigations.

5. Conclusions

The first attempt is made to correlate experimental data from fully functional crystalline high- k MOSFETs with results obtained from process- and device-simulation. The measured device characteristics agrees reasonably well with properly adjusted simulation results. The comparison reveals that increased values of the interface state density degrades sub-threshold slope and carrier mobility. However, even though carrier mobility depends slightly on the selected mobility model, interface states alone are insufficient to explain the low mobility values. Additional effects appear to be responsible, like enhanced surface roughness or strain. Nevertheless, damascene metal gate technology has proven to be superior to the conventional poly-Si gate CMOS processing, since the process steps potentially damaging to the high- k gate stack are omitted. However, when device performance is compared to SiO_2 reference MOSFETs, the need of further improvements of the crystalline high- k materials and processing is still obvious.

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