

Development of 3C-SiC MOSFETs

Mietek Bakowski, Adolf Schöner, Per Ericsson, Helena Strömberg, Hiroyuki Nagasawa,
and Masayuki Abe

Abstract— The paper reviews the development of the 3C-SiC MOSFETs in a unique development project combining the material and device expertise of HAST (Hoya Advanced Semiconductor Technologies) and Acreo, respectively. The motivation for the development of the 3C-SiC MOSFETs and the summary of the results from the lateral and vertical devices with varying size from single cell to $3 \times 3 \text{ mm}^2$ large devices are reviewed. The vertical devices had hexagonal and square unit cell designs with $2 \text{ }\mu\text{m}$ and $4 \text{ }\mu\text{m}$ channel length. The p-body was aluminum implanted and the source was nitrogen or phosphorus implanted. Low temperature Ti/W contacts were evaluated.

Keywords— vertical MOSFET, 3C-SiC, channel mobility.

1. Introduction

The 3C-SiC is a cubic polytype of SiC and can be grown on Si. This means that large 3C-SiC crystals equal in diameter to the commercially available Si wafers can be readily made. Processing of large area wafers greatly improves cost per manufactured device. The 6" diameter 3C-SiC wafers have been demonstrated [1].

The 3C-SiC is a promising material for MOSFET devices because of high channel mobility due to lower density of interface states compared to 4H-SiC. Poor performance of 6H- and 4H-SiC MOSFETs is related to the interface states located in the band gap close to the conduction band edge limiting the transport of electrons in the channel [2]. Due to the smaller band gap of 3C-SiC, the interface states observed in 6H- and 4H-SiC are located in the conduction band and have no effect on the transport properties of the channel. Channel mobility values of 75 to $260 \text{ cm}^2/\text{Vs}$ have been reported [3–6].

The 3C-SiC polytype has lower critical electric field value due to the lower band gap. It means that the drift region doping corresponding to a given blocking voltage will be lower compared to the hexagonal 4H- and 6H-SiC polytypes. This also means that the specific junction capacitance will be lower in the 3C-SiC devices as compared to the 4H- and 6H-SiC ones. This is an advantage from the point of view of high speed MOSFETs [7].

Considering all of the above and given large-area substrates of good quality, 3C-SiC may well be the material of choice for medium voltage (600 V to 1200 V) MOSFETs.

We have reported earlier on large area lateral 3C-SiC MOSFETs [8] and on vertical large area 3C-SiC MOSFETs with varying size from a single unit cell to $3 \times 3 \text{ mm}^2$ [9]. We have also reported earlier on the impact of technology on the characteristics of vertical 3C-SiC implanted MOSFETs (DMOSFETs). The MOSFET devices investi-

gated here have a single implanted p-body profile. They will be, however, referred to as DMOSFETs since they represent the most simple and close approximation of double-diffused Si MOSFET concept in SiC technology. The exact translation of the DMOSFET concept into SiC technology is sometimes called DIMOSFET (double implanted MOSFET). Devices with phosphorus and nitrogen implanted source were compared. The impact of low temperature Ti/W contacts on the device characteristics was evaluated and compared to Ni-silicide contacts annealed at 950°C [10]. In this review we include some of the most recent results of voltage blocking characteristics and the temperature dependence of the channel mobility.

2. Lateral MOSFETs

2.1. Experimental

The 2" 3C-SiC $\langle 001 \rangle$ substrates were manufactured by HAST (Hoya Advanced Semiconductor Technologies). A $2 \text{ }\mu\text{m}$ thick p-type epi layer with an Al-doping of 10^{16} cm^{-3} was grown at Acreo. For epitaxial LT MOSFETs (lateral trench MOSFETs), an additional n+ source and drain layer with nitrogen doping concentration of 10^{19} cm^{-3} and thickness of $0.3 \text{ }\mu\text{m}$ was grown. The LDD MOSFETs (lightly-doped-drain MOSFETs) were implanted with nitrogen at 500°C in order to create two box profiles with the doping of 10^{18} cm^{-3} and 10^{20} cm^{-3} in the low doped drain region and source and drain contact regions, respectively. The gate oxide was grown thermally for 90 min at 1100°C in dry oxygen followed by a 3-hour post-oxidation anneal in wet oxygen at 950°C . The resulting oxide thickness was about 60 nm. The devices have two level metallization with oxide/nitride isolated bridges between gate and source interconnections. The $1 \times 1 \text{ mm}^2$, $2 \times 2 \text{ mm}^2$ and $3 \times 3 \text{ mm}^2$ devices contain 220, 880 and 1980 unit cells, respectively. A post-processing annealing was done for 30 min at 400°C in nitrogen.

2.2. Results

Typical output characteristics of the lateral LDD MOS devices are shown in Fig. 1. Both the drain current and the leakage current scale linearly with the device size up to the maximum investigated device size of $3 \times 3 \text{ mm}^2$, as shown in Fig. 2. We could obtain a current of about 0.3 A and 1.2 A with the current flow in the $\langle 110 \rangle$ and $\langle \bar{1}10 \rangle$ direction, respectively, from the largest $3 \times 3 \text{ mm}^2$ devices with gate voltage of 20 V.

Lateral 3C-SiC MOSFET devices were fabricated with the area up to $3 \times 3 \text{ mm}^2$. The LDD MOSFET devices

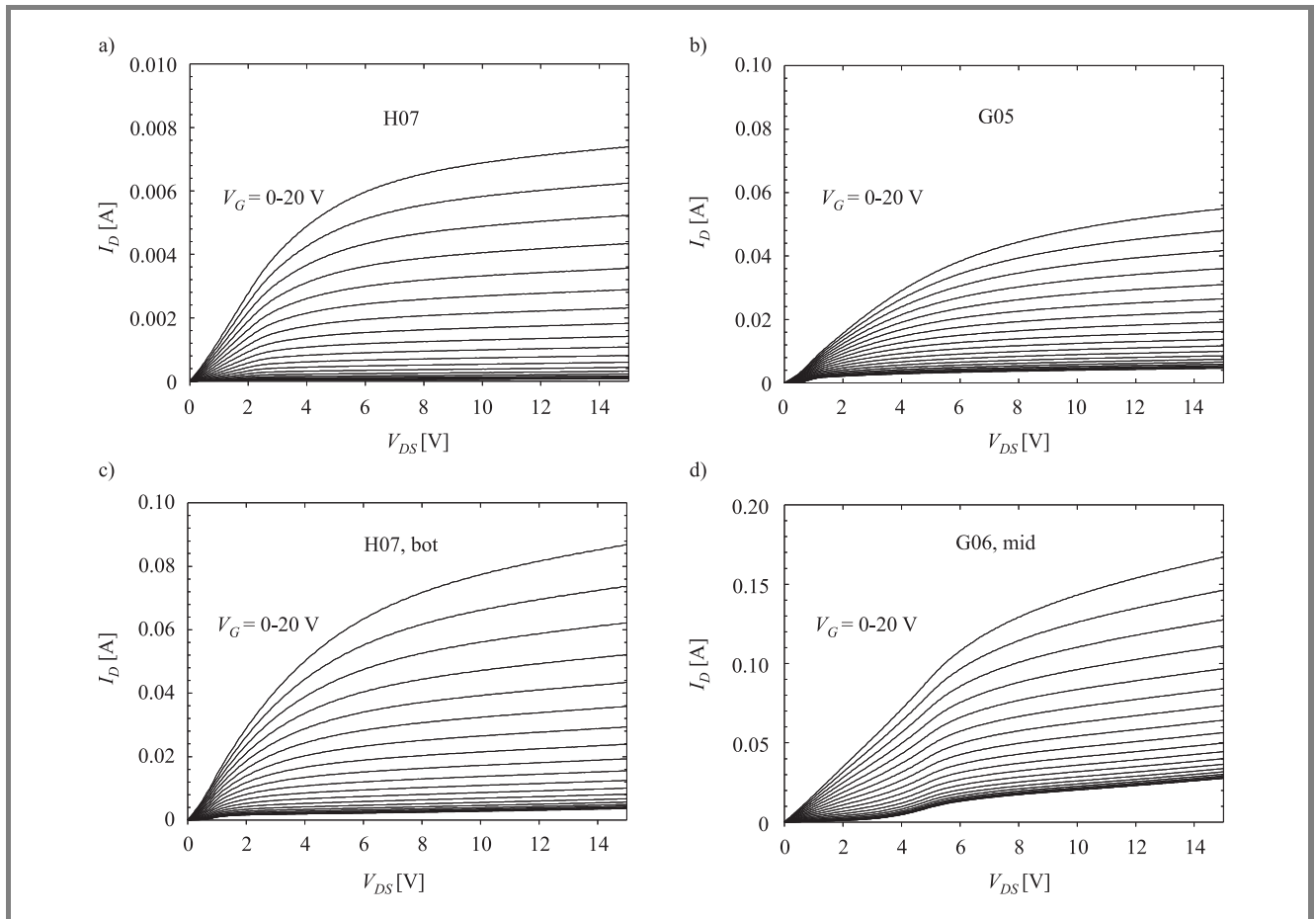


Fig. 1. Output characteristics of large-area LDD MOS devices containing 12×5 (a); 22×10 (b); 44×10 (c); 66×10 (d) cells; $4 \mu\text{m}$, 400°C , corresponding to $0.5 \times 0.5 \text{ mm}^2$, $1 \times 1 \text{ mm}^2$, $2 \times 1 \text{ mm}^2$ and $3 \times 1 \text{ mm}^2$ device area, respectively. Only data with the current flow along the $\langle 110 \rangle$ direction are shown. Note leakage current due to the implanted drain junction.

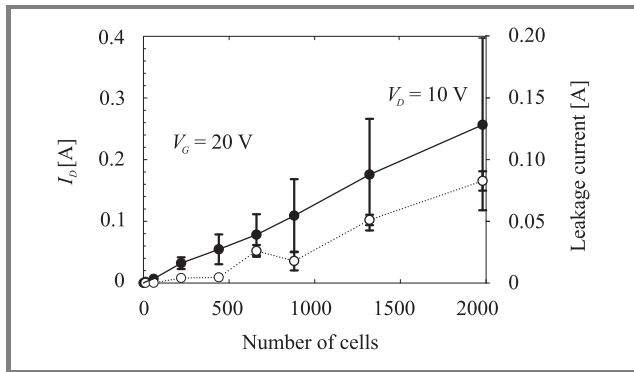


Fig. 2. Drain current (solid line) and leakage current (dotted line) as a function of the number of unit cells for LDD MOS devices with $4 \mu\text{m}$ channel length and current flow along the $\langle 110 \rangle$ direction.

have blocking capability of 100 V and channel mobility 2–3 times higher compared to the average 4H-SiC devices with current flow along the $\langle \bar{1}10 \rangle$ direction [1]. Channel mobility of devices with current flowing along the $\langle 110 \rangle$ direction is comparable to that of an average

4H-SiC device. The properties of the fabricated MOSFETs, of both LT- and LDD-type are dominated by high density of interface states of the order of $10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$. This is at

Table 1
Summary of lateral MOSFET parameters

Parameter	LT MOS (w3) After 400°C anneal $\langle 110 \rangle / \langle \bar{1}10 \rangle$	LDD MOS (w4) After 400°C anneal $\langle 110 \rangle / \langle \bar{1}10 \rangle$
V_{Th} [V]	5/7.5	3/3–5
μ_{eff} [cm^2/Vs]	8–10/2–6 ($V_G = 25 \text{ V}$)	2–4/5–8 ($V_G = 20 \text{ V}$)
μ_{FE} [cm^2/Vs]	15–20/6–15 ($V_G = 25 \text{ V}$)	2–6/10–15 ($V_G = 20 \text{ V}$)
D_{it} [$\text{cm}^{-2}/\text{eV}^{-1}$]	$2 \cdot 10^{13} / 3 \cdot 10^{13}$	$2-4 \cdot 10^{13} / 3-6 \cdot 10^{13}$
Note the dependence of the mobility on the direction of current flow and high density of interface states, D_{it} , obtained from the subthreshold slope.		

present the main reason for the poor performance of 3C-SiC devices compared to what was reported in [5]. The linear scaling of the device performance with the device area confirms the potential of the 3C-SiC material for fabrication of large-area devices. A correlation of high leakage current and high number of extended crystal defects (mainly stacking faults) has been observed. The results are summarised in Table 1.

3. Vertical MOSFETs

3.1. Experimental

The 10 μm thick, $5 \cdot 10^{15} \text{ cm}^{-3}$ doped n-type epilayers were grown on 2" 3C-SiC (001) substrates manufactured by HAST [1]. Box profile with the depth of approximately 1 μm and maximum doping of 10^{18} cm^{-3} obtained by means of aluminum implantation combining five energies from 30 to 700 keV was used to define the p-body region and the ring termination. The n+ source region is defined by a box profile obtained by means of either nitrogen implantation combining three energies of 50, 90 and 150 keV or phosphorus implantation combining three energies of 70, 120 and 200 keV. The depth of this box profile is 0.4 μm and maximum doping is $4 \cdot 10^{19} \text{ cm}^{-3}$. All implantation processes were performed at room temperature. The gate oxide was grown thermally for 90 min at 1100°C in dry oxygen followed by a 3-hour post-oxidation anneal in wet oxygen at 950°C. The resulting oxide thickness was about 60 nm. All wafers underwent a shallow nitrogen implantation (30 keV, $5 \cdot 10^{12} \text{ cm}^{-2}$) in the gate oxide region prior to the thermal oxidation, which has been reported to reduce the interface-state density D_{it} [11]. The fabricated MOSFETs have two level metallization with oxide/nitride isolation between gate and source interconnections. Devices with the area of 1 mm^2 contain up to 976 hexagonal and 660 square unit cells, while those with the area of $3 \times 3 \text{ mm}^2$ contain up to 12000 hexagonal and 8000 square unit cells.

3.2. Results

An example of the output characteristics and device lay-out is shown in Fig. 3.

The difference in performance between devices with phosphorus (P) and nitrogen (N) implanted source is illustrated in Fig. 4, where a comparison between P and N doped $400 \times 400 \mu\text{m}^2$ MOSFETs containing 102 hexagonal cells and ring termination (active area $7.3 \cdot 10^{-4} \text{ cm}^2$), is shown. A comparison of channel mobility extracted from the output characteristics of devices with N doped source and two metallization technologies, nickel silicide and low temperature Ti/W ohmic contacts, is shown in Fig. 5. It is clearly seen that the channel mobility is degraded in the case of nickel silicide contacts due to the 950°C silicidation step performed after gate oxide formation (Fig. 5c).

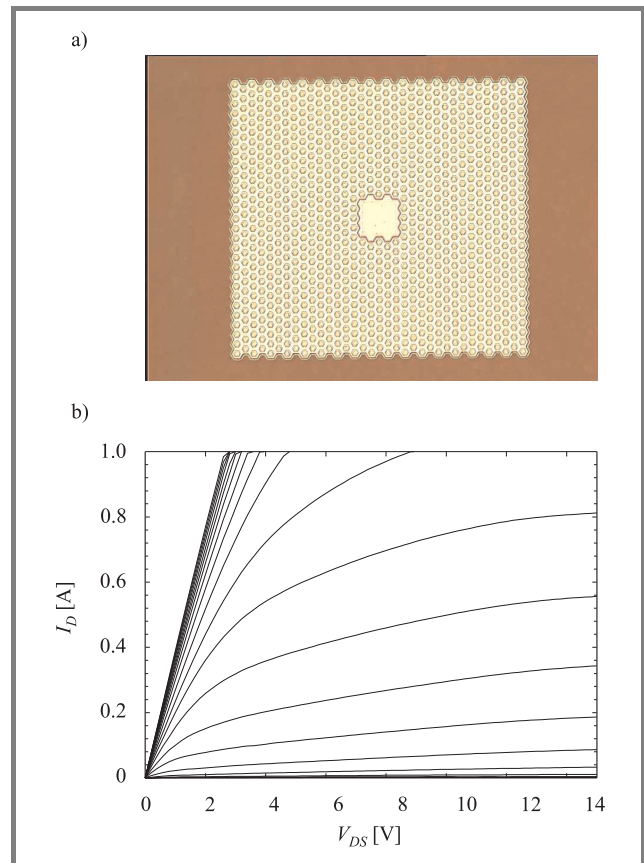


Fig. 3. Micrograph (a) and output characteristics of a $1 \times 1 \text{ mm}^2$ 3C-SiC MOSFET containing 976 hexagonal cells with 2 μm channel length and P implanted source (b). The cell pitch for this device is 28 μm . High temperature steps following the thermal oxidation were avoided and the ohmic contact to the source was made with as-deposited Ti/W.

The channel mobility values are improved by reducing the thermal budget of the processing steps following the gate oxidation (Fig. 5b). The channel mobility ranges from 30 to 40 cm^2/Vs and from 20 to 30 cm^2/Vs for P and N doped source devices, respectively.

Table 2

Comparison of vertical MOSFET parameters for devices with P and N implanted source

Parameter	P impl. source Ti/W no anneal	N impl. source Ti/W no anneal
V_{Th} [V]	-5 to 3	0
μ_{eff} [cm^2/Vs]	30-40	20-30
μ_{FE} [cm^2/Vs]		
D_{it} [$\text{cm}^{-2}\text{eV}^{-1}$]	$1 \cdot 10^{13}$	$7 \cdot 10^{12}$
Sub-threshold slope [mV/dec]	750	750
R_{on} [$\text{m}\Omega\text{cm}^2$] ($V_G = 15 \text{ V}$)	17 ($L_{ch} = 2 \mu\text{m}$) 30 ($L_{ch} = 4 \mu\text{m}$)	24 ($L_{ch} = 2 \mu\text{m}$) 46 ($L_{ch} = 4 \mu\text{m}$)

The devices have high density of interface states of the order of $10^{13} \text{ cm}^{-2}\text{eV}^{-1}$ and sub-threshold slope of 750 mV per decade as illustrated in Fig. 6. In spite of high D_{it} values relatively high channel mobility was observed. From $\text{SiO}_2/\text{3C-SiC}$ MOS interface studies it is expected that D_{it} values can be reduced by at least one order of magnitude, which again indicates the potential of 3C-SiC for high current MOSFET devices [12].

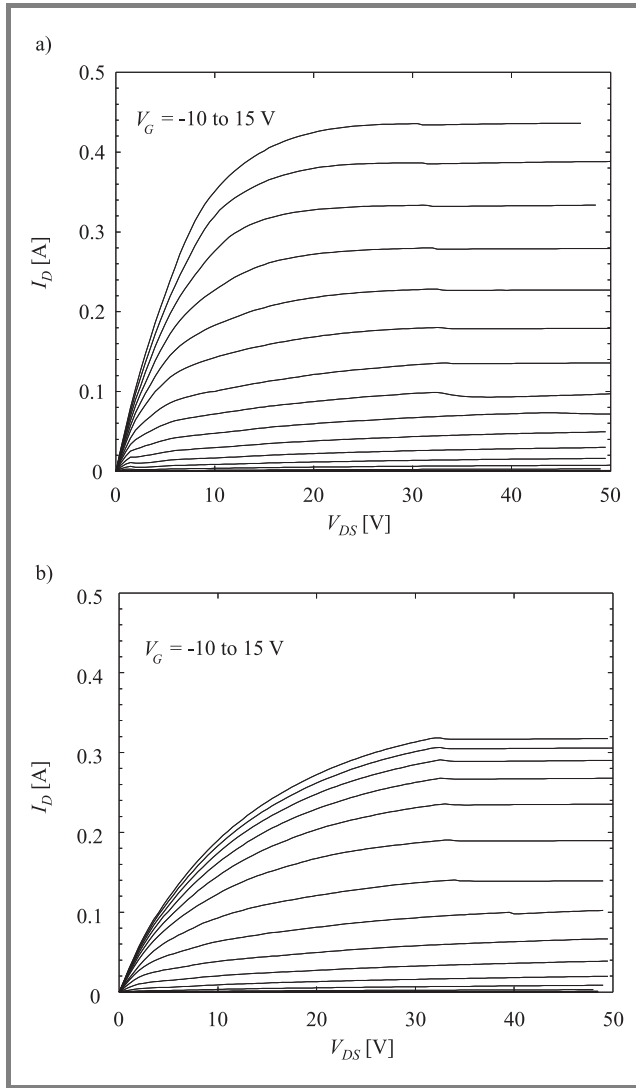


Fig. 4. Output characteristics of a device containing 102 hexagonal cells with $2 \mu\text{m}$ channel length and P implanted source (a) and with N implanted source (b).

The summary of the results obtained from MOSFET with P and N implanted source is given in Table 2.

Vertical 3C-SiC MOSFET devices were fabricated with the area up to $3 \times 3 \text{ mm}^2$. The blocking capability of MOSFET devices was typically 100 V at leakage currents below 1 mA. The specific on-resistance obtained from 0.0025 cm^2 and 0.01 cm^2 devices with P doped source was $17 \text{ m}\Omega\text{cm}^2$ and $30 \text{ m}\Omega\text{cm}^2$ for the channel length of $2 \mu\text{m}$ (cell pitch $28 \mu\text{m}$) and $4 \mu\text{m}$ (cell

pitch $33 \mu\text{m}$), respectively. For the devices with N doped source, the corresponding values of the specific on-resistance were $24 \text{ m}\Omega\text{cm}^2$ and $46 \text{ m}\Omega\text{cm}^2$.

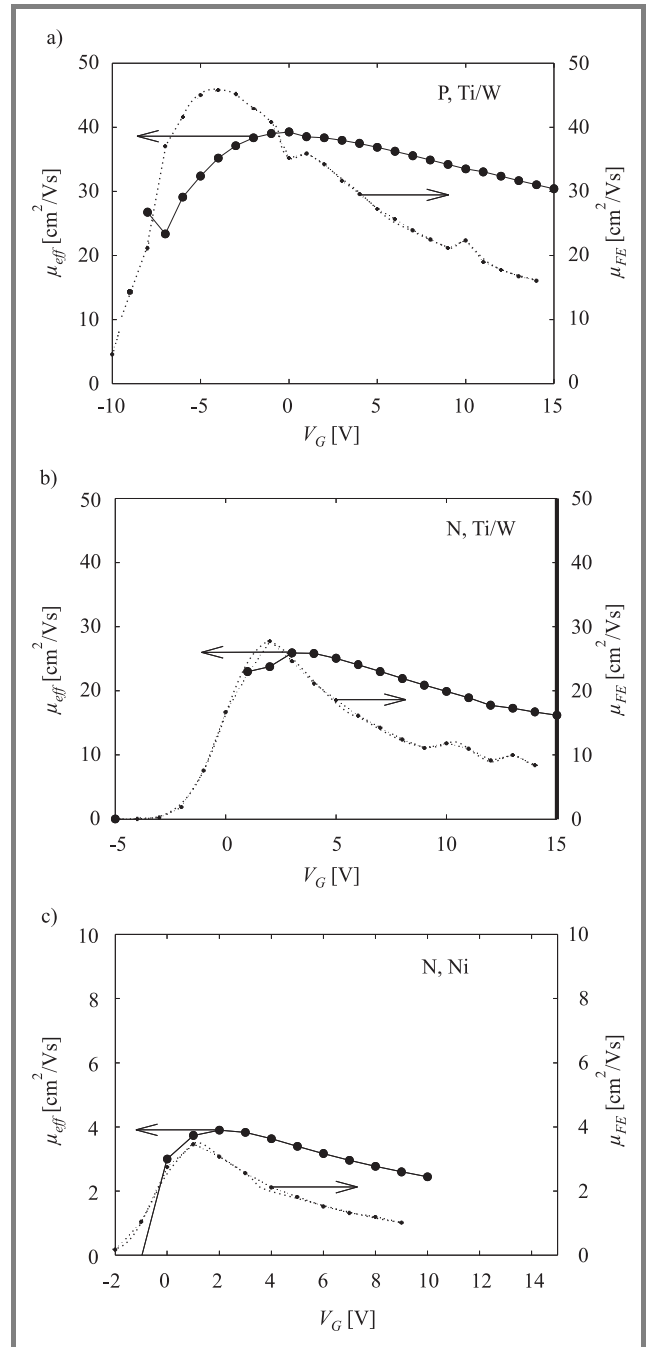


Fig. 5. Channel mobility extracted from the output characteristics of single hexagonal cell devices with P implanted source and Ti/W contact (a), with N implanted source and Ti/W contact (b) and with N implanted source and nickel silicide contact (c). Channel length $L_{ch} = 2 \mu\text{m}$.

The drain and the leakage currents scale linearly with the device size up to the maximum investigated size of $1 \times 1 \text{ mm}^2$, as in the case of lateral devices. The linear scaling of the device performance with the device

area confirms the potential of the 3C-SiC material for the fabrication of large area MOSFET devices. The blocking capability deteriorates with increasing number of cells due to increasing leakage. Large differences in leakage current were observed between devices positioned in areas containing stacking faults and in stacking fault-free areas.

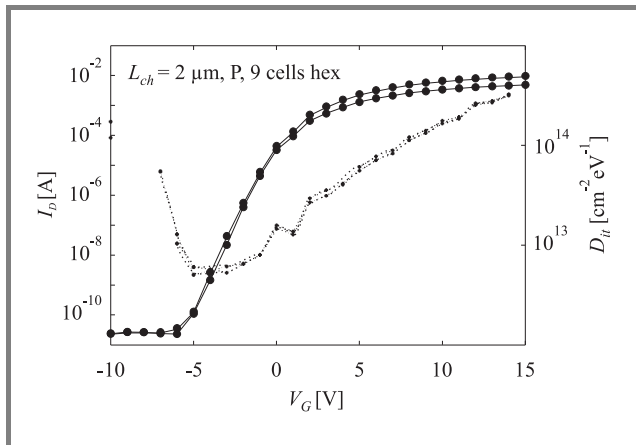


Fig. 6. Sub-threshold characteristics and calculated interface state density for a device with P implanted source at V_{DS} of 0.1 and 0.2 V.

A correlation of high leakage current and high number of extended crystal defects (mainly stacking faults) has been observed. To make full use of the performance 3C-SiC MOSFETs can offer the number of crystalline defects has to be reduced.

The values of specific on-resistance are comparable to the best values demonstrated for 4H-SiC vertical DMOSFETs.

4. Recent results

A significant improvement of the reverse blocking capability have been obtained in devices made on the material obtained recently using the so-called switch-back epitaxy (SBE) [13]. Blocking capability between 550 and 600 V has been achieved at a leakage current of 1 μ A, as shown in Fig. 7. The value of the maximum blocking voltage agrees well with the expected value of the breakdown voltage corresponding to the doping and thickness of the epitaxial drift layer.

Another optimistic finding is that the temperature dependence of the channel mobility is similar to that of the bulk material as can be seen in Fig. 8. The expected mobility dependence for the bulk material is shown as a dashed line in the figure. This is an interesting finding considering that the temperature dependence of channel mobility in hexagonal 6H- and 4H-SiC polytypes is often explained in terms of hopping conduction involving deep interface traps and that mobility increases with temperature [14].

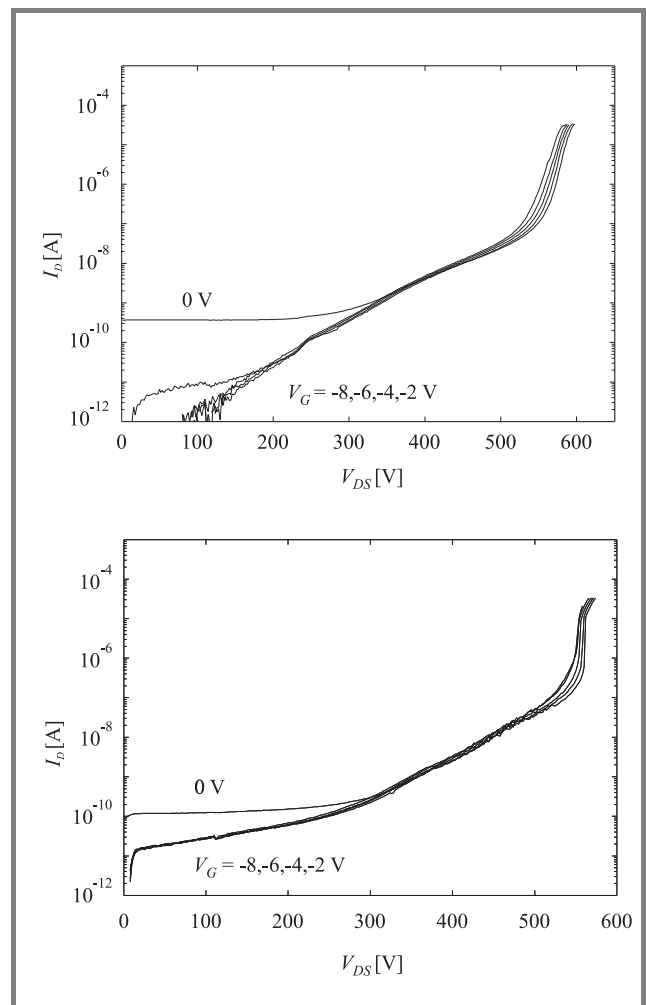


Fig. 7. Good blocking characteristics obtained on 1 cell MOSFETs made on the latest SBE material.

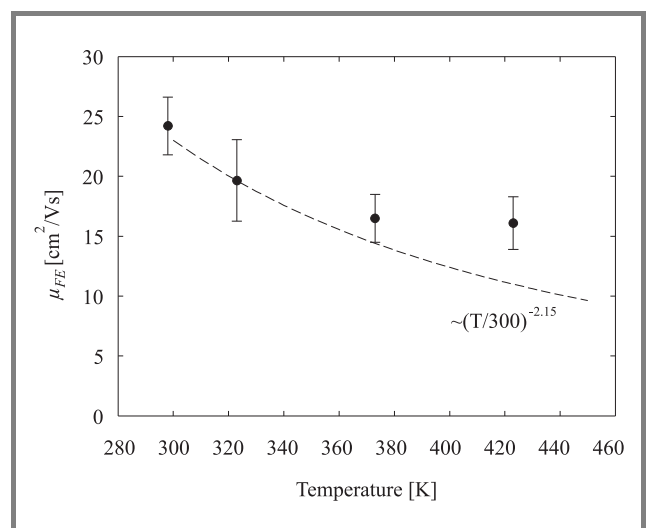


Fig. 8. Temperature dependence of the channel mobility extracted from the latest devices. The bulk mobility temperature dependence dominated by the phonon scattering is shown as a dashed line (the shown dependence holds for the 4H- and 6H- bulk material).

5. Comparison with 4H-SiC MOSFETs

The main differences in the expected performance of the 3C-SiC MOSFETs and 4H-SiC MOSFETs are illustrated in Figs. 9 and 10 [7].

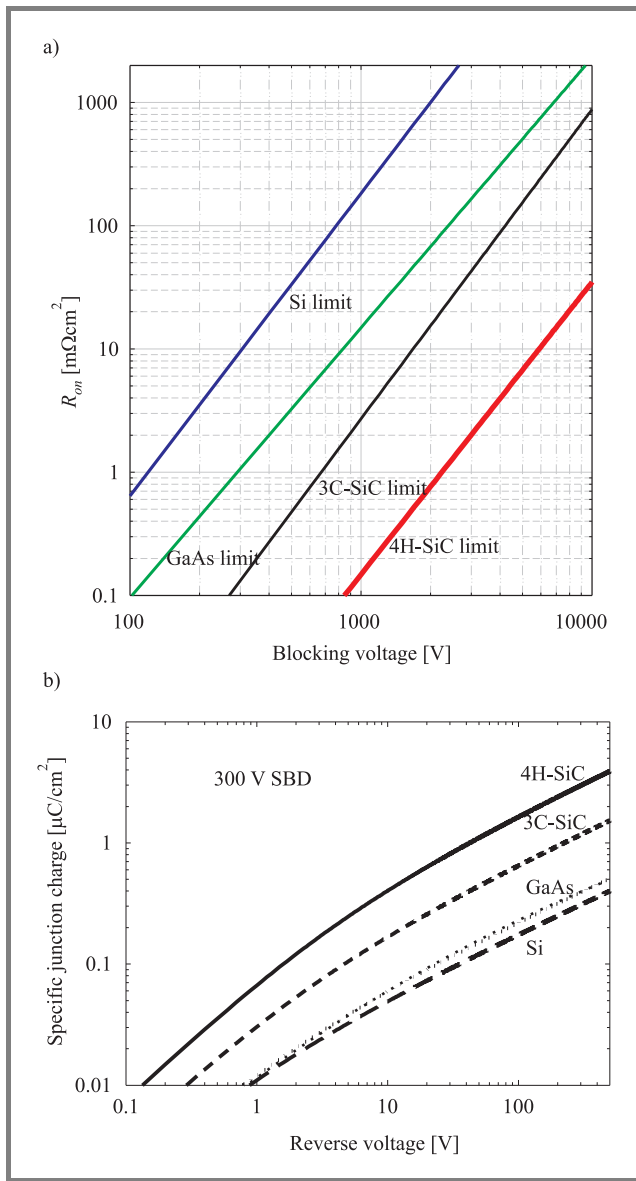


Fig. 9. The specific on-resistance, R_{on} , due to the drift region required for different blocking voltages for selected materials. This is the theoretical limit of R_{on} for the MOSFETs with homogeneously doped drift region in these materials (a). The specific value of the junction capacitance for the case of the homogeneously doped drift region for selected materials (b).

The window of possible improvement of specific resistance R_{on} in relation to silicon is smaller in the case of 3C-SiC due to the lower value of the critical electric field as shown in Fig. 9a. At the same time the lower doping required for a given blocking voltage in the case of 3C-SiC results in lower specific junction capacitance and faster devices as illustrated in Fig. 9b.

In Fig. 10 an estimation of the ultimate performance of DMOSFET devices for different values of the channel mo-

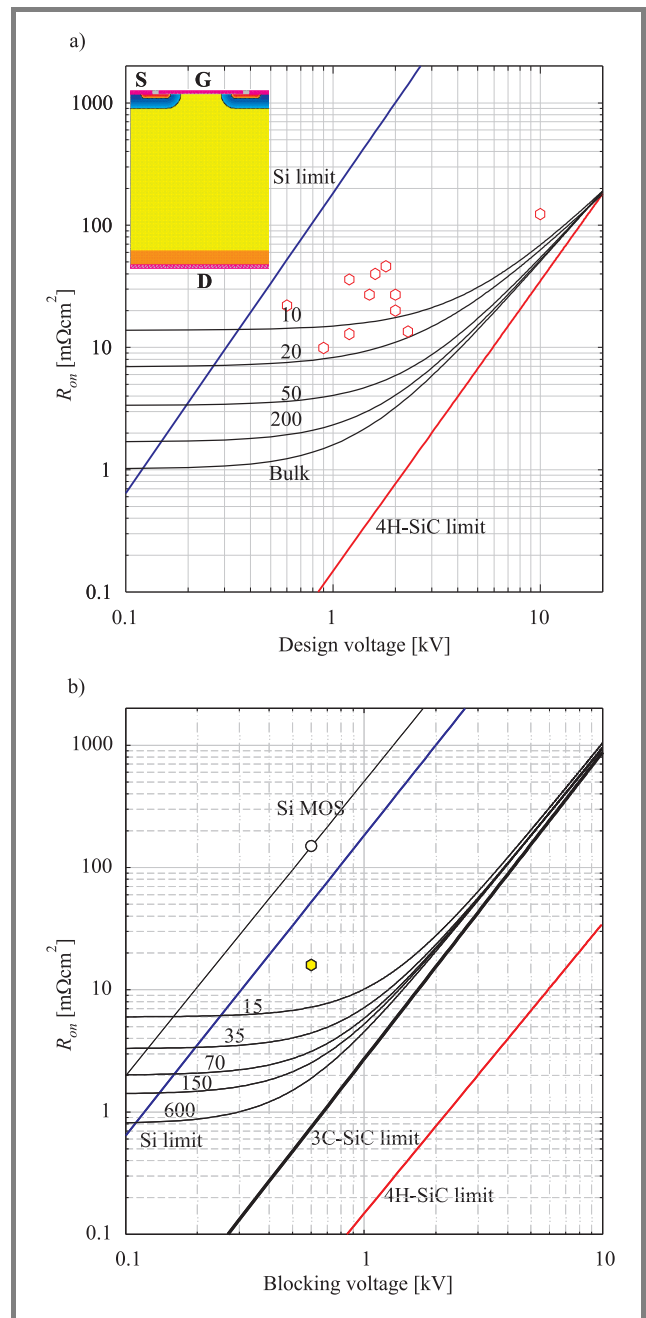


Fig. 10. A comparison of calculated and experimental data for 4H-SiC (a) and the 3C-SiC (b) DMOSFETs, respectively. The calculated data are for the ideal structure with $10 \mu m$ cell pitch and $1 \mu m$ channel length (the $1 \mu m$ line-width lithography) and for different values of channel mobility. The experimental data point for 3C-SiC corresponds to the structure with $28 \mu m$ cell pitch and $2 \mu m$ channel length ($R_{on} = 17 m\Omega cm^2$). The experimental values for 4H-SiC are values published by others.

bility is shown based on simulations together with the values of R_{on} demonstrated experimentally in the case of both 4H- (Fig. 10a) and 3C-SiC (Fig. 10b) DMOSFETs. It can

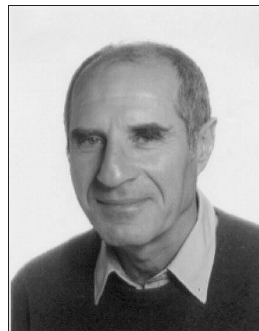
clearly be seen that the voltage range of 3C-SiC DMOS-FETs is limited to about 1200 V. The simulated structure is shown in an inset in Fig. 10a.

6. Summary and conclusions

The potential of 3C-SiC for 600 V MOSFET devices has been verified. The full blocking capability of 550–600 V has been obtained with new SBE material in the case of small devices. The leakage current was at the same time reduced by several orders of magnitude compared to the conventional material. The current capability has been shown to scale linearly with the device area. High enough values of the channel mobility (30–40 cm²/Vs) have been obtained on large-area devices. The temperature dependence of channel mobility similar to that of the bulk material has been obtained in spite of high density of interface states. The device performance is dominated by the material quality and specifically by the density and distribution of the dislocations. Further improvement is necessary concerning the density of the dislocations and interface states.

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Mietek Bakowski was born in Bydgoszcz, Poland, in 1946. He completed M.Sc. studies at the Faculty of Electronics, Warsaw University of Technology, in 1969. He received his Ph.D. and the Assistant Professor competence from Chalmers University of Technology, Gothenburg, Sweden, in 1974 and in 1981, respectively, and is

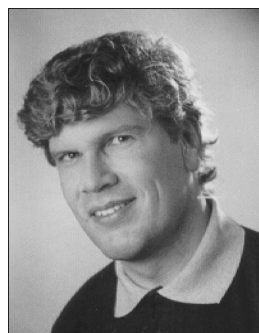
presently a Senior Scientist at Acreeo AB, Kista, Sweden. He has worked with the development of silicon bipolar and BiMOS power devices and since 1994 with the design, simulation and electrical evaluation of SiC power devices. In 2000–2003 he has been appointed Adjunct Professor at Royal Institute of Technology, KTH, Kista, Sweden.

e-mail: mietek.bakowski@acreeo.se

Acreeo AB

Electrum 236

SE-164 40 Kista-Stockholm, Sweden



Adolf Schöner was graduated in physics at the Institute of Applied Physics, University Erlangen-Nürnberg, Germany. After receiving his Ph.D. in 1994, he joined the Industrial Microelectronics Center (IMC) in Kista, Sweden, to continue working with material and processing issues of the material silicon carbide (SiC), specializing in electrical

characterization of SiC epitaxial layers and devices. At Acreeo AB he is now responsible for the development of electronic devices based on wide band gap materials and the epitaxial SiC-material development.

e-mail: adolf.schoner@acreeo.se

Acreeo AB

Electrum 236

SE-164 40 Kista-Stockholm, Sweden



Per Ericsson was graduated in 1992 and obtained a Ph.D. in solid state electronics in 1997 from Chalmers University of Technology, Gothenburg, Sweden. He worked with LD MOS RF-power device design and process integration issues at Ericsson Microelectronics be-

tween 1998 and 2000. He is now employed by Acreo AB in the Electronic Devices Group. His work mainly involves process development and device design for high power and high frequency devices based on wide band gap materials such as SiC and GaN.

e-mail: per.ericsson@acreo.se

Acreo AB

Electrum 236

SE-164 40 Kista-Stockholm, Sweden



Helena Strömberg focuses her interest on solid state electronics and has 14 years industrial experience from Ericsson Co. working with high power RF transistors and capacitors. Since 2002 she has been with Acreo AB working with process development, qualification of new processes and processing materials and fabrication of the SiC

and GaN devices. Specifically, she was involved in processing of MOSFET, MESFET and HEMT transistors and SBD and PiN rectifiers.

e-mail: helena.stromberg@acreo.se

Acreo AB

Electrum 236

SE-164 40 Kista-Stockholm, Sweden



Hiroyuki Nagasawa received the B.E., M.E., and Ph.D. degrees of engineering from Tokai University, Japan, in 1985, 1987, and 1997, respectively. After receiving M.E. degree, he worked at Toshiba Co., as a semiconductor process engineer. From 1989, he was involved in development of X-ray lithography technologies

in Hoya Co., and was mainly concerned with thin-film formation of 3C-SiC. In 2002, he joined in Hoya Advanced Semiconductor Technologies (HAST) Co. Ltd. as a chief-technology-officer (CTO). From 2006, he is conducting developments of SiC material and devices at Hoya Co. Ltd. as Senior General Manager.

e-mail: Hiroyuki_Nagasawa@sngw.rdc.hoya.co.jp

Hoya Co.

SiC Development Center

1-17-16 Tanashioda

Sagamihara 229-1125, Japan



Masayuki Abe received the B.E., M.E., and Ph.D. degrees in electrical engineering from Osaka University, Japan, in 1967, 1969 and 1973, respectively. In 1973, he joined Fujitsu Laboratories Ltd., Japan, where he was engaged in developing high-radiance LEDs, microwave HEMTs, high-speed HEMT LSIs for supercomputer,

and low-temperature poly-Si TFTs for LCD flat-panels. Since 1998, he has been engaged in developing hexagonal GaN-HEMTs, infrared image-sensor at KRI Inc., and also 3C-SiC power MOSFETs and cubic GaN-HEMTs at Hoya Co. He is currently General Manager, Hoya Co., and President, HEMTCORE and 3D-bio Co. Ltd. Doctor M. Abe is a Fellow of IEEE.

e-mail: Masayuki_Abe@sngw.rdc.hoya.co.jp

Hoya Co.

SiC Development Center

1-17-16 Tanashioda

Sagamihara 229-1125, Japan