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Capacitive Coupling And Parasitic Capacitances of Converter's – EMC

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***Summary*: The paper is dealing with some electromagnetic compatibility (EMC) problems of converters and inverters, which are utilized for feeding of electric machines and its analyzing by PSPICE program. The main attention is focused on implications of parasitic capacitance and capacitive coupling existence.**

Keywords:
electromagnetic compatibility, converter, PSPICE simulation, parasitic capacitances, capacitive coupling

1. INTRODUCTION

Development of power semiconductor parts caused vehement evolution of the power electronics branch in the last fifteen years. Main focus of the above mentioned branch is concentrated to the application of individual types of power semiconductor parts in electrical circuits, which are used for electrical energy conversion of certain parameters to different parameters. Such a circuits are called converters. During the converter functionality investigation was necessary first theoretically analyze and then practically verify the assumed activity of converter. Now we can eliminate laborious theoretical analysis and economical exacting realization by numerical computer simulation, which can also disclose the startling facts concerning of the electromagnetic compatibility (EMC) problems.

2. 4Q DC IMPULSE CONVERTER AND ITS EMC

The connection of four quadrants impulse converter, which is shown in Figure 1, is usually utilized for speed DC motor regulation. Bipolar transistors and diodes are used as power semiconductor parts in this case. Each of these parts can be changed by equivalent parallel combination of its resistor and capacitor in the cutt-off condition. As consequence of the fact that circuit is non-linear so the theoretical analyzing should be very difficult. If we will utilize numerical computer simulation by PSPICE program then we can do it very easy.

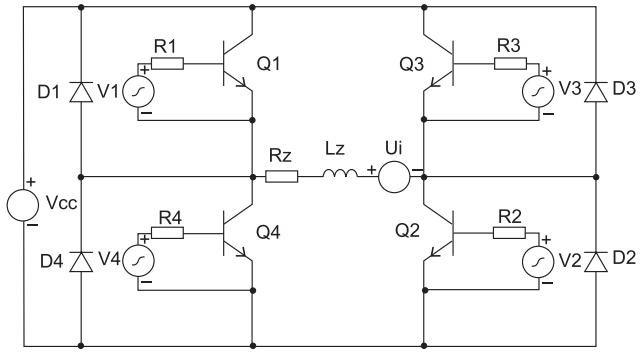


Fig. 1. 4Q DC impulse converter

First, it is necessary to write the input file with respect to the equivalent electrical scheme. After PSPICE program solving we can obtain transient curves of circuit currents and voltages. The input file example for investigated circuit is shown in following:

```
Four quadrants impulse converter
Vcc 1 0 DC 100
D1 5 1 KY195
D2 0 12 KY195
D3 12 1 KY195
D4 0 5 KY195
Q1 1 2 5 KD606
Q2 12 13 0 KD606
Q3 1 9 12 KD606
Q4 5 6 0 KD606
R1 2 3 5
R2 14 13 5
R3 10 9 5R4 7 6 5
Rz 5 16 10
Lz 16 17 2m
Vi 17 12 DC 5
V1 3 5 PULSE(0 15 0 0 0 0.5m 1m)
V2 14 0 PULSE(0 15 0 0 0 0.5m 1m)
V3 10 12 PULSE(0 15 0.7m 0 0 0.3m 1m)
V4 7 0 PULSE(0 15 0.7m 0 0 0.3m 1m)
.MODEL KD606 NPN
.MODEL KY195 D CJO=800p
.LIB C:\SPICE1\ASIM\PARTS\NOM.LIB
.TRAN 10n 5m 0 1u
.OPTIONS ITL4=500 ITL5=0 reltol=0.01
.PROBE
.END
```

Simulation results of transistor and load currents and voltages are pictured in Figure 2. From the curves one can see that during first part of the switching period is open the first diagonal of transistors and on the rest time is open the second one. The dead time during diagonal switching is necessary from the reason of short circuit existence possibility of two transistors connected in series in one-branch. Such short circuit existence can be leading to the destruction of the both transistors. The dead time section is not visible in picture in due to existence of load inductance, which causing

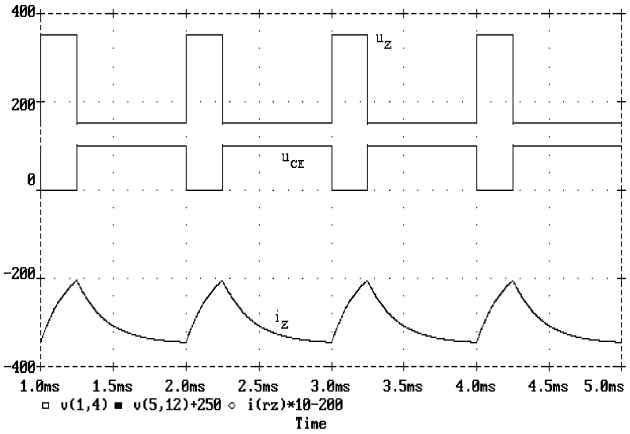


Fig. 2. Continuous current

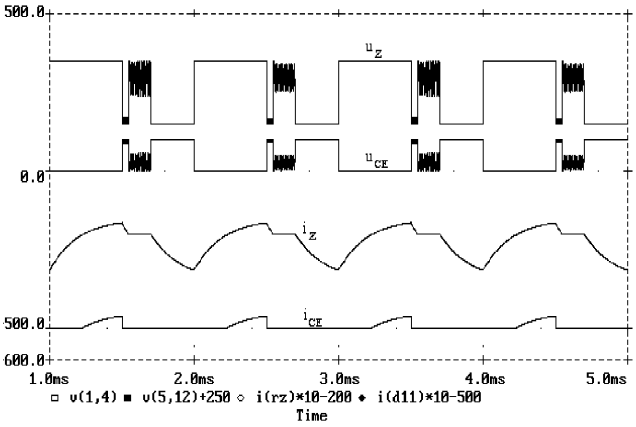


Fig. 3. Interrupted current

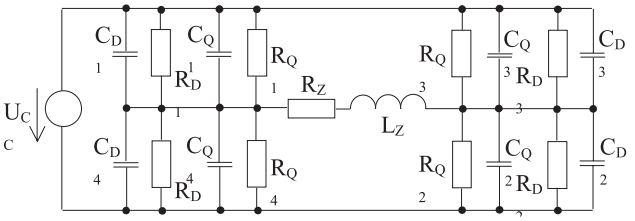


Fig. 4. Equivalent electrical scheme

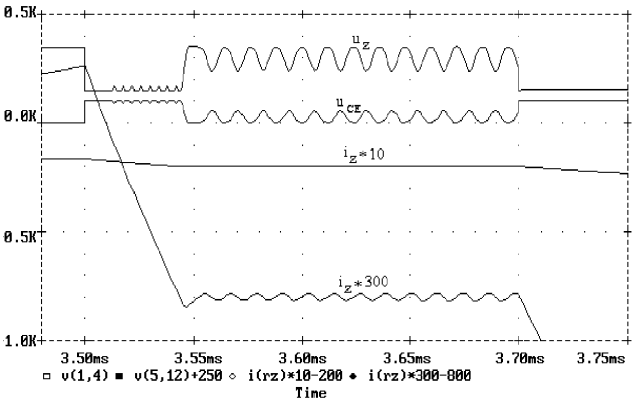


Fig. 5. Detail of oscillation process

that the current is leading through backward connected diodes and this fact exactly defines the load voltage. If we will change the ratio of the open time of the first and second diagonals in the next step, then we will change also the average value of the converter output voltage and such a way the speed of DC motor, too.

Described situation is drawing in Figure 3. From figure is evident that load current has the zero value in the particular part of period. It is resulting to the conclusion that in this time must be zeroing also load voltage by Ohm's law. However, from picture we can see that above mentioned voltage is not zero and also it is very undulating.

This fact has very unfavorable effect on the used power semiconductor parts and quality of converter electromagnetic compati-bility. Simple explanation of this fact is possible to do by next figure – Figure 4, which is showing the equivalent electrical scheme of described converter at the moment when the load current is equal to zero. Each of the power semiconductor parts can be changed by equivalent parallel combination of its resistor and capacitor in the cutt-off condition. $C_{Q1} = C_{Q2} = C_{Q3} = C_{Q4} = C_Q = 1200$pF, $C_{D1} = C_{D2} = C_{D3} = C_{D4} = C_D = 800$pF, $R_{Q1} = R_{Q2} = R_{Q3} = R_{Q4} = R_Q = 1330\Omega$, $R_{D1} = R_{D2} = R_{D3} = R_{D4} = R_D = 5000\Omega$, $R_Z = 10\Omega$, $L_Z = 2$mH.

Parasitic transistor and diode capacitances together with the load inductance create the resonance circuit, which is easily inclined to the oscillation. Resonant frequency is possible to state from loop impedance if its imaginary part will be equal to zero.

$$\dot{Z} = R_Z + j\omega L_Z + 2.\frac{\left(\frac{R_Q.R_D}{R_Q+R_D}\right).\left(\frac{-j}{\omega.(C_Q+C_D)}\right)}{\left(\frac{R_Q.R_D}{R_Q+R_D}\right)+\left(\frac{-j}{\omega.(C_Q+C_D)}\right)} \quad (1)$$

$$Im(\dot{Z}) = \omega L_Z - 2.\frac{\left(\frac{R_Q.R_D}{R_Q+R_D}\right)^2.\left(\frac{1}{\omega.(C_Q+C_D)}\right)}{\left(\frac{R_Q.R_D}{R_Q+R_D}\right)^2+\left(\frac{1}{\omega.(C_Q+C_D)}\right)^2} = 0 \quad (2)$$

$$f_r = \frac{\sqrt{\frac{2}{L_Z.(C_Q+C_D)} - \frac{1}{\left(\frac{R_Q.R_D}{R_Q+R_D}\right)^2.(C_Q+C_D)^2}}}{2.\pi} = 83272.9\text{Hz} \quad (3)$$

Detail imagination about transistor voltage, load voltage and load current, which is three hundred times magnified, we can obtain from Figure 5.

Measured waveforms are displayed in Figure 6 and Figure 7. The oscillation frequency is depending mainly on the transistor capacitance value. If the best parts with small parasitic capacitance will be used then the higher oscillation frequency and the worse EMC will be. It is evident that the

oscillation period takes 12 μs and so the converter is operating as transmitter with the frequency 83.272 kHz.

3. CONVERTERS PARASITIC CAPACITANCE CALCULATION

Capacitive coupling is typical for galvanically separated circuit nodes, between which exists mutual influence by individual intensity vectors $\bar{E}_i$ of electrostatic field, Figure 8. In such case the influence value is given by rising or decreasing slope of potential in described nodes, electrode area dimensions, space dielectric property and wire geometrical ordering in described nodes.

For predictive investigation of capacitive coupling implications we will come out from well-known Maxwell's equations valid for electrostatic field:

$$rot\ \bar{E} = 0 \tag{4}$$

$$div\ \bar{D} = \rho \tag{5}$$

where the vector of electric induction $\bar{D}$ is given as:

$$\bar{D} = \varepsilon.\bar{E} \tag{6}$$

Based on physics knowledge we can state the force acting between two elementary charges Q_1 and Q_2.

$$\bar{F} = \frac{1}{4\pi\varepsilon_0}\int_{S_1}\int_{S_2}\frac{\bar{r}_{12}}{r_{12}^3}.\rho_1.dS_1.\rho_2.dS_2 \tag{7}$$

where $p_1 = dQ_1/dS_1$ and $p_2 = dQ_2/dS_2$. One element $\bar{E}_{1i}$ of electrostatic intensity vector $\bar{E}_1$ can be expressed as:

$$\bar{E}_{1i} = \frac{\bar{F}_{1i}}{Q_{2i}} = \frac{\frac{Q_{2i}}{4\pi\varepsilon_0}\int_{S_1}\frac{\bar{r}_{12}}{r_{12}^3}.\rho_1.dS_1}{Q_{2i}} = \frac{1}{4\pi\varepsilon_0}\int_{S_1}\frac{\bar{r}_{12}}{r_{12}^3}.\rho_1.dS \tag{8}$$

Total electrostatic intensity vector $\bar{E}$ at investigated place will be given as sum of vectors $\bar{E}_1$ and $\bar{E}_2$ induced by both charged volumes. Existing voltage between these volumes is possible to express by next equation.

$$U_{12} = \varphi_1 - \varphi_2 = \int_1^2 \left(\bar{E}_1 + \bar{E}_2\right)\ .\ d\bar{r}_{12} =$$

$$= \int_1^2 \left(\frac{1}{4\pi\varepsilon_0}\int_{S_1}\frac{\bar{r}_{12}}{r_{12}^3}.\rho_1.dS_1 + \frac{1}{4\pi\varepsilon_0}\int_{S_2}\frac{\bar{r}_{21}}{r_{21}^3}.\rho_2.dS_2 \right).d\bar{r}_{12} \tag{9}$$

If we will suppose that $Q_1 = Q$ and $Q_2 = -Q$, so we can to write the equation for created capacitance.

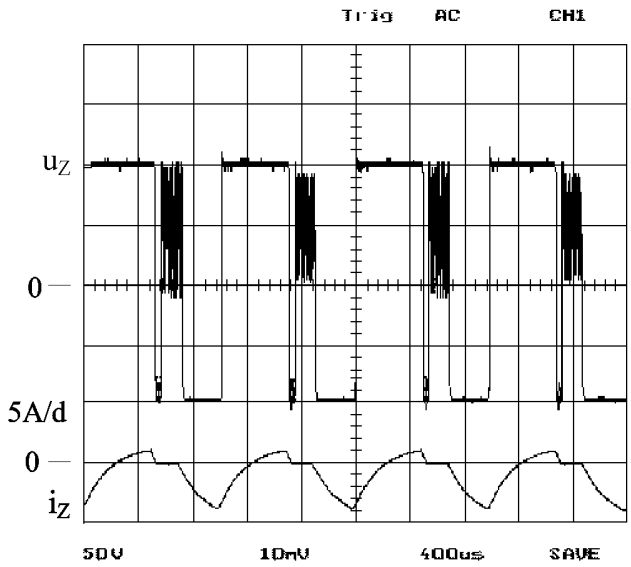


Fig. 6. Measured waveforms of load voltage u_Z and current i_Z

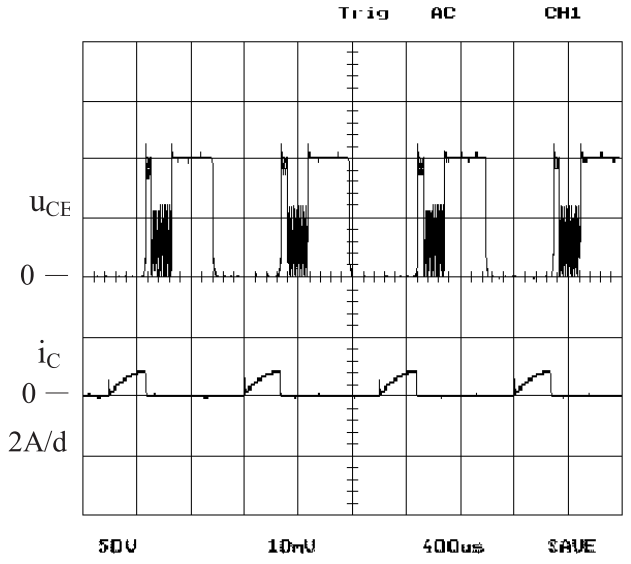


Fig. 7. Measured waveforms of transistor voltage u_{CE} and current i_C

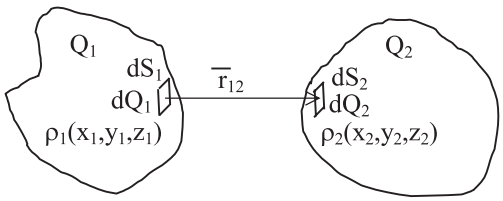


Fig. 8. Capacitive coupling

$$C_{12} = \frac{Q}{U_{12}} \tag{10}$$

In many cases the engineers must state mutual parasitic capacitance of two wires, which have optional routing as it is shown in Figure 9. The analytical expression of resulting capacitance is very difficult in such case and in due to they

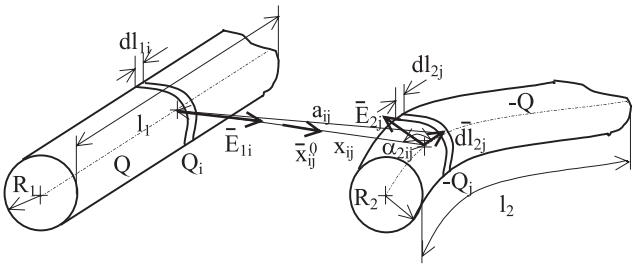
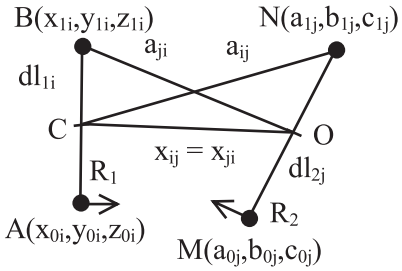


Fig. 9. Capacitive coupling



C((x1i-x0i)/2,(y1i-y0i)/2,(z1i-z0i)/2)
O((a1j-a0j)/2,(b1j-b0j)/2,(c1j-c0j)/2)

Fig. 10. 3-D Cartesian system

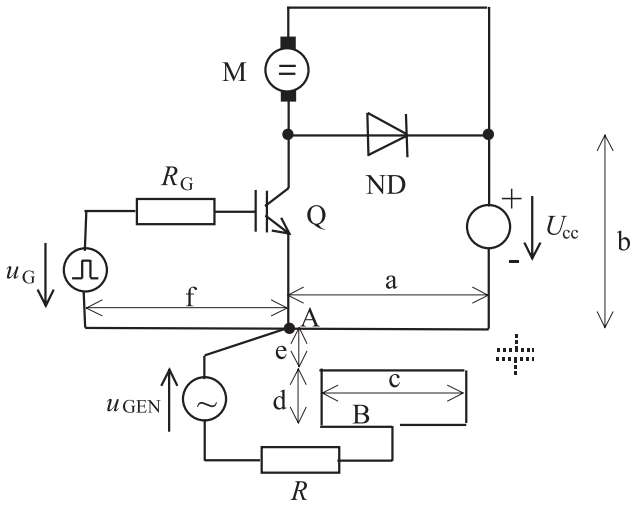


Fig. 11. Investigated circuit

are utilizing analytic-numerical method consist in differential form utilizing. For all that the following basic assumption must be done.

$$l_1 = \sum_{i=1}^{m\to\infty} dl_{1i}, \quad l_2 = \sum_{j=1}^{k\to\infty} dl_{2j} \tag{11}$$

The potential at the second wire place we can express by next equation.

$$\varphi_2 = \sum_{i=1}^{m} \frac{Q_i}{2\pi\varepsilon dl_i}.ln\frac{x_{ij}-R_2}{R_1}.sin(\alpha_{2ij}) =$$

$$= \sum_{i=1}^{m} \frac{Q_i}{2\pi\varepsilon dl_i}.ln\frac{x_{ij}-R_2}{R_1}.\sqrt{1-\left(\frac{x_{ij}^2+\left(\frac{dl_{2j}}{2}\right)^2-a_{ij}^2}{x_{ij}.dl_{2j}}\right)^2} \tag{12}$$

Similar we can state the potential for first wire position.

$$\varphi_1 = \sum_{j=1}^{n} \frac{-Q_j}{2\pi\varepsilon dl_j}.ln\frac{x_{ji}-R_2}{R_1}.sin(\alpha_{1ji}) =$$

$$= \sum_{j=1}^{n} \frac{-Q_j}{2\pi\varepsilon dl_j}.ln\frac{x_{ji}-R_2}{R_1}.\sqrt{1-\left(\frac{x_{ji}^2+\left(\frac{dl_{1i}}{2}\right)^2-a_{ji}^2}{x_{ji}.dl_{1i}}\right)^2} \tag{13}$$

Voltage between both wires will be given as:

$$U = \frac{Q}{2\pi\varepsilon}\left(\sum_{i=1}^{m} \frac{ln\frac{x_{ij}-R_2}{R_1}.\sqrt{1-\left(\frac{x_{ij}^2+\left(\frac{dl_{2j}}{2}\right)^2-a_{ij}^2}{x_{ij}.dl_{2j}}\right)^2}}{dl_{1i}} + \right.$$

$$\left. + \sum_{j=1}^{n} \frac{ln\frac{x_{ji}-R_2}{R_1}.\sqrt{1-\left(\frac{x_{ji}^2+\left(\frac{dl_{1i}}{2}\right)^2-a_{ji}^2}{x_{ji}.dl_{1i}}\right)^2}}{dl_{2j}}\right) \tag{14}$$

Searched value of parasitic capacitance is possible to state by Coulomb's law.

$$C_{12}=\frac{2\pi\varepsilon}{\left(\sum_{i=1}^{m}\frac{\ln\frac{x_{ij}-R_2}{R_1}\cdot\sqrt{\left(1-\frac{\left(x_{ij}^2+\left(\frac{dl_{2j}}{2}\right)^2-a_{ij}^2\right)^2}{x_{ij}dl_{2j}}\right)^2}}{dl_{1i}}+\sum_{j=1}^{m}\frac{\ln\frac{x_{ij}-R_2}{R_1}\cdot\sqrt{\left(1-\frac{\left(x_{ji}^2+\left(\frac{dl_{1j}}{2}\right)^2-a_{ji}^2\right)^2}{x_{ji}dl_{2j}}\right)^2}}{dl_{2i}}\right)} \quad (15)$$

Expressing of individual equation members for 3-D Cartesian system shown in Figure 10 is possible to do by the following equations.

$$dl_{1i}=\sqrt{\left(x_{1i}-x_{0i}\right)^2+\left(y_{1i}-y_{0i}\right)^2+\left(z_{1i}-z_{0i}\right)^2} \quad (16)$$

$$dl_{2j}=\sqrt{\left(a_{1j}-a_{0j}\right)^2+\left(b_{1j}-b_{0j}\right)^2+\left(c_{1j}-c_{0j}\right)^2} \quad (17)$$

$$a_{ij}=\sqrt{\left(a_{1j}-\left(x_{1i}-x_{0i}\right)/2\right)^2+\left(b_{1j}-\left(y_{1i}-y_{0i}\right)/2\right)^2+\left(c_{1j}-\left(z_{1i}-z_{0i}\right)/2\right)^2} \quad (18)$$

$$a_{ji}=\sqrt{\left(x_{1i}-\left(a_{1j}-a_{0j}\right)/2\right)^2+\left(y_{1i}-\left(b_{1j}-b_{0j}\right)/2\right)^2+\left(z_{1i}-\left(c_{1j}-c_{0j}\right)/2\right)^2} \quad (19)$$

$$x_{ij}=x_{ji}=\sqrt{\left(\left(a_{1j}-a_{0j}\right)/2-\left(x_{1i}-x_{0i}\right)/2\right)^2+\left(\left(b_{1j}-b_{0j}\right)/2-\left(y_{1i}-y_{0i}\right)/2\right)^2+\left(\left(c_{1j}-c_{0j}\right)/2-\left(z_{1i}-z_{0i}\right)/2\right)^2} \quad (20)$$

Only such wire length elements dl_{1i} and dl_{2j} must be taken for total parasitic capacity calculation, which are fulfilling the next conditions.

$$x_{ji}^2+\left(\frac{dl_{1i}}{2}\right)^2=\left(x_{1i}-\left(a_{1j}-a_{0j}\right)/2\right)^2+ \\ +\left(y_{1i}-\left(b_{1j}-b_{0j}\right)/2\right)^2+\left(z_{1i}-\left(c_{1j}-c_{0j}\right)/2\right)^2 \quad (21)$$

$$x_{ij}^2+\left(\frac{dl_{2j}}{2}\right)^2=\left(a_{1j}-\left(x_{1i}-x_{0i}\right)/2\right)^2+ \\ +\left(b_{1j}-\left(y_{1i}-y_{0i}\right)/2\right)^2+\left(c_{1j}-\left(z_{1i}-z_{0i}\right)/2\right)^2 \quad (22)$$

Correctness verification of obtained results can be done by simulation and measuring. For this purpose is possible to utilize the connection of DC impulse converter shown in Figure 11.

We will try to state the value of parasitic capacitance between the node A of impulse converter and node B of sense loop. Space dielectric material is created by air. Geometrical dimensions of investigated circuits are a = f = 0.2 m, b = 0.3m, c = 0.1m, d = 0.05m, e = 0.00135m. Wires are made from cooper with the radius R = 0.0006m. Based on above mentioned parameters it is possible to calculate the individual partial parasitic capacitances.

$$C_{ace}=\frac{1}{\frac{1}{2\pi\varepsilon_0 a}\ln\frac{e-R}{R}+\frac{1}{2\pi\varepsilon_0 c}\ln\frac{e-R}{R}}=16.63\,pF \quad (23)$$

$$C_{aced}=\frac{1}{\frac{1}{2\pi\varepsilon_0 a}\ln\frac{(d+e)-R}{R}+\frac{1}{2\pi\varepsilon_0(c-0{,}001)}\ln\frac{(d+e)-R}{R}}=0.8306pF \quad (24)$$

$$C_{fce}=\frac{1}{\frac{1}{2\pi\varepsilon_0 a}\ln\frac{\sqrt{e^2+a^2}-R}{R}+\frac{1}{2\pi\varepsilon_0 c}\ln\frac{\sqrt{e^2+a^2}-R}{R}}=0.6391pF \quad (25)$$

$$C_{fced}=\frac{1}{\frac{1}{2\pi\varepsilon_0 a}\ln\frac{\sqrt{(d+e)^2+a^2}-R}{R}+\frac{1}{2\pi\varepsilon_0(c-0{,}001)}\ln\frac{\sqrt{(d+e)^2+a^2}-R}{R}}=0.6314\,pF \quad (26)$$

$$C_{bda-c}=\frac{1}{\frac{1}{2\pi\varepsilon_0\frac{b}{2}}\ln\frac{\sqrt{\left(\frac{b}{4}+e+\frac{d}{2}\right)^2+\left(\frac{a}{2}-\frac{c}{2}\right)^2}-R}{R}+\frac{1}{2\pi\varepsilon_0 d}\ln\frac{\sqrt{\left(\frac{b}{4}+e+\frac{d}{2}\right)^2+\left(\frac{a}{2}-\frac{c}{2}\right)^2}-R}{R}}=0.3989pF \quad (27)$$

$$C_{bda+c}=\frac{1}{\frac{1}{2\pi\varepsilon_0\frac{b}{2}}\ln\frac{\sqrt{\left(\frac{b}{4}+e+\frac{d}{2}\right)^2+\left(\frac{a}{2}+\frac{c}{2}\right)^2}-R}{R}+\frac{1}{2\pi\varepsilon_0 d}\ln\frac{\sqrt{\left(\frac{b}{4}+e+\frac{d}{2}\right)^2+\left(\frac{a}{2}+\frac{c}{2}\right)^2}-R}{R}}=0.3658pF \quad (28)$$

$$C=C_{ace}+C_{aced}+C_{fce}+C_{fced}+2.C_{bda-c}+ \\ +2.C_{bda+c}=20.26\,pF \quad (29)$$

Based on calculated capacitance the simulation analyze in PSPICE program is possible to do now by circuit connection shown in Figure 12. Parameters of individual elements are U_{CC} = 70 V, R_Z = 11.66 Ω, L_Z = 400 μH, R = 1 MΩ, u_{GEN} = 2 sin (ωt) V. Simulation results for frequency f = 10 kHz are pictured in Figure 13.

The same output values obtained by simulation, but for frequency f = 50 kHz are shown in Figure 14. Measured values of u_{CE}, u_{GEN} and u_C are shown in next figures Figure 15 till to Figure 18.

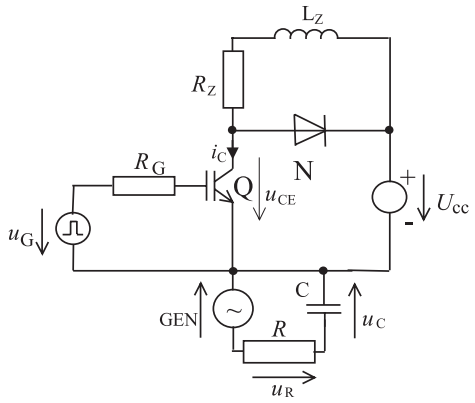


Fig. 12. Simulation circuit

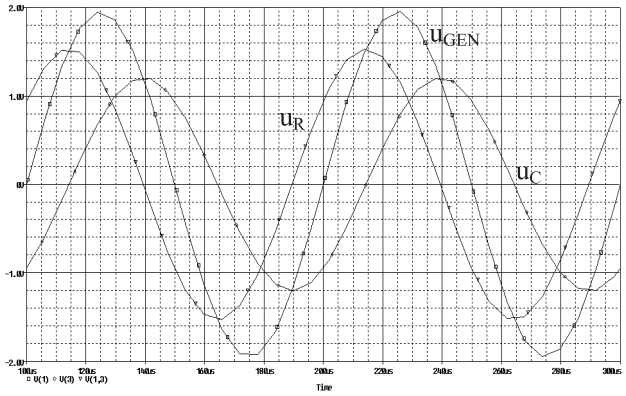


Fig. 13. Simulation results for f = 10 kHz

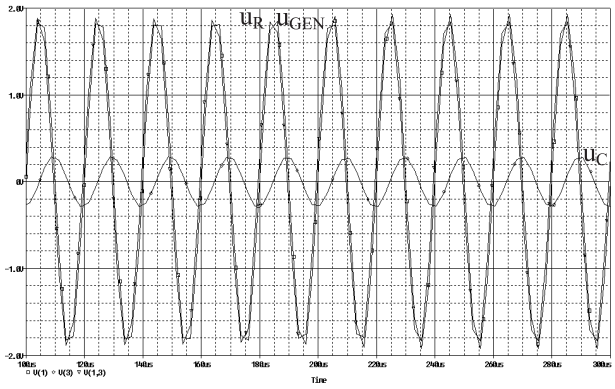


Fig. 14. Simulation results for f = 50 kHz

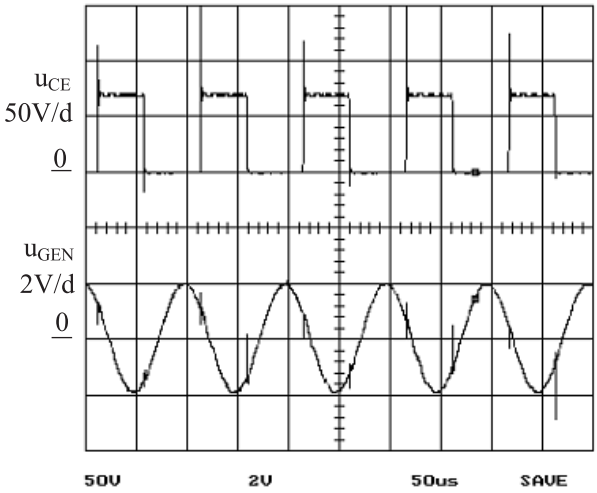


Fig. 15. Measured results for f = 10 kHz

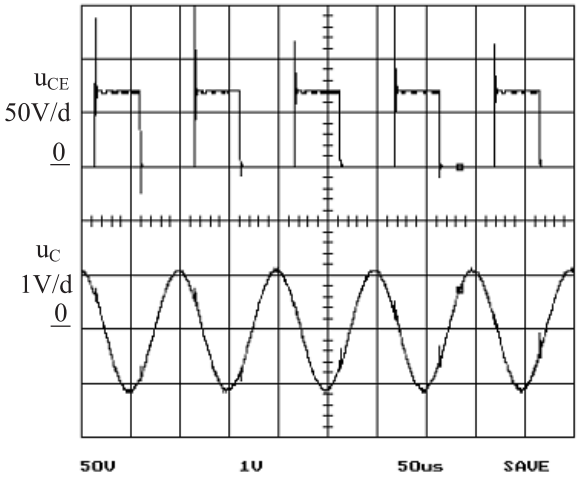


Fig. 16. Measured results for f = 10 kHz

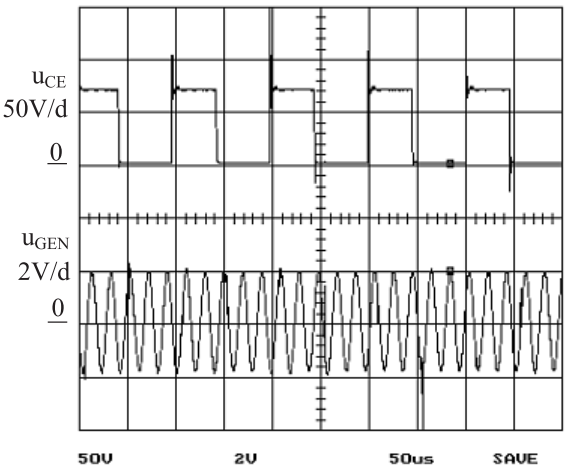


Fig. 17. Measured results for f = 50 kHz

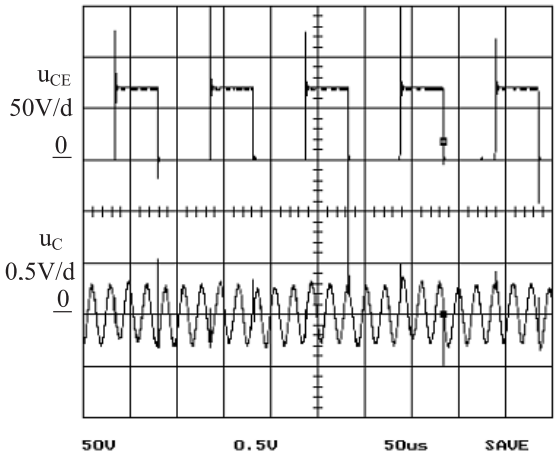


Fig. 18. Measured results for f = 50 kHz

By comparing of simulated and measured results one can see that obtained results are identical and it means that derived analytical formula for parasitic capacitance calculation is valid.

In due to additional verification requirement the same problem is possible to analyze also by numerical, finite element simulation method of electrostatic field. Obtained result is shown in Figure 19.

From data window is possible to state that the value of electrical flux between both nodes is $5.4357.10^{-12}$ C. Based on the program property we must multiple this value by value of wires perimeter $l = 2.p.R = 2.p.0.6 = 3.76$ mm. Total electrical flux is then 20.4382 C. In due to fact that the voltage between nodes have value 1V, so the resulting parasitic capacitance is C = 20.4382 pF.

By comparing of all results we can state that difference is only 0.879% and it means that the correctness of derived formula for parasitic capacitance calculation is satisfy.

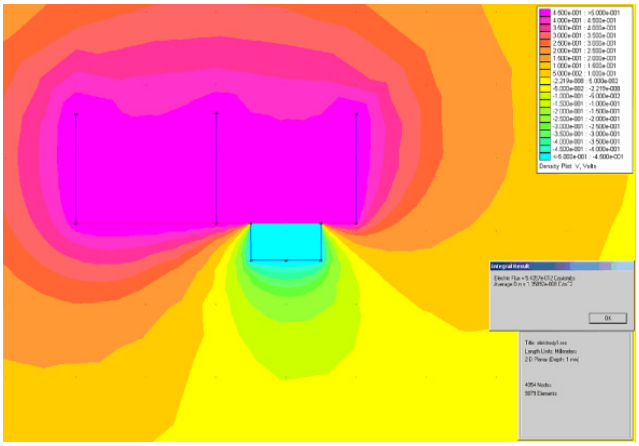


Fig. 19. Finite element method simulation

4. CONCLUSION

Performed analyzes indicates that not only large current switching frequency has the main influence on the converter's EMC but equally important is also the switch off state with small parasitic resonant load current.

Obtained formula for parasitic capacitance calculation enabling predictive EMC investigation. Although such converter capacitances seem to be negligible so performed analyze show to us that it can have important influence. Mainly in the case when the switching frequency is high or one of the both nodes belong to the circuit with great impedance. It is obviously in the case of capacitive coupling existence between CMOS integrated circuits and power converter circuit when EMC quality can be very fundamental for right equipment operation.

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