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Three-level Modulation Techniques to Reduce Instantaneous Common Mode Voltage in Induction Machines

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Summary: **Problems on inverter motor drives such as bearing currents are introduced due to common mode voltages. Different solutions are proposed on literature, for two-level or multilevel inverter. Instantaneous zero common mode voltage by using a three-level inverted could be achieved. This paper proposes a commutation strategy that allows zero common mode voltage by using medium vectors, and also a new representation as a plane on the commutation space is defined which is called zero common mode voltage plane. On this defined plane, every turning vector fulfil this property. Simulations and experimental results clearly show method's efficiency.**

Keywords:
common mode voltages, multilevel inverter, drive systems

1. INTRODUCTION

Inverter-operated drive systems allow variable speed and therefore energy saving for variable speed operation when compared with conventional drive systems. However, at low switching frequencies, these drive systems suffer from additional losses for rated motor speed, additional noise and torque ripples and have poor dynamic performance. Motor operation with higher switching frequencies can reduce the additional losses, additional noise and torque ripples and increase the drive dynamics. Due to fast switching, new phenomena have come up that had not been of influence before, but come into it effect. Fast switching IGBT-inverter operated motors are submitted to increase winding stress, increased EMI-problems as well as additional ground and bearing currents.

With the trend of motor drives improvement, multilevel inverter appears on 1975 [1]. By having the opportunity to operate at different voltage levels allows to decrease the effect of some of the classical inverter problems such as dv/dt or EMI [1–5]. Furthermore by choosing right commutation strategies has been demonstrated a clear common mode voltage reduction. Also common mode could be reduced on two levels inverter by choosing proper commutation technique, despite of it could be reduced but never could disappear in these two levels inverters.

One of the software approaches for two-level inverter control is to use non-zero switching states for inverter control [5–6]. The approach presented in [5] doesn't invoke any zero switching state to reduce the common-mode voltage. However, the linear modulation range is reduced and thereby reducing the range of speed (torque) control. Furthermore the instantaneous common mode voltage on a two level inverter never will be zero.

Case of three-level inverters will be different too, several papers [7–11] clearly introduce and demonstrate the possibility of instantaneous zero common mode voltage. It is possible by using determined vectors on commutation. [7] shows a clear Zero-sequence currents modeling and presents a clearly guide to understand common mode effects and possible mitigation.

[8–10] introduce the concept of null space vectors to kink two level and multilevel modulation. And demonstrate the clear decrease of common mode effects by optimizing space vector switching sequences. But not an instantaneous zero common mode is clearly demonstrated, however it is well introduced.

[11] clearly shown proper approach for get an instantaneous zero common mode by using multilevel medium vectors. On this paper those hypothesis is assumed and demonstrated, three level inverter has been simulated with proper commutation for assure the zero common mode voltages.

In [12] the new conception of multilevel vectors representation is shown, by representing different commutation states as points on the space. In case of three-level inverter a cube could be defined. In this paper new plane has been defined as the zero common mode plane. Where every turning vector contained on this plane fulfill those property. Simulation and experimental results clearly demonstrate method's efficiency.

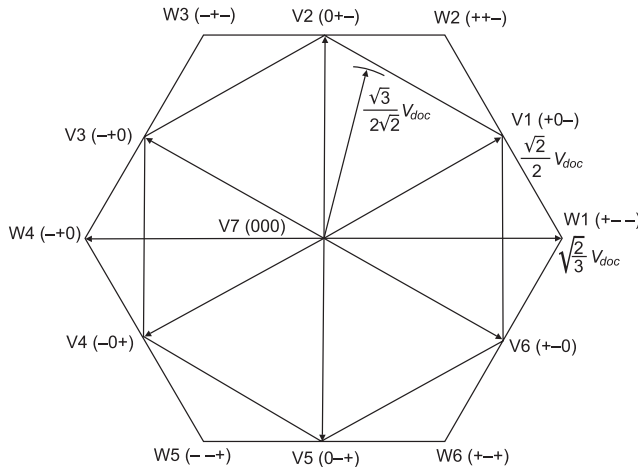

Fig. 1. Commutation hexagon "V" vectors produces no common mode

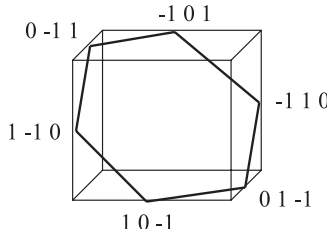

Fig. 2. Zero common mode voltage plane

2. PROPOSED APPROACH

Different vectors must be used to avoid common mode voltage in a tree level modulation. Common mode voltage is defined as the addition of 3 line voltages. For a equilibrate source V0 must be zero, standard grid supply is a clear example. In multilevel converters, especially in diode clamped typology is possible to design commutation strategies using specified vectors in order to avoid common mode. Using medium vectors guarantied the 3 lines voltages addition equal to zero which means no common mode voltages. Figure 1 shows the spatial distribution of these vectors.

These vectors define a plane into a cube defined for the hall possible vectors three level converter. In those plane a rotating vector could be defined with the property of zero value in common mode voltage. Figure 2 shows the plane defined as a zero common mode. Every vector contained on this plane must have this property.

In Figure 1 the commutation hexagon can be seen. The vectors whose name starts by 'V' are those that don't produce common mode voltages, and consequently the ones that have been used for this modulation.

The generation of the sinusoidal voltage is made by using a turning reference vector. This vector crosses through pass the different sextants of the hexagon. In each one there are commutations by using two adjacent vectors, those that define the sextant. The time of each one have to be applied is determined by the voltage signal's medium value, but is easier to understand the vectorial decomposition in the adjacent vectors axis represented in Figure 3.

The medium value obtained with the combination of the vectors should be the same of the medium values of the reference voltage. Consequently the result of the decomposition shall fulfill the following expression (1).

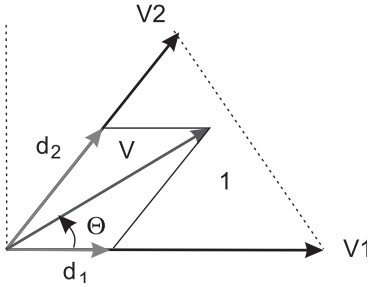

Fig. 3. Duty ratio deduction d_1 & d_2

$$V_{ref}T = V_1T_1 + V_2T_2 + V_0T_0 \tag{1}$$

where:
— T_1 – Time for vector 1
— T_2 – Time for vector 2
— T_0 – Time for the null vector
— T – Sampling period

Each of these times can be get using the following equations

$$T_2 = \frac{V_{ref}T\,sin\left(\alpha_{ref}\right)}{V_2\,sin\left(\frac{\pi}{3}\right)} \tag{2}$$

$$T_1 = \frac{V_{ref}T\,cos\left(\alpha_{ref}\right) - V_2T_2\,cos\left(\frac{\pi}{3}\right)}{V_1} \tag{3}$$

$$T_0 = T - T_1 - T_2 \tag{4}$$

No matter which sextant the system is working into, it is just needed to work in the 60 degrees reference frame in order to get easily the different times.

3. SIMULATION MODEL

The developed model used was a simplified hardware structure, though things such as DC voltage control, or commutation losses were not introduced. Focus of the paper was to implement a modulation using a specific type of vectors. Structure used has been the one described below in the following picture (Fig. 4.).

The final result of building the structure seen above in Simulink blocks is the following (Fig. 5.).

3.1. Commutation

Every vector that has been described at Figure 5 carries out the state of three different legs. So in each commutation period, nine different switches have to receive information about its state, and some of them will have to change it.

In the developed model a function has been built in order to translate the vector information into individual Boolean variable for the different switches,

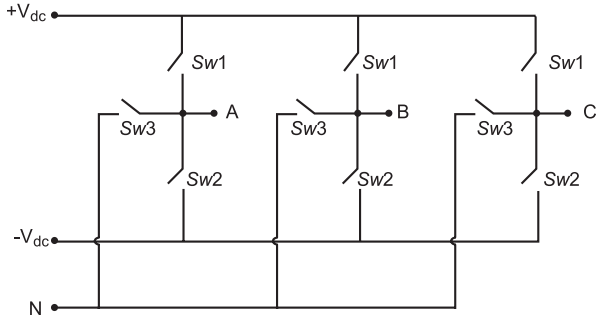

Fig. 4. Simplified three level inverter

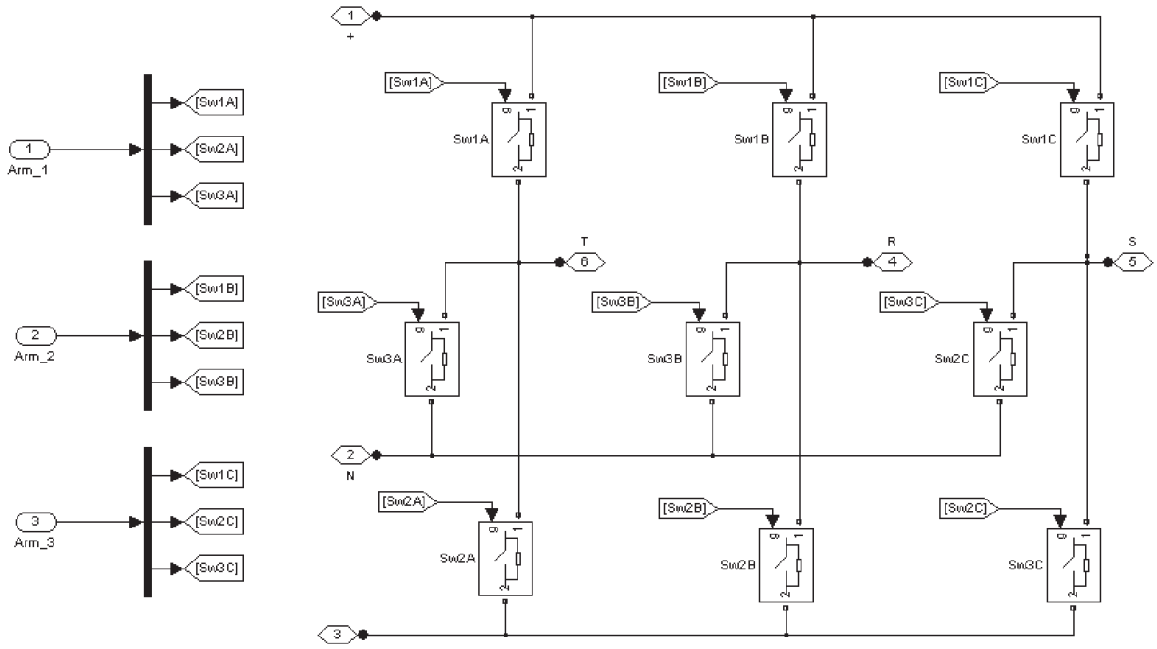

Fig. 5. Simulink multilevel converter

3.2. Full model

The complete model of the system has the following appearance (Fig. 9.).

Where phase to phase output block is the RST system, waiting for some charge to be connected.

As it has been described there are different important blocks:

— Reference block – Where reference vector characteristics are given, and some information about the DC inverter bus, and switching frequency.
— Sample block – There is 4 sample and hold block that refresh in every switching periods modulation function inputs.
— Modulation – Is a calculation block function which works with equations (2), (3) and (4). The output contains three sextant vectors and the time that each has to remain active.
— Duty ratio – This block takes care of giving just a single vector to the commutation function.
— Commutation – This subsystem is responsible of translating the entrance vector into ´1´´s and '0'´s for switch.
— Three level inverter following scheme on Figure 1.

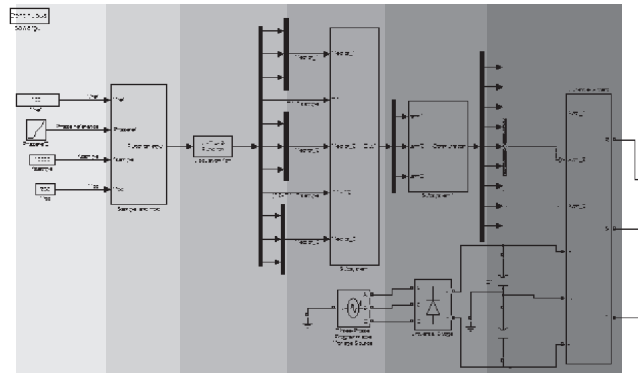

Fig. 9. Simulation model

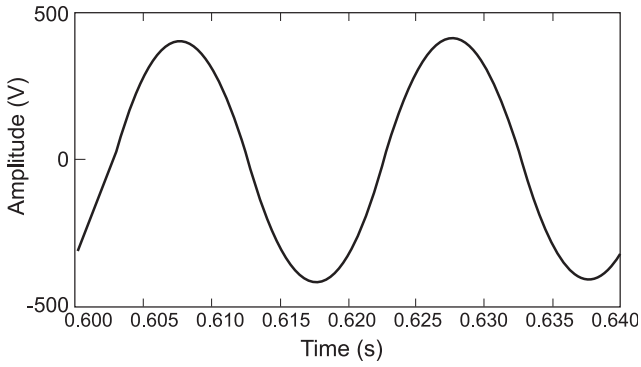

Fig. 10. 50 Hz reference wave

4. SIMULATION RESULTS

Simulation is done connecting three levels inverter to standard grid power supply. In ideal configuration with neutral converter point in ground connection (Fig. 10).

The temporal response of the line voltage is also checked (Fig. 11).

The results are satisfactory, so the overall method is validated. There is just one thing remaining to check. This modulation should not give common mode voltage, if adding the value of the 3 phase-to-phase voltages the output is always '0' the modulation will be satisfactory also from the common model emission point of view.

The simulated result of this addition corresponds to the Figure 12. It is obvious that the common mode emission is '0' even when the scale is very low (near the μs). So we can conclude that the goal of reducing the common mode voltage (and the common mode current in addition) has been achieved.

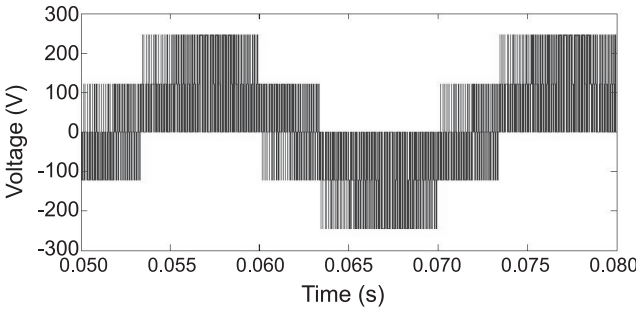

Fig. 11. Temporal three lever converter line voltage

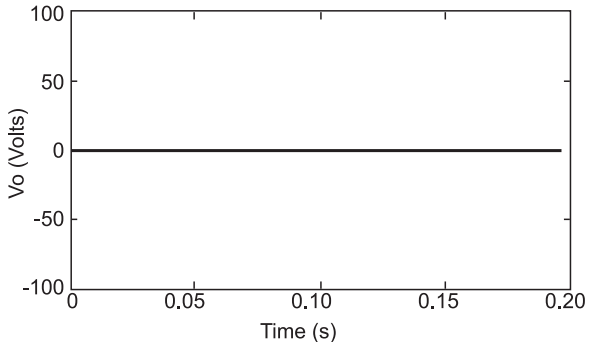

Fig. 12. Common mode voltage emission with ideal connection

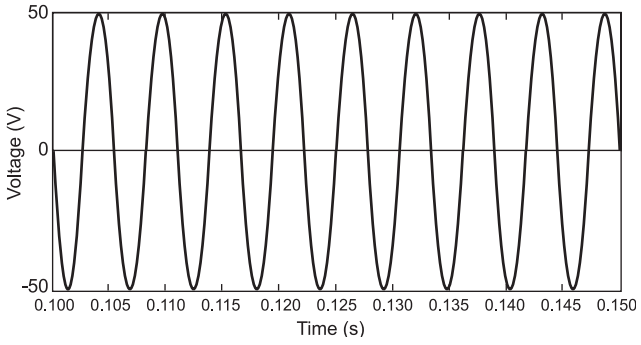

Fig. 13. Common mode voltage emission with floating neutral point

In ideal configuration, converter's neutral point is ground connected, if its configuration is changed using floating neutral point as a real configuration, on common mode appear low frequency voltage oscillations on neutral point, it is shown on Figure 13, and must be reduced by modulation improvement. However its oscillations are not as critical for induction machines as high frequency noise on common mode that is the cause of bearings currents and insulation problems. On Figure 13 is shown low frequency voltage oscillation due to oscillation in floating neutral point with clearly no high frequency components.

Table I. Test rig values

$V_{uv} = V_{wu} = V_{vw}$	160 Vrms
$L_s = L_1$	10 mH
C1 = C2	1.1 mF
R_L	16.5
M	0.75

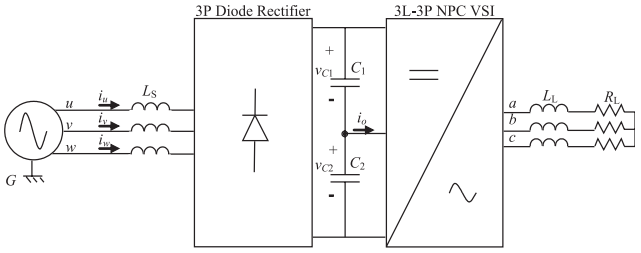

Fig. 14. Experimental configuration

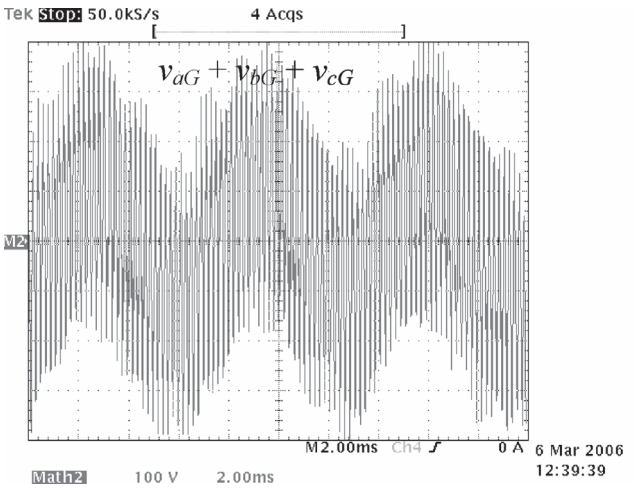

Fig. 15. Common mode voltage on time domain for a two levels converter

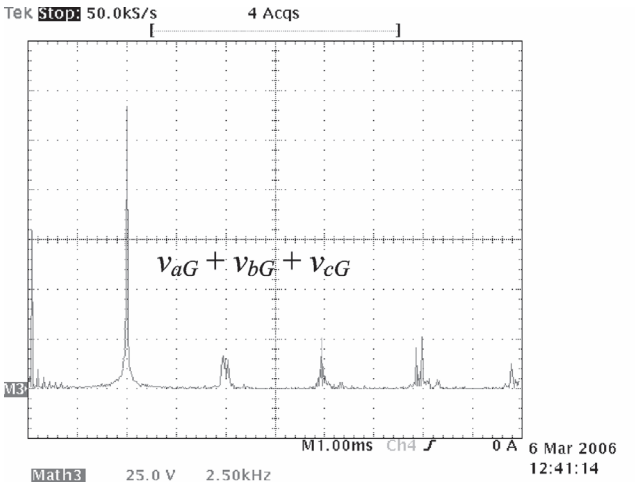

Fig. 16. Common mode voltages spectra for two levels converter

5. EXPERIMENTAL RESULTS

Following are presented experimental results for the purposed modulation; the implementation was done, by using three levels inverter working as a two level and following with the purposed modulation. Inverted was grid connected and LR load was used with 160Vrms applied. Load and converter configuration is shown (Fig. 14), values are shown in (Table 1).

Test results are shown on figures 15, to 18. At first two levels modulation was introduced, figures 15 and 16 clearly

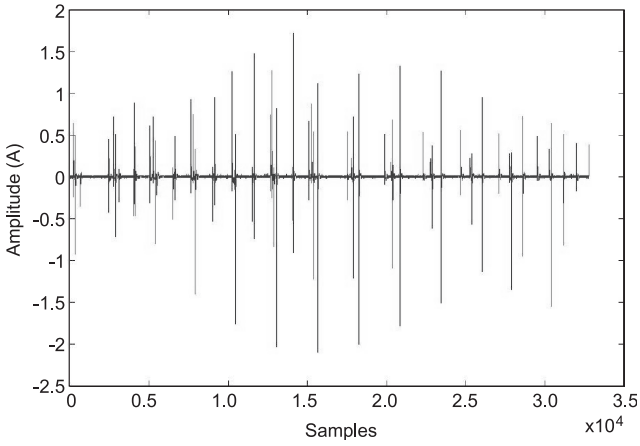

Fig. 17. Common mode current spectra for two level inverter

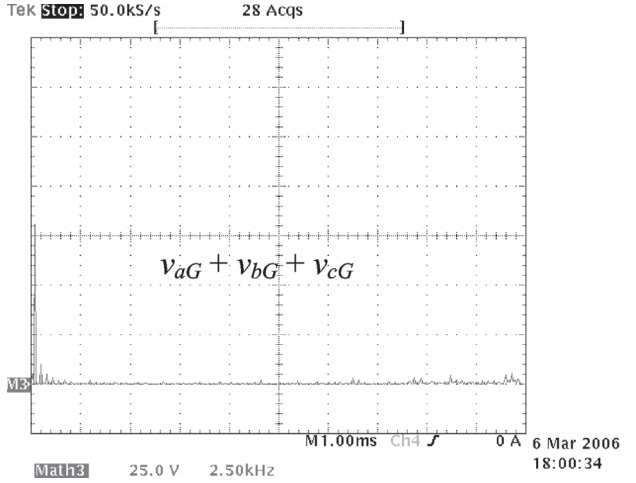

Fig. 19. Common mode voltages spectra for three level converter

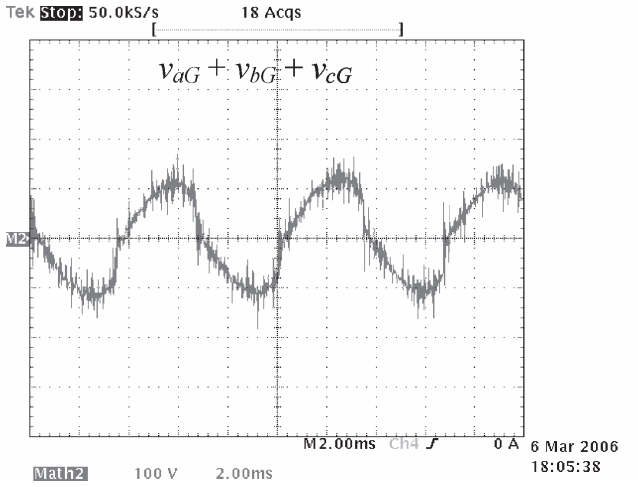

Fig. 18. Common mode voltage on time domain for a three levels converter

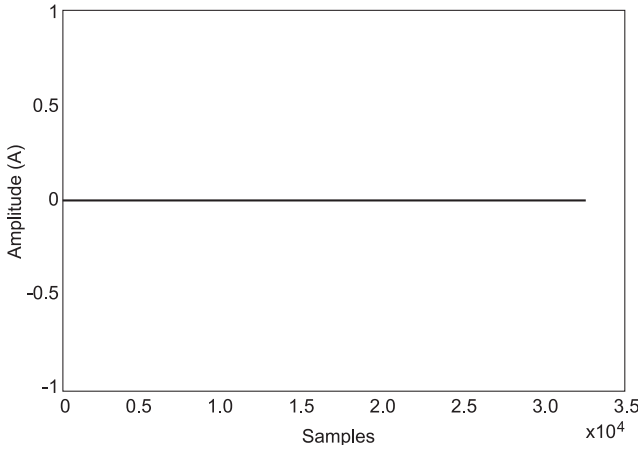

Fig. 20. Common mode current for three level converter

shown common mode voltages on temporal domain (Fig. 15) and frequency domain (Fig. 16). Main consequence of common mode voltage is shown on Figure 17, where common mode currents are shown. Those discharges are the main cause of bearing fault condition in induction machines.

Common mode Voltage on two levels inverter has two main different components, first one with lower amplitude a low frequency that is due to voltage oscillations on capacitors and second one about three times switching frequency with more amplitude, that is due to two levels modulation. The higher frequencies are much critical, because it causes most of the common mode fault effects. On Figures 18 and 19 the high frequency noise in a three levels inverter is shown clearly, and demonstrates modulation's efficiency on high frequency noise reduction.

6. CONCLUSIONS

Present paper expose fatal effects due to converter supply on induction machines, which are caused for common mode voltages on two level converters, due to high frequency noise components.

Three level converters especially in case of diode clamping configuration allows introducing zero voltage sequence common mode modulation by using medium vectors. Zero common mode voltage space is defined into three level converters switching cube, where every turning vector will have this property. By using this modulation common mode converter effects must be reduced, but some limitations appear especially for use non adjacent vectors. However three level converters present a good chance for zero sequence noise reduction that allows increasing Induction machines live.

Simulation and experimental results clearly shown great advances on zero sequence noise reduction, using medium vectors the common mode voltage will disappear and machine's live increase is guarantied.

7. ACKNOWLEDGMENT

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REFERENCES

1. Baker R.H., and Bannister L.H.: *Electric power converter*. U.S. Patent 3 867 643, Feb. 1975.
2. Kempski A., Smolenski R., Kot E.: *Mitigation techniques of conducted emi in multilevel inverter drives*. Compatibility in Power Electronics, 2005. IEEE June 1, 2005, pp. 218–222.
3. Oguchi K., Tanaka T., Hoshi N., Kubota T.: *A novel control method for single-phase slow switching multilevel rectifiers*. Industry Applications Conference, 2002. 37th IAS Annual Meeting. Conference Record of the Volume 3, 13–18 Oct. 2002, pp. 1966–1973.
4. Rodriguez J., Jih-Sheng Lai, Fang Zheng Peng: *Multilevel inverters: a survey of topologies, controls, and applications*. Industrial Electronics, IEEE Transactions on Volume 49, Issue 4, Aug. 2002, pp. 724–738.
5. Cacciato M., Consoli A., Scarcella G., and Testa A.: *Reduction of common-mode currents in PWM inverter motor drives*. IEEE Trans. on Industrial Applications, Vol. 35, 1999, pp. 469–476.
6. Lee H.D., and Sul S.K.: *Common-mode voltage reduction method modifying the distribution of zero-voltage vector in PWM converter/inverter system.* IEEE Trans. on Industrial Applications, Vol. 37, 2001, pp. 1732–1738.
7. Ye Z., Boroyevich D., and Lee F.C.: *Modeling and Control of Zero-Sequence Current in Parallel Multi-Phase Converters*. IEEE 2000.
8. McGrath B.P., Holmes D.G., and Lipo T.: *Optimized Space Vector Switching Sequences for Multilevel Inverters.* IEEE Trans. On Power Electronics, Vol 18, No. 6, 2003.
9. Loh P.C., Pang G.H.H., and Holmes D.G.: *Multi-level discontinuous pulsewidth modulation: common mode voltage minimization analysis*. IEEE Proc. Electr. Power Applications, Vol. 151, No.4, 2004.
10. Rodriguez J., Pontt J., Correa P., Cortés P., and Silva C.: *A New Modulation Method to Reduce Common-Mode Voltages in Multilevel Inverters*. IEEE Transactions on Industrial Electronics, Vol.51, No.4, 2004.
11. Zhang H., von Jouanne A., and Wallace A.: *Multilevel Inverter Modulation Schemes to eliminate Common-Mode Voltages*. IEEE, 1998.
12. Prats M.M., Franquelo L.G., Leon J.I., Portillo R., Galván E., and Carrasco J.M.: *A SVM-3D generalized algorithm for multilevel converters*. IEEE 2003.

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