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Passive Filter Design for Three-Phase Inverter Interfacing in Distributed Generation

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Summary: **With the growing use of inverters in distributed generation, the problem of injected harmonics becomes critical. These harmonics require the connection of low pass filters between the inverter and the network. This paper presents a design method for the output LC filter in grid coupled applications in distributed generation systems. The design is according to the harmonics standards that determine the level of current harmonics injected into the grid network. Analytical expressions for the maximum inductor ripple current are derived. The filter capacitor design depends on the allowable level of switching components injected into the grid. Different passive filter damping techniques to suppress resonance affects are investigated and evaluated. Simulated results are included to verify the derived expressions.**

Key words:
DG,
Inverter,
Grid connected,
Filtering,
Damping,
Harmonics

I. INTRODUCTION

The contribution of distributed generation (DG) is anticipated to grow rapidly in the near future. In addition to environmental aspects, their shorter building time may be a motivating force accelerating development. However, there are some barriers before wider DG deployment is achievable. One barrier is the connecting link to the network or grid. The DG situation is new in distribution networks since traditionally there are no generation units connected to the distribution network. New regulations and recommendations are needed for DG. Moreover, new practical solutions are essential to make DG viable.

The need for inverters in distributed generation systems and micro-grids has clarified the significance of achieving low distortion, high quality power export via inverters. Both switching frequency effects and grid voltage distortion can lead to poor power quality. A well designed filter can attenuate switching frequency components but impacts on control bandwidth and the impedance presented to grid distortion. The proposed system in Figure 1 employs power filters to meet imposed utility distortion limits, to avoid parallel resonance, and improve poor power quality.

The passive filter not only affects inverter harmonic injection but impacts on the harmonics produced by a coupled non- linear load. There are several techniques for controlling harmonic current flow, such as magnetic flux compensation, harmonic current injection, DC ripple injection, series and parallel active filter systems, and static VAr harmonic compensation [1-3]. Passive harmonic filters are often used to reduce voltage harmonics and current distortion in distributed generation systems.

The harmonic currents injected by a grid connected inverter can be classified as:

— Low frequency harmonics;
— Switching frequency harmonics; and
— High frequency harmonics.

Each category harmonic must be sufficiently and appropriately attenuated [4]. The current harmonics generated, if injected into the grid, can cause the malfunction of sensitive apparatus connected to the same bus. According to the harmonic standards, which determine the level of current harmonics injected into the grid network [5], the power filter should attenuate the harmonics to specific levels. Inverters for grid interfacing will need to incorporate interface filters to attenuate the injection of current harmonics.

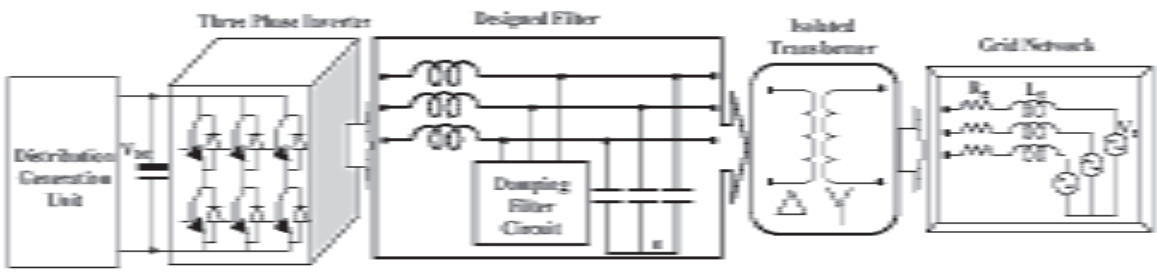


Fig. 1. Block diagram of the proposed interfacing system

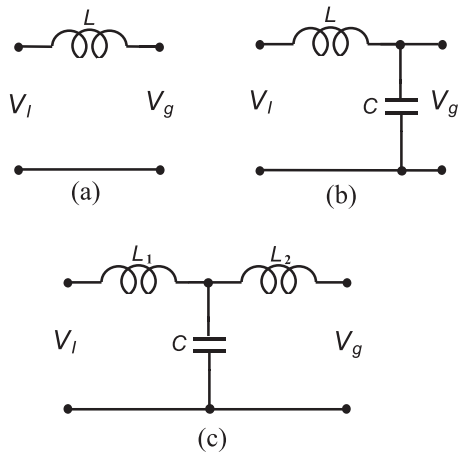


Fig. 2. Filter configuration circuits

II. FILTER CIRCUIT CONFIGURATIONS

The three main existing harmonic filter topologies for three-phase inverters follow.

A. L-Filter — First order

Attenuation of the basic inductor filter shown in Figure 2(a) is –20 dB/decade over the whole frequency range. Using this filter, the inverter switching frequency has to be high in order to sufficiently attenuate the inverter harmonics [2].

B. LC–Filter — Second order

The LC-filter in Figure 2(b) is a second order filter giving –40 dB/decade attenuation. Since the previous L-filter achieves low attenuation of the inverter switching components, a shunt element is needed to further attenuate the switching frequency components. This shunt component must be selected to produce low reactance at the switching frequency. But within the control frequency range, this element must present a high magnitude impedance. A capacitor is used as the shunt element. The resonant frequency is calculated from (1).

$$f_0 = \frac{1}{2\pi}\frac{1}{\sqrt{LC}} \tag{1}$$

The LC-filter in Figure 2(b) has been investigated in UPS systems with a resistive load [3]. This LC-filter is suited to configurations where the load impedance across C is relatively high at and above the switching frequency. The cost and the reactive power consumption of the LC-filter are more than to the L-filter because of the addition of the shunt element.

C. LCL-Filter — Third order

The third filter common in the literature is the LCL-filter configuration shown in Fig. 2(c). It produces better attenuation of inverter switching harmonics than the L and LC filters.

Key advantages of the LCL-filter are:

— Low grid current distortion and reactive power production;
— Attenuation of -60 dB/decade for frequencies in excess of the resonance frequency;
— Possibility of using a relatively low switching frequency for a given harmonic attenuation.

The resonant frequency of the LCL-filter is given by:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{2}$$

With low inductance on the inverter side, it is difficult to comply with IEEE519 standards without an LCL filter. An LCL filter can achieve reduced levels of harmonic distortion with lower switching frequencies and with less overall stored energy. On the other hand the LCL filter may cause both dynamic and steady state input current distortion due to resonance.

III. ANALYSIS OF THE DIFFERENT FILTER CONFIGURATIONS

The three different filter configurations will be analyzed. The distributed generation unit is assumed to operate in the grid connected mode, with the inverter connected to the grid network through a power filter.

A. L-filter

Figure 3a shows the output power as function of DC link voltage and the coupling filter inductance (L-filter) between the inverter and the grid network, based on:

$$P_o = \frac{3V_g}{X_L}\sqrt{{V_I}^2 - {V_g}^2} \tag{3}$$

The output power increases with increasing DC link voltage (V_{DC}) and decreasing filter inductance (L).

The purpose of the filter inductance is to reduce the current harmonics injected into the grid. The first surface in Figure 3b is the inductor harmonic current which is injected into the grid network. The second surface in Figure 3(b) is the standard grid injected harmonic current limits. The two surfaces are calculated as a function of DC link voltage and the filter inductance, at a switching frequency of 10 kHz. It is assumed that the grid voltage V_g comprises only a fundamental frequency component and the network is a short circuit at other frequencies. The grid network is assumed stiff, that is, the network impedance is zero. The harmonic current expression is:

$$\left|I_{o\ har}\right| = \frac{\left|V_{I\ har}\right|}{X_{Lh}} \tag{4}$$

If harmonic order (h) is greater than 35, the harmonic currents injected to the grid network must be less than 0.3 % $I_{\mathbf{rated}}$ [5]. The choice of filter elements is therefore required to take into account the inequality:

$$\left|I_{o\ har}\right| < \frac{0.3\%P_{rated}}{3V_g} \tag{5}$$

where P_{rated} is defined by Figure 3(a).

The L-filter cannot achieve the harmonic limit in equation (5). Figure 3b confirms this filter limitation and its inability to sufficiently reduce the harmonic injection current level. One solution is to increase the switching frequency to greater than 20 kHz, as shown in Figure 3c. The DC link voltage is fixed at 670 V.

B. LC-filter

The limitation of the LC filter is that the shunt element is ineffective when connected to a stiff grid network, where the grid impedance is insignificant at the switching frequency. The output current ripple is the same as the inductor current ripple with an L-filter, where the attenuation depends solely on the filter inductance.

C. LCL-filter

In most applications, an isolation transformer is used between the power filter and the grid. This inserts leakage inductance, which is seen by the grid. A modified LC-filter plus leakage inductance will be used in this study, which is basically an LCL-filter type but with constant leakage inductance L_2 on the output. The analysis will assume that L_2 is equal to the leakage inductance of the isolated transformer.

Figure 4a shows the output power as function of DC link voltage and inductor filter inductance, as given by equation (6). The output power increases with DC link voltage increase and decreasing filter inductance.

$$P_o = \frac{3V_g}{X_{L1} + X_{L2} - \dfrac{X_{L1}X_{L2}}{X_C}} \sqrt{V_I^{\,2} - V_g^{\,2}\left(1 - \frac{X_{L1}}{X_C}\right)^2} \qquad (6)$$

For a stiff grid, the output current harmonics injected are:

$$\left|I_{o\ har}\right| = \frac{\left|V_{I\ har}\right|}{X_{L1} - \dfrac{X_{L2}X_C}{X_{L2} - X_C}} \frac{X_C}{X_{L2} - X_C} \qquad (7)$$

Figure 4b shows the output grid harmonics and current harmonics limits as a function of DC link voltage and inductance (L_1). The switching frequency is 10 kHz, and comparing Figure 3b with the previous LC-filter, it can be seen that the LC-filter with an isolated transformer can satisfy the harmonic limit requirements by a sufficient margin. Figure 4c shows the harmonic grid currents and the harmonic injection limits into the grid network as a function of the switching frequency and inductance. The harmonic requirement can be achieved with a switching frequency greater than 3.5 kHz.

A relationship between the inductor L_1 and the capacitor C with constant output power, DC link voltage and isolated transformer inductance can be obtained from equations (8) and (9), where the desirable harmonic limits are taken into account. The required output harmonic limits can be achieved for a range of values of L_1 and C. Decreased inductance raises the possible output power and decreases inductance, whilst raising capacitance increases VAr consumption and raises the

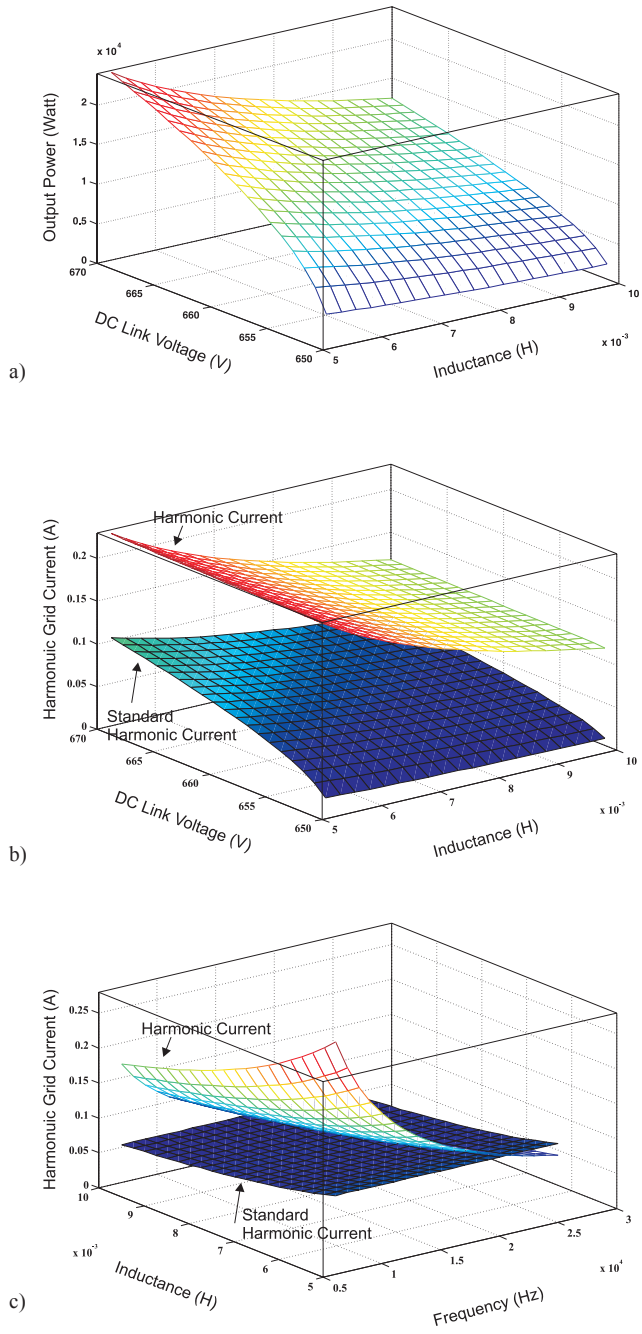


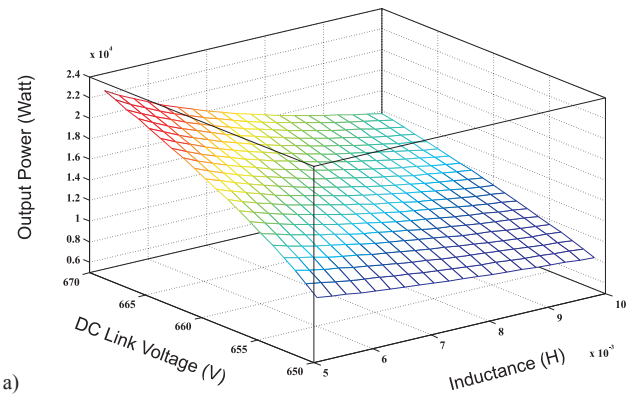
Fig. 3. Characteristics of L-Filter: (a) output power as function of DC link voltage and inductor inductance; (b) harmonic current as function of DC link voltage and inductor inductance; and (c) harmonic current as function of switching frequency and inductor inductance

inverter harmonic currents. The inductor harmonic content affects both the inverter rating and the control system.

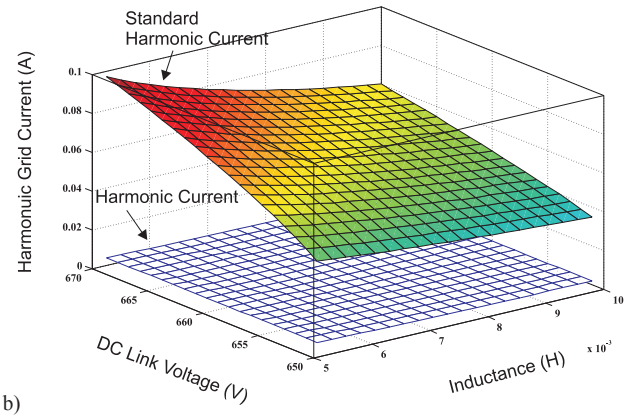
$$X_{L1h} = \frac{1000V_g\left|V_{I\ har}\right|X_{Ch} + X_{L2}X_{Ch}P_{rated}}{\left(X_{L2h} - X_{Ch}\right)P_{rated}} \qquad (8)$$

$$X_{Ch} = \frac{1}{2\pi\left(f_s - 2f_m\right)C},\ X_{L2h} = 2\pi\left(f_s - 2f_m\right)L_2$$

$$L_1 = \frac{1000V_g\left|V_{I\ har}\right|X_{Ch} + X_{L2}X_{Ch}P_{rated}}{2\pi\left(f_s - 2f_m\right)\left(X_{L2h} - X_{Ch}\right)P_{rated}} \qquad (9)$$



a)



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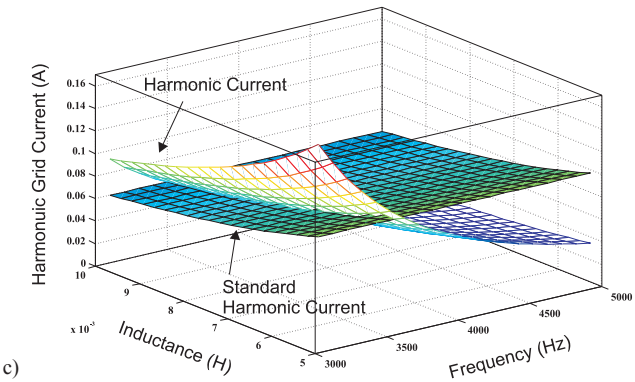

c)

Fig. 4. Characteristics of LCL-Filter: (a) output power as function of DC link voltage and inductor inductance; (b) harmonic current as function of DC link voltage and inductor inductance; and (c) harmonic current as function of switching frequency and inductor inductance

Figure 5 illustrates the relationship between inductance and shunt capacitance at different frequencies. The rated power and isolation transformer inductance are 10 kW and 1 mH respectively.

Figure 6 shows rated inductor current, the harmonic inductor current (inverter current), and the harmonic limit that can be superimposed on the inductor current, with capacitance and switching frequency variation.

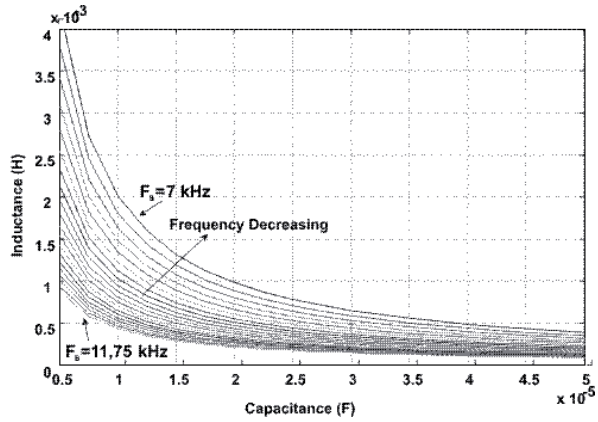

Fig. 5. Inductance versus capacitance and frequency

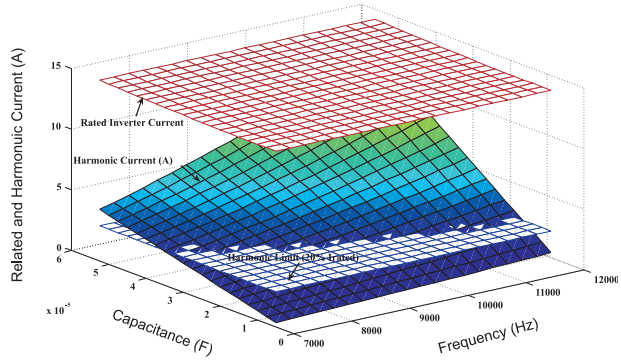

Fig. 6. Rated and harmonic currents as a function of switching frequency and capacitance

The inductor (inverter) current variation with capacitance and isolated transformer inductance is given by equation:

$$|I_{inv}| = \sqrt{\left(\frac{P_o}{3V_g}\left(1-\frac{X_{L2}}{X_C}\right)\right)^2 + \left(\frac{V_g}{X_C}\right)^2} \qquad (10)$$

The fundamental inverter current does not depend on the switching frequency. The inductor harmonic current caused by the inverter switching (f_s-$2f_m$) is given by:

$$|I_{inv\ har}| = \frac{V_{I\ har}}{X_{L1h} - \dfrac{X_{L2h}X_{Ch}}{X_{L2h}-X_{Ch}}} \qquad (11)$$

Figure 7 shows the percentage harmonic inverter current as a function of inductance at different switching frequencies. The harmonic limit for the inverter current is also shown.

IV. FILTER DESIGN TECHNIQUES

In [6] the total harmonic inductor current and capacitor voltage of the LC filter was derived but the filter component values were not derived. Minimum LC filter reactive power was used to determine the LC values. Alternatively the system time constant, the cost function and THD are used to determine the LC values [7]. The scheme in [8] adds an

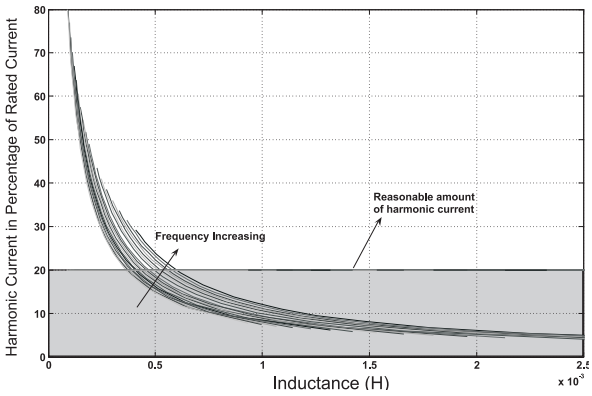

Fig. 7. Harmonic current as a function of inductance at different frequencies

LC trap filter in cascaded with the conventional LC filter, which proved effective in filtering the voltage harmonics. Another harmonic filter design approach is based on the transfer function [9].

V. LC FILTER DESIGN APPROACH

The LC low pass filter is able to attenuate most low order harmonics in the output voltage waveform. To minimize distortion, for linear or non linear loads, the inverter output impedance must be minimized. Therefore the capacitance should be maximized and the inductance minimized when specifying the cut-off frequency. This decreases the overall cost, weight, volume and $Q\left(\sqrt{\mathrm{L}/\mathrm{C}}/R\right)$. But by increasing the capacitance, the inverter power rating will be increased due to the reactive power increase due to the filter. The switching frequency in high power applications is chosen with regard to inverter efficiency, since switching losses are a significant portion of the overall losses. It is desirable to minimize the size and cost of the filtering components by increasing the switching frequency, but efficiency sets a limit (a design trade off must be made).

Any design technique must achieve the standard requirements in [5]. Figure 8 illustrates the inverter phase voltage output and its frequency spectrum. The associated module cannot be connected to the utility unless the high frequency components are attenuated from the output voltage. The shown results are from a SPWM inverter operated at 2 kHz on a 400 V DC link.

The inductor determines the ripple in the inductor current and reduces the low frequency harmonic components. The phase voltage of the SPWM inverter in the proposed system is shown in Figure 9. Consider the inverter phase a voltage V_a in Figure 9, and assume that the output voltage V_{ga} varies slowly relatively to the switching frequency. Then the voltage across the inductor is:

$$V_L = V_{Ia} - V_{ga} \tag{12}$$

To determine the maximum inductor ripple current, the values of V_{Ia} and V_{ga} are as in equations (13) and (14). The phase voltage duty cycle at maximum output is 75%:

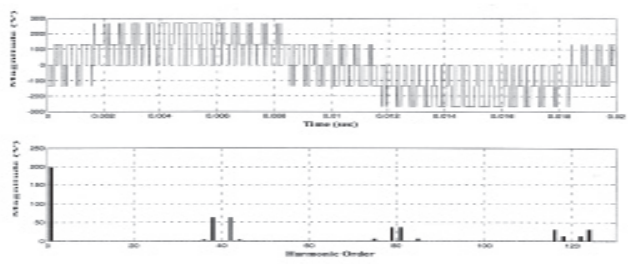

Fig. 8. Inverter phase voltage with respect to the load neutral and its frequency spectrum

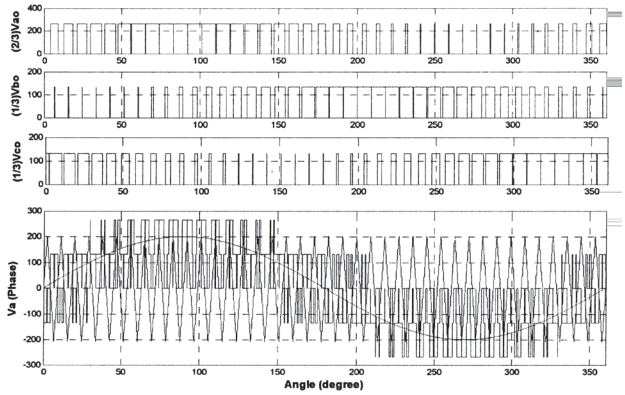

Fig. 9. Output phase voltage and carrier signal

$$V_{Ia} = \frac{2}{3}V_{DC},\ V_{ga} = \frac{1}{2}V_{DC} \tag{13}$$

$$V_L = \frac{2}{3}V_{DC} - \frac{1}{2}V_{DC} = \frac{1}{6}V_{DC} \tag{14}$$

According to the harmonic standard [5], 15–20% of the rated current is allowable; 20% is assumed. The maximum ripple can now be calculated from equation (16). The ripple current depends on the DC link voltage, inductance, and the switching frequency. The DC link voltage and switching frequency are constant, thus the inductance can be calculated from equation (19):

$$V_L = L\frac{\Delta\hat{I}_L}{\hat{\delta}T_s},\quad \Delta\hat{I}_L = \hat{\delta}T_s\frac{V_L}{L} \tag{15}$$

$$\Delta\hat{I}_L = \hat{\delta}\frac{V_L}{L\,f_s} = \frac{1}{6}\frac{\hat{\delta}V_{DC}}{L\,f_s} \tag{16}$$

$$\hat{\delta} = 1 - \frac{1}{4} = \frac{3}{4} \tag{17}$$

$$\Delta\hat{I}_L = \frac{1}{8}\frac{V_{DC}}{L\,f_s} \tag{18}$$

$$L = \frac{1}{8}\frac{V_{DC}}{\Delta \hat{I}_L f_s} \tag{19}$$

where:
V_L — inductor voltage,
f_s — switching frequency,
V_{DC} — DC link voltage,
$\hat{\delta}$ — maximum duty cycle
L — filter inductor

The high frequency components have to be eliminated from the inductor current when connected to the grid. This must be performed by the shunt impedance which is low at high frequencies. Capacitor selection is a trade off between inductor and capacitor reactive power. In a grid connected mode, the harmonic current injected into the grid network is the main issue. In the island connected mode, the DG unit is the source of power and voltage harmonics, which are the main concerns.

It is assumed that the DG unit is connected to the grid through an isolation transformer. The inverter is considered a current source injecting currents into the grid. Assume that V_I is the inverter output voltage, V_c is the capacitor voltage and I_o, I_{L1} are the inverter output current and inductor current, respectively:

$$\frac{V_c(s)}{V_I(s)} = \frac{Z_c(s)\,(Z_t(s)+Z_g(s)}{Z_c(s)\,(Z_t(s)+Z_g(s)+Z_{L1}(s))+Z_{L1}(s)\,(Z_t(s)+Z_g(s))}$$

$$\frac{I_{L1}(s)}{V_I(s)} = \frac{Z_c(s)+(Z_t(s)+Z_g(s)}{Z_c(s)\,(Z_t(s)+Z_g(s)+Z_{L1}(s))+Z_{L1}(s)\,(Z_t(s)+Z_g(s))}$$

$$\frac{I_o(s)}{V_I(s)} = \frac{Z_c(s)}{Z_c(s)\,(Z_t(s)+Z_g(s)+Z_{L1}(s))+Z_{L1}(s)\,(Z_t(s)+Z_g(s))}$$

where:
Z_c — capacitor impedance,
Z_g — grid network impedance,
Z_t — transformer impedance,
Z_{L1} — inductor impedance.

$$\frac{I_o(s)}{I_{L1}(s)} = \frac{Z_c(s)}{Z_c(s)+Z_t(s)+Z_g(s)} \tag{20}$$

The grid may be the (stiff) mains, a micro-grid, or a stand alone load, meaning that the grid impedance may range from almost zero (stiff mains) to infinite (no-load stand-alone). Using $Z_g = 0$ in the previous transfer functions, the worst case conditions for the filter are:

$$\frac{I_o(s)}{I_{L1}(s)} = \frac{Z_c(s)}{Z_c(s)+Z_t(s)} \tag{21}$$

$$\left|Z_c(f-2f_m)\right| = \left|Z_t(f-2f_m)\right|\left|\frac{I_o(f-2f_m)}{I_{L1}(f-2f_m)-I_o(f-2f_m)}\right| \tag{22}$$

$$\left|I_{L1}(f-2f_m)\right| = \frac{\left|1+\frac{Z_t(f-2f_m)}{Z_c(f-2f_m)}\right|\cdot\left|V_I(f-2f_m)\right|}{\left|Z_t(f-2f_m)+Z_{L1}(f-2f_m)+\frac{Z_{L1}(f-2f_m)\,Z_t(f-2f_m)}{Z_c(f-2f_m)}\right|} \tag{23}$$

The switching frequency output current will be a fraction of the rated current as per the standards specification [5]:

$$I_o(f-2f_m) = X.I_{Rated} \tag{24}$$

In the island connected mode, the inverter becomes a voltage source since it will be supplying power. Thus the output voltage must be filtered of undesired harmonics. The grid impedance Z_g is now substituted by Z_{Load}:

$$\left|Z_{Load}\right| = \frac{\left|V_{O\ rated}\right|}{\left|I_{O\ rated}\right|} \tag{25}$$

$$\frac{V_o(s)}{V_I(s)} = \frac{Z_{Load}(s)}{Z_t(s)+Z_{Load}(s)+Z_{L1}(s)+\frac{Z_{L1}(s)(Z_t(s)+Z_{Load}(s))}{Z_c(s)}} \tag{26}$$

VI. CASE STUDY

Consider a 10 kVA three-phase inverter connected to a grid network through an isolation transformer 240/415 Δ/Y with X = 0.3 Ω. The DC link voltage is 400 V and the switched frequency is 4 kHz. From equation (19), the filter inductance will be 2.5mH. The standards state that the harmonic orders greater than 35 must not exceed 0.3 % rated current [5]. Thus the capacitance calculated from equation (19) is C=50 μF.

The grid network impedance L_g and R_g vary depending on where the DG unit is connected to the grid. The values of the designed filter components are; L_1 = 2.5mH, C = 50 μF and L_t = 1 mH. The grid impedance used in the analysis is L_g = 0.1mH and R_g = 1mΩ.

VII. DAMPING FILTER DESIGN

Passive LC filters have high Q characteristics, hence low damping at the resonant frequency, which can cause system instability. Advanced techniques are used to actively damp resonance effects [10–11]. Such methods add complexity to the control system. Damping may be ignored because of the existence of the inductor parasitic resistances, which afford damping or to retain filter simplicity and efficiency. Initially the system is observed without adding any damping elements to the filter. The following transfer functions can be derived, involving the inverter voltage V_I and the grid voltage V_g, taking into account transformer inductance L_t. Figure 10 shows the output current and capacitor voltage transfer function, without any damping elements:

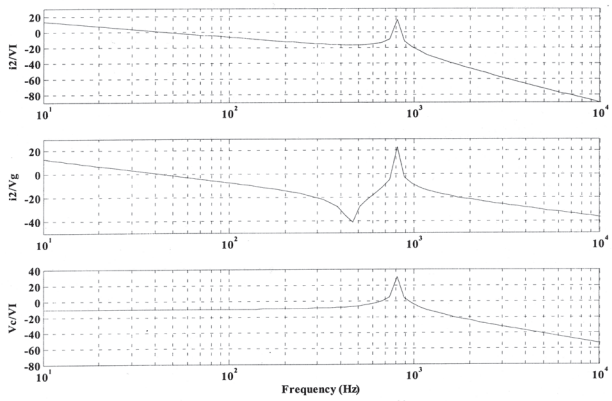

Fig. 10. System transfer functions

$$\frac{i_o}{V_I} = \frac{1}{s^3 L_1 C(L_g + L_t) + s^2 L_1 R_g C + s(L_1 + L_t + L_g) + R_g}$$

$$\frac{i_o}{V_g} = \frac{s^2 L_1 C + 1}{s^3 L_1 C(L_g + L_t) + s^2 L_1 R_g C + s(L_1 + L_t + L_g) + R_g}$$

$$\frac{V_c}{V_I} = \frac{sL_g + R_g}{s^3 L_1 C(L_g + L_t) + s^2 L_1 R_g C + s(L_1 + L_t + L_g) + R_g}$$

Several passive damping topologies can be used; each having its particular properties. The main aim of damping is to suppress resonance without reducing attenuation at the switching frequency, nor affecting the fundamental. The different resonance frequency damping methods are investigated and compared.

A. Method (1) — *R* parallel with the shunt element

Resistance can be added in parallel with the shunt capacitor, as illustrated by Figure 11a. The impact of the resistor is to reduce the effects of resonance on the grid current and the capacitor voltage as shown in Figure 11b. It is a simple method but results in increased losses.

B. Method (2) — R_d in series with the shunt element

Series damping resistance can be added to the shunt path as shown in Figure 12a. Figure 12b shows that the damping increases as R_g increases. This method has two main drawbacks. First, larger resistance reduces the attenuation above the resonant frequency and second, the resistance is a source of significant loss.

C. Method (3) — Parallel L_d and R_d in series with the shunt element

In the filter in Figure 13a, the inductor L_d presents low impedance at power frequencies which reduces the current flow through the parallel resistor. The resistive losses decrease with increased inductance. At high frequencies, the influence of the inductor will be minimal, as the inductive reactance is high. As shown in Figure 13b, increasing the inductance L_d, increases losses and costs, and attenuation rises.

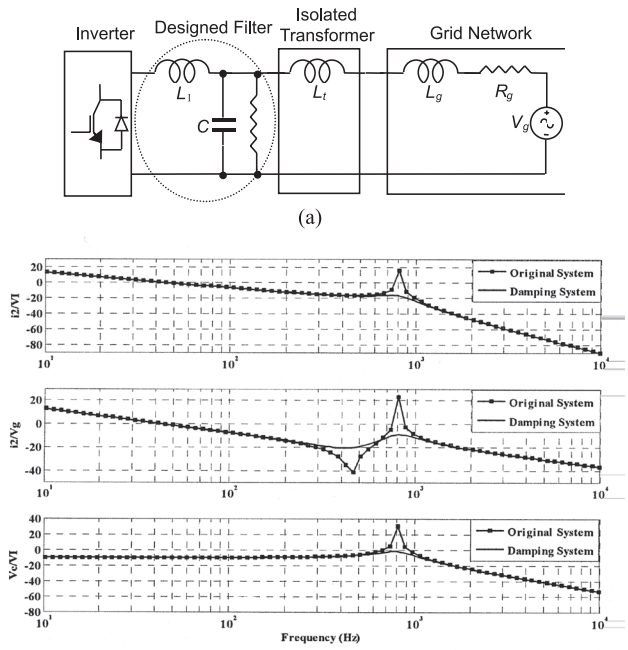

Fig. 11. Shunt R damping: (a) circuit and (b) characteristics

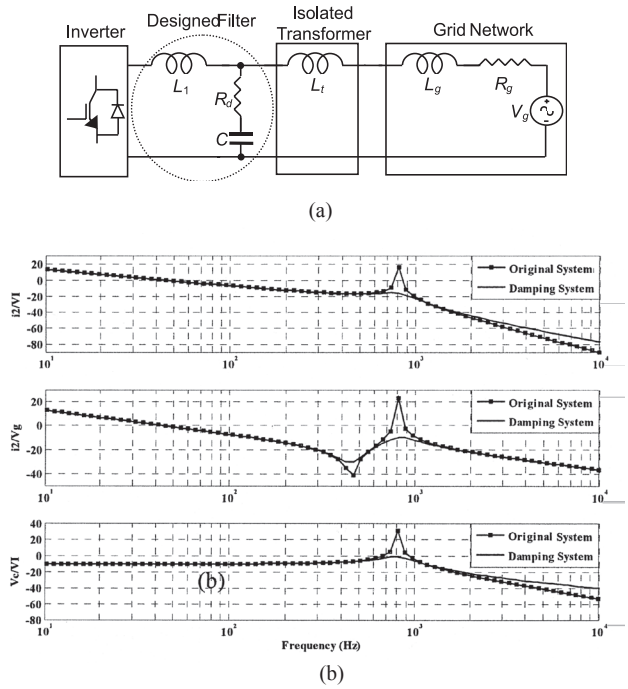

Fig. 12. Series R with the shunt element: (a) circuit and (b) characteristics

D. Method (4) — Series C_d and R_d in parallel with the shunt element

A series R_d–C_d can be added in parallel with the shunt capacitor as shown in Figure 14a. The parallel combination of the damping capacitance and the filter capacitance must be the same as calculated in equation (22) to give the same cut off frequency and same reactive power consumption. The attenuation will be reduced with increased C_d, as shown in Figure 14b.

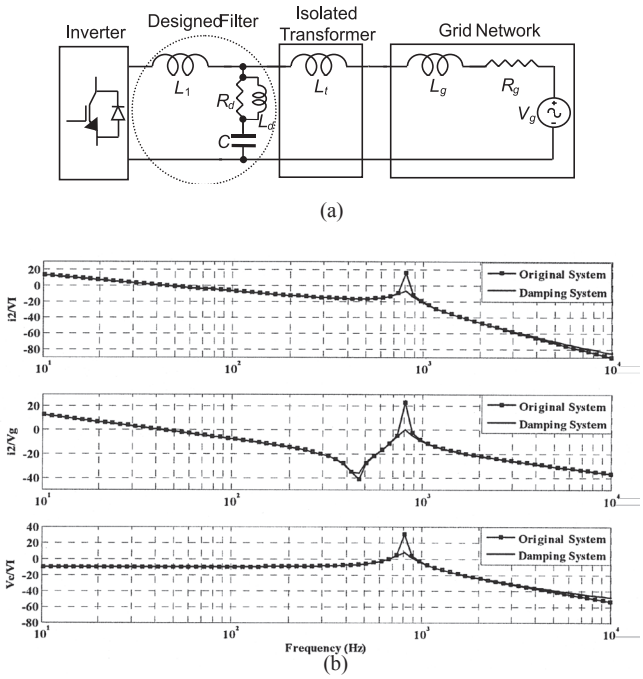

Fig. 13. Parallel L and R in series with the shunt element: (a) circuit and (b) characteristics

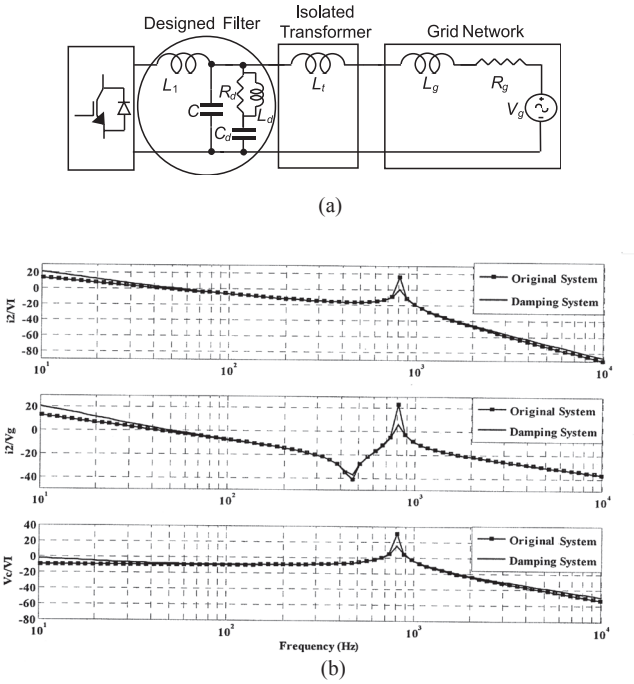

Fig.15. L and R in parallel with series C, all in parallel with the shunt element: (a) circuit and (b) characteristics

E. Method (5) – L_d and R_d in parallel with series C_d, all in parallel with the shunt element

In Figure 15a inductance is added to the R_d–C_d. The losses are reduced as the impedance of the inductor is low at low frequencies, as shown in Figure 15b.

F. Method (6) – Series L_d, R_d and C_d in parallel with the shunt element

The tuned L_d–C_d circuit in parallel with the shunt element, as shown in Figure 16a, provides a sink at the resonant frequency. At the fundamental frequency, the system acts like method (4), as the impedance of the inductance is small, as shown in Figure 16b. The inductor becomes active at the resonant frequency. The damping harmonic filter is chosen to reduce the effect of the 810 Hz resonance on the system. Therefore C_d is selected as 20 μF and L_d from equation (28).

$$L_d = \frac{1}{\omega_o^2 C_d} \tag{27}$$

If the summation of C and C_d is maintained constant, with C_d = 20 μF, then C = 30 μF, L_d = 1.9 mH, and R_d = 3Ω.

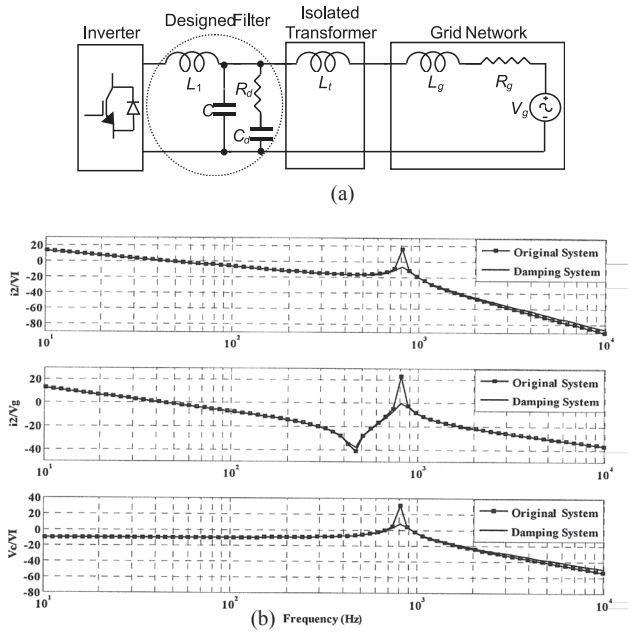

Fig. 14. Series C and R in parallel with the shunt element: (a) circuit and (b) characteristics

G. Method (7) — R_d in series with L_1 which are in parallel with L_d

There are some approaches that add an inductor into the system instead of a capacitor. Damping based on shunting the series element is shown in Figure 17a. The size of the inductor of the R_d–L_d damping approach is often much smaller than when adding blocking capacitor C_d with an -C_d damping network. This damping method is favoured for high density inverters. Figure 17b shows the filter frequency domain performance.

VIII. SIMULATIONS

The proposed filter design was applied to a three-phase SPWM inverter operating at 4 kHz, and connected to a grid network with the previous specification. Figure 18 shows the inverter output three-phase and inductor currents in the time domain, while Figure 19 shows their frequency spectrum.

The seven damping techniques can be used to suppress any hazards caused by resonance. Table 1 compares between the different damping techniques, showing the power loss at the fundamental power frequency with a fixed 23dB attenuation at the resonance frequency.

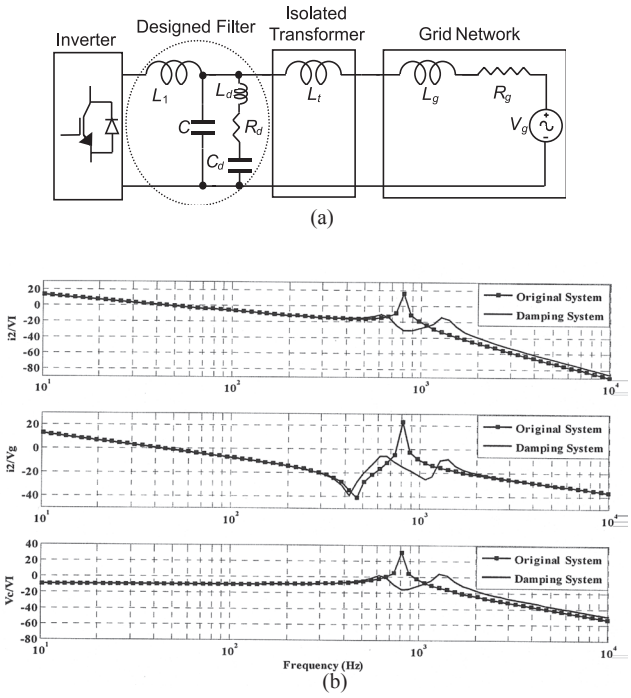

Fig. 16. Series L, R and C in parallel with the shunt element: (a) circuit and (b) characteristics

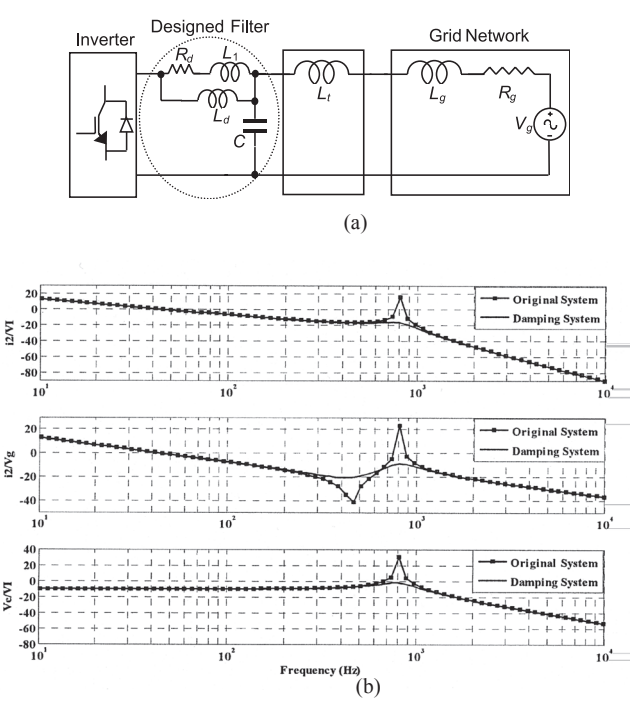

Fig. 17. R_d in series with L_1 which are in parallel with L_d: (a) circuit and (b) characteristics

The Table shows that power losses increase with increasing attenuation. Method (6) is the only exception, as increased attenuation decreases the power losses.

CONCLUSION

This paper has investigated the design procedures for LC filters used with grid connected inverters in distributed generation systems. The filter design is based on achieving the standard level determined by IEEE519 for harmonic limits. Several passive damping circuit configurations have been considered. The different methods were evaluated and assessed by using Bode plots. The proposed filter design and damping circuits can be used within distributed generation systems.

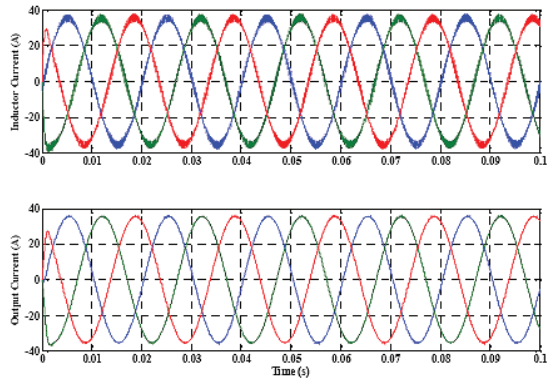

Fig. 18. Output phase current and inductor current

REFERENCES

1. Singh B., Al-Haddad K. and Chandra A.: *A review of active filters for power quality improvement.* IEEE Transactions on Industry Electronics, Vol. 46, No. 5, 1999, pp. 960–971.

Table 1.

Damping method	Power Loss
1	1.5 kW
2	6.5 W
3	3.2 W
4	6.9 W
5	1.6 W
6	4 W
7	96 W

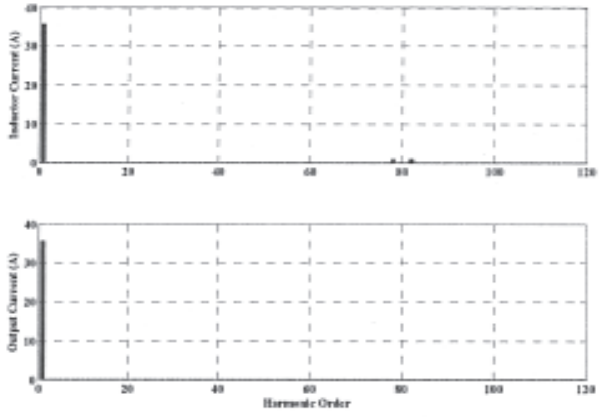

Fig. 19. Frequency spectrum of the output and inductor currents

2. El-Habrouk M., Darwish M.K. and Mehta P.: *Active power filters: a review.* Electric Power Applications, IEE Proce., Vol.147, Issue 5, 2000, pp. 403–413.
3. Akagi H.: *Active harmonic filters*. Proc. of the IEEE Vol. 93, Issue 12, Dec. 2005 pp. 2128–2141.
4. Holmes D.G., Lipo T.A.: *Pulse Width Modulation for Power Converters: Principles and Practice.* IEEE Press Series on Power Engineering, — Wiley-IEEE Press, Edition 1 October 2003.
5. IEEE Standards 519-1992, Recommended Practices and Requirements for Harmonic Control in Electric Power Systems, 1992.
6. Dahono P.A., Purwadi A., Qamaruzzaman: *An LC filter design method for single-phase PWM inverters.* Power Electronics and Drive Systems, Proceedings 1995, Vol.2, 1995, pp.571–576.
7. Kim J., Choi J., Hong H.: *Output LC filter design of voltage source inverter considering the performance of controller*. Power System Technology, Proceedings, 2000, Vol. 3, pp.1659–1664.
8. Sozer Y., Torrey D.A., Reva S.: *New inverter output filter topology for PWM motor drives*. Power Electronics, IEEE Transactions, Nov 2000, Vol. 15, Issue 6, pp. 1007–1017.
9. Phipps J.K.: *A transfer function approach to harmonic filter design*. Industry Applications Magazine IEEE, March-April 1997, Vol. 3, pp. 68–82.
10. Dahono P.A., Bahar Y.R., Sato Y., Kataoka T.: *Damping of transient oscillations on the output LC filter of PWM inverters by using a virtual resistor*. Power Electronics and Drive Systems, 2001, Proceedings, Vol. 1, pp. 403–407.
11. Dahono P.A., Taryana E.: *A new control method for single-phase PWM inverters to realize zero steady-state error and fast response.* Power Electronics and Drive Systems (PEDS), 2003, Vol. 2, pp. 888–892.

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