Control Circuit for Series Active Power Filters Based on Programmable Logic Devices

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Summary: This paper describes a control circuit for the active power filters working with three-phase AC power line. It describes logic circuitries as well as laboratory test results. The control circuit was realized with programmable logic devices, fast analog-to-digital and digital-to-analog converters. Proposed system working with open-loop control, it allows significantly simplifying its logic structure. Programmable logic devices do simultaneously a few independent tasks, so a control algorithm can be performing fast, improving considerably compensation dynamic. This paper includes results of laboratory tests of the active power filter consisted of proposed control circuit and a voltage-source converter.

1. INTRODUCTION

The common application of nonlinear loads in power distribution system cause serious distortions of line voltage. Nonlinear loads, especially six-pulse diode rectifiers, and thyristor power converters with phase control, inject into the power system high level of current harmonics, what has an important influence for increase voltage harmonics in grid.

Passive (LC) or active (APF) filters can improve the quality of the voltage in transmission/distribution system. Shunt passive LC filters are used to improve power factor and to suppress current harmonics. One of the biggest disadvantages of passive filters is impossibility to change their compensation characteristic. More effectiveness of eliminating current harmonics, and also voltage harmonics can be achieved by active filters.

Proposed control circuit is designed to work with voltage-source converter and than it functions as a series active filter. The control circuit was realized with programmable logic

devices (PLD). Implementation in PLD in compare to use a microprocessor unit allows faster execution of a control algorithm. Some tasks such as data processing and control external devices can be executed by PLD simultaneously in view of flexible configuration of logic resources.

2. SERIES ACTIVE POWER FILTERS

Series active filter works as a programmable voltage-source v_{AF}, which is connected between a load and mains. Load voltage is equal to the sum of mains voltage and voltage of the active filter v_{AF} reduced by the voltage drop of the power line. Compensation voltage v_{AF} generates actual voltage magnitude in opposite to distorted load voltage magnitude. Block diagram of the active power filter is shown in Figure 1.

The active power filters realize:

— compensation of a voltage drop on the impedance Z_L of the grid,
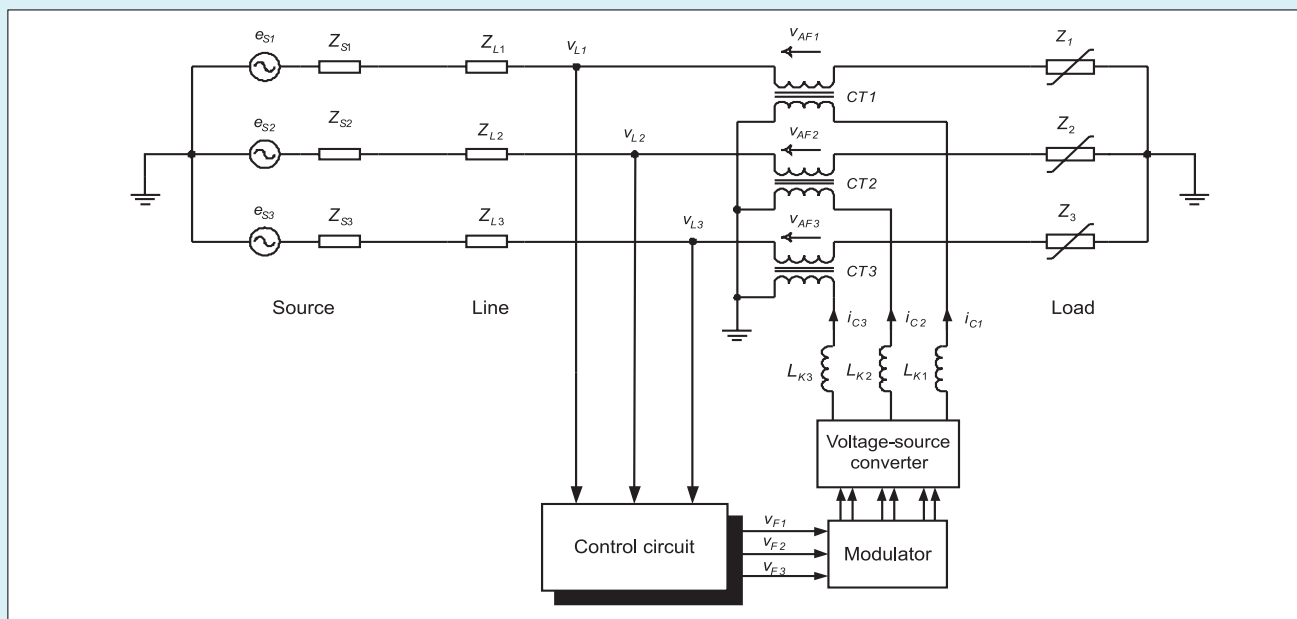

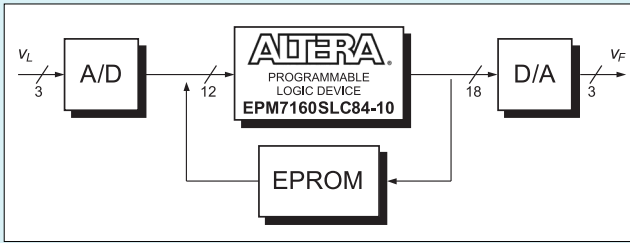Fig.1. Basic diagram of the series active filter

Fig. 2. Block diagram of the control circuit for active power filters

— imbalance reduction and voltage stabilization in the grid,
— elimination voltage harmonics, unbalance, flicker and notching from the load terminals,
— limitation magnitude increase of the short-circuit current and limit its.

3. CONTROL CIRCUIT FOR THE ACTIVE POWER FILTERS

The control circuit is applied to generate temporary magnitude of reference compensation voltage v_F and v_{AF} through the coupling transformer. Actual magnitude of reference compensation voltage v_F is calculated based on measured line voltage v_L. Figure 2 shows the block diagram of the proposed control circuit.

The principles of proposed control circuit:
— application of programmable logic device,
— high precision of input and output voltage obtained with 12-bit resolution digital data processing and fast analog-to-digital and digital-to-analog converters,

— processing 920 samples of digital signal per one period of mains voltage,
— wide range of operating frequency: 45…55Hz,
— optionally digital representation of output signal.

The control circuit was designed to work with analog input and output signal with amplitude equal to ±5V. All data processing routines are executed in digital system. As a central processing unit was applied programmable logic device. It allows to the most efficient data processing in the time-domain.

The amplitude of the input signal – power line voltage v_L, and also output signal – reference compensation voltage v_F are by in a ratio of 1:100 to real amplitudes. Assumed 12-bit resolution of digital word allows eliminate the error of the analog signal amplitude v_F below 0.24V (with reference to voltage amplitude of the power line). Assumed number of samples per mains period – 920, allows eliminate angle error below 0.4°.

Reference compensation voltage v_F is expressed by:

$$v_F\left(t\right) = v_L\left(t\right) - v_{sin}\left(t, f\right) \tag{1}$$

Actual value of the reference compensation voltage v_F is defined as the difference between actual value of the supply line voltage v_L and actual value of the sinusoidal template v_{sin}. The three-phase sinusoidal template is being determined by reading successively data from a nonvolatile memory. This approach allows significantly simplify the control circuit and also accelerate control and data processing. Specific sample of the sinusoidal template can be generated by determine proper memory address.
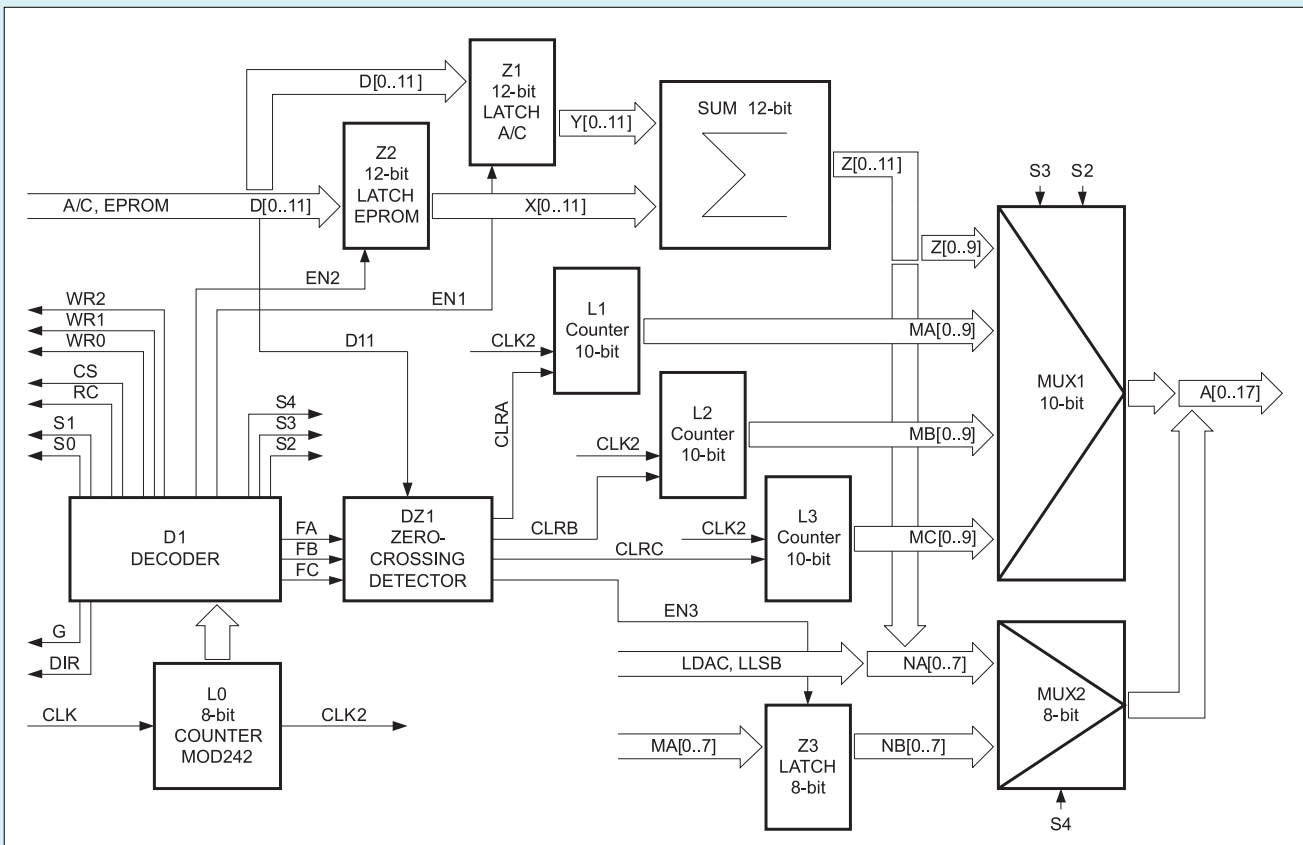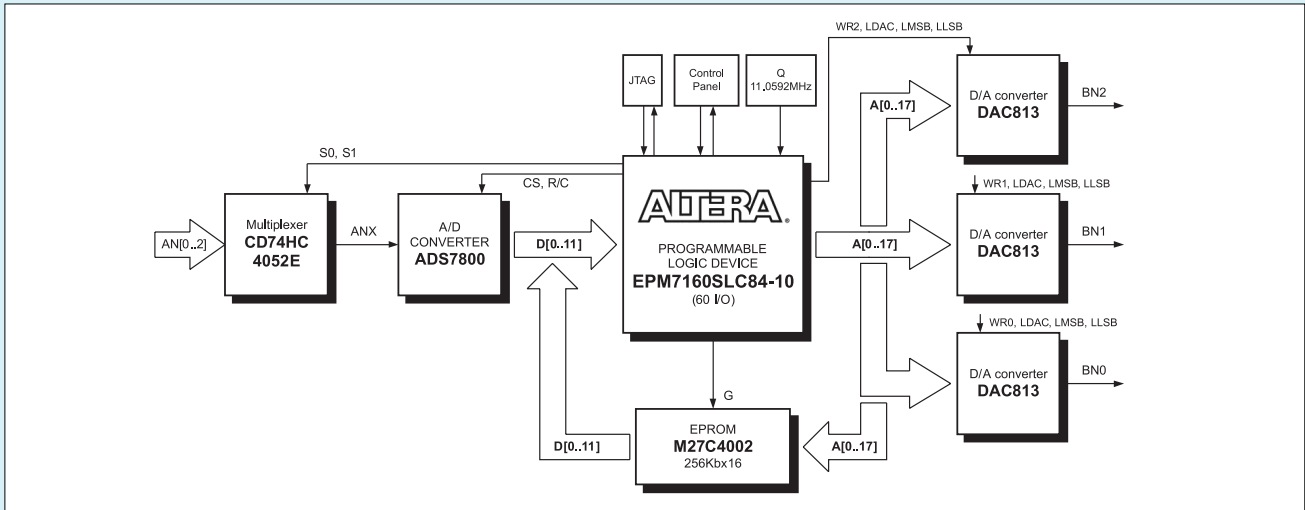

Fig. 3. Logic structure

Fig. 4. Block diagram of proposed control circuit

4. CONTROL CYCLE

All operations concerning both 12-bit digital data processing and controls peripheries devices are being done by programmable logic device. Figure 3 shows the detailed logic structure that was implemented into the PLD.

The PLD is clocked by the external oscillator. System clock is connected to the counter L0, this one in combination with the D1 decoder works as instruction counter. It performs such task as: multiplexer addressing, initiate conversion both analog-to-digital and digital-to-analog converter, hold data in internal registers, synchronization between the zero-crossing point and the sinusoidal template, initiate reading samples of sinusoidal template stored in nonvolatile memory, enabling/disabling and addressing internal multiplexers structure.

Control circuit cycle begins with addressing the external multiplexer with the S0 and S1 lines thereby put the proper analog signal to the analog-to-digital converter. In the next moment line CS and RC enables converter and initiates conversion. After approximately 3ms the conversion is finished, and converted data is stored into Z1 register. Input of the Z1 register is connected to the D[0..11] bus, this bus is also used to lead the 12-bit digital data from the external memory, in the next moment 12-bit word is held in Z2 register. These data stored in Z1 and Z2 register are lead to the inputs of the SUM adder. This adder works according to equation (1). It's a combinational logic circuitry, thus it doesn't need initialization. SUM generates correct result shortly after it's got the input data (calculation time depends on timing parameters of the PLD). The Z[0..11] bus leads 12-bit word which is digital representation of the reference compensation voltage. This signal is sent to the inputs of the MUX1 multiplexer, next to the A[0..17] bus and finally to the proper digital-to-analog converter.

The others logic circuits are used to determine the frequency of the power line voltage and also to calculate the present sample of the sinusoidal template. The zero-crossing detector and three 10-bit counters L1, L2, and L3 are used for this purpose. The number of the sample – memory address is determined by the value one of these counters (each counter

is individual for one phase). The value of each counter is incremented with the fixed time step, and reset after the zero crossing detection. If the counter L1 is reset, its lower 8-bits are held in Z3 register. Then register Z3 contains information about value of the power line frequency. Register Z3 is connected to the bus NB[0..7] and addresses the external memory and then determine the frequency of the sinusoidal template. Memory address consists of two parts: frequency and a number of the sample.

5. PROPOSED SYSTEM CONFIGURATION

Proposed control circuit for the active power filters consists of few blocks. Figure 4 shows block diagram of the control circuit, it consists of analog-to-digital conversion part (HC4052, ADS7800), sinusoidal template (M27C4002), control and processing unit EPM7160 (approximately 3200 logic gates), digital-to-analog conversion part (DAC813).

6. TIMINGS

The number of assumed control cycles per mains period determines the amount of time for execution the single cycle. It cannot exceed $22\mu s$. Figure 5 illustrates timings of the control circuits divided into analog-to-digital converter, PLD, digital-to-analog converter. The complete cycle takes about $19.2\mu s$; most of the time takes conversion analog-to-digital and digital-to-analog, about 64% of the whole time.
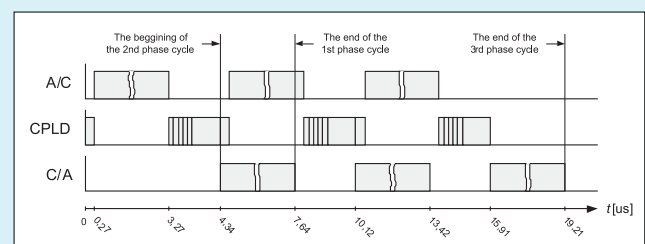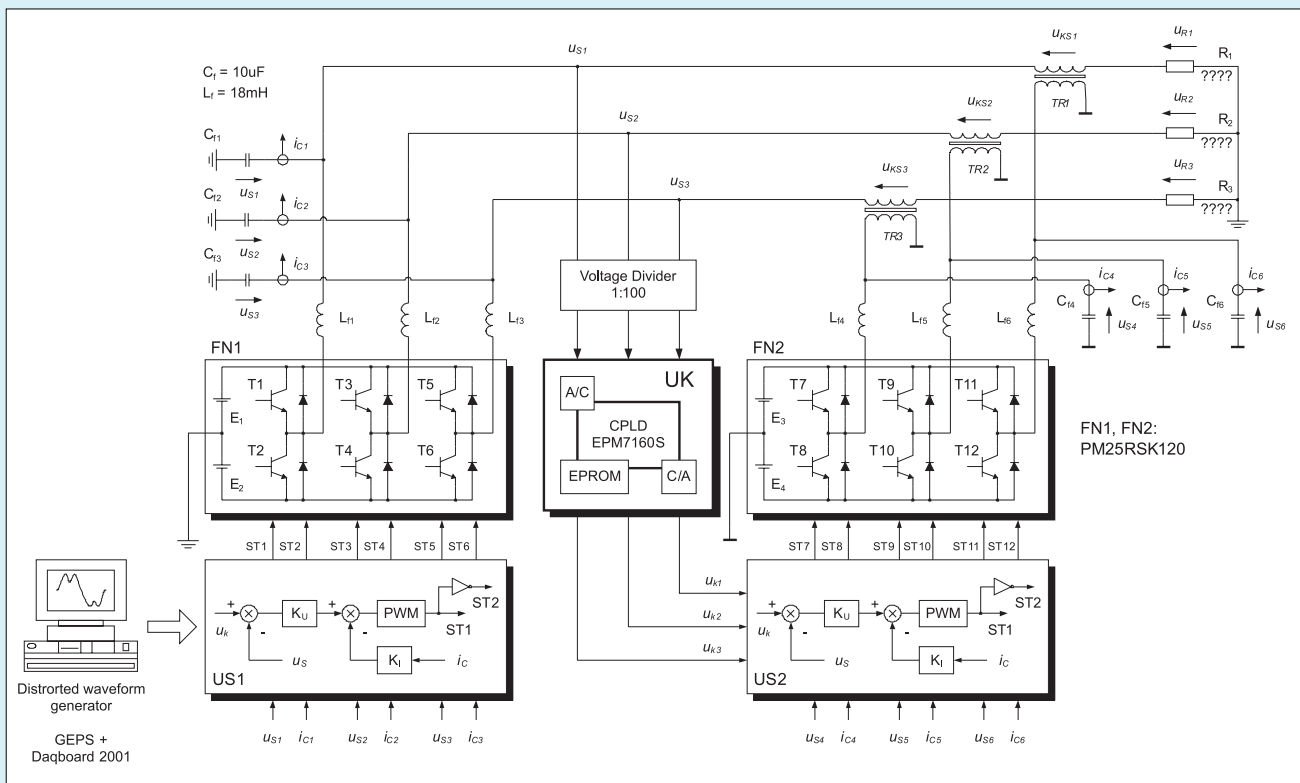

Fig. 5. Timings of the control circuit

Fig.6. Block diagram of the laboratory test circuit

7. LABORATORY EXPERIMENTS

The control circuit was implemented with lower resolution of the digital word (9-bits instead of 12-bits). Limitation of the resolution was necessary because of insufficient amount of logic gates in used PLD. Figure 6 shows the block diagram of the laboratory test circuit. The series active power filter consists of the control circuit of the APF – UK, voltage-source converter FN2 and its control circuit US2. The APF eliminates voltage harmonics from the load terminals by the coupling transformer connected in series between the three-phase source (GEPS – imbalance/harmonics waveform generator and a voltage-source converter FN1) and the load. In experiment was used three-phase resistant load R of power about 250W. The analyses are done with many parameters variations of the supply, as the nominal parameters of the source there were assumed: rms voltage equal to 110V and frequency of 50Hz.

On the Figures 7 and 8 are shown the results of the laboratory experiments. Figure 7a shows the waveforms on the load terminals in case of unbalance supply voltage with the rms voltage equal to 110V, 125, 85V. In the next case (Fig.7b) supply voltage except for voltage unbalance generates voltage harmonics, and these parameters are equals to: $U_{S1} = 110V$, $U_{S1-3h} = 30\%$; $U_{S2} = 85V$, $U_{S2-5h} =10\%$; $U_{S3} = 85V$, $U_{S3-7h} = 5\%$.

Figure 8a illustrates waveforms on the load terminals in case of voltage flicker of 15%, which fluctuates at 5Hz. On the Figure 8b is shown voltage swing of 10% on the load terminals, which fluctuates at 2.5Hz. Both Figures 7 and 8 shows the voltage on the load terminals without as well as with compensation of the voltage. The APF starts compensate at the time marked vertical line t1.

8. CONCLUSIONS

The series active power filter based on proposed control circuit compensates all of tested voltage flicker/imbalance. The voltage THD is reduced to about 2%. The application of PLD to the control circuit achieves great dynamic of compensation, thanks to high number of control cycles per mains period, thereby it provides low value of the phase shift between compensation voltage and distorted line voltage.

The proposed system works as an open-loop control. Some of the advantages of this configuration are no instability problem, high reliability, extremely simple logic structure, and also low costs. There is no possibility to hang up the system, because it is hardware logic structure.

The system can compensate for most of the voltage harmonics and unbalance on the load terminals, but it doesn't check how successful the compensation has been.

The control circuit can work with a voltage-source converter by supplying analog or digital signals. In the laboratory experiments were used analog interface only.

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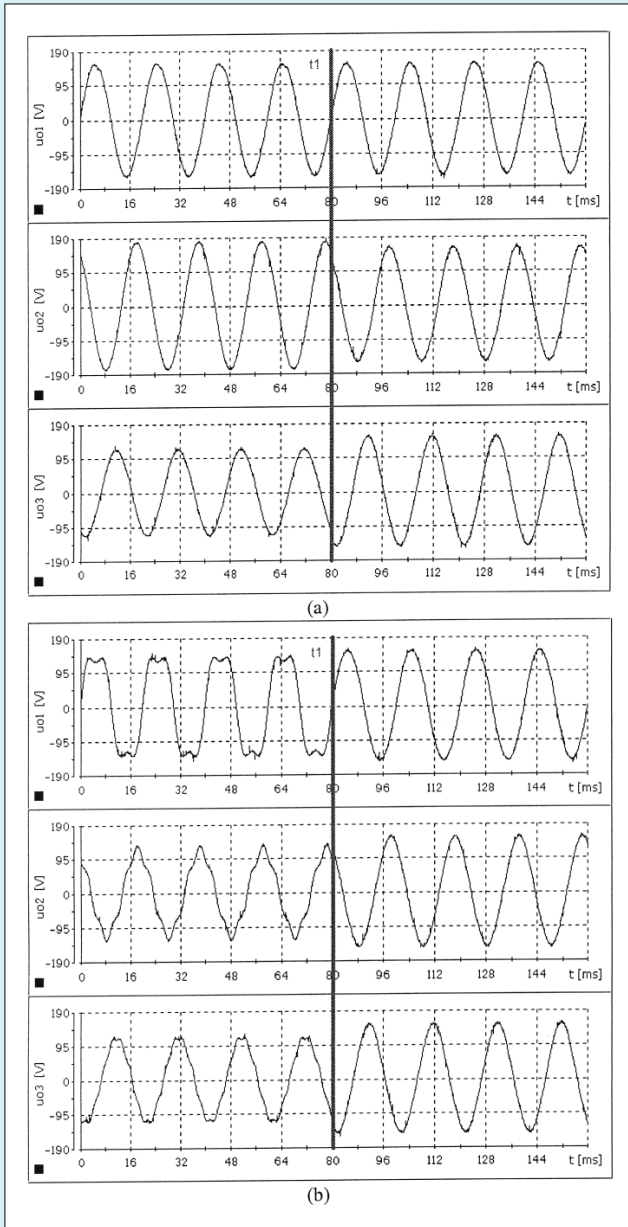5. *"Programmable Logic Device Family MAX7000"*, Altera Corporation, 2003

Fig.7. Voltage waveforms on the load terminals before and after compensation by the series active filter: a) unbalance, b) unbalance and harmonics

Fig. 8. Voltage waveforms on the load terminals before and after compensation by the series active filter: a) flickers, b) swings

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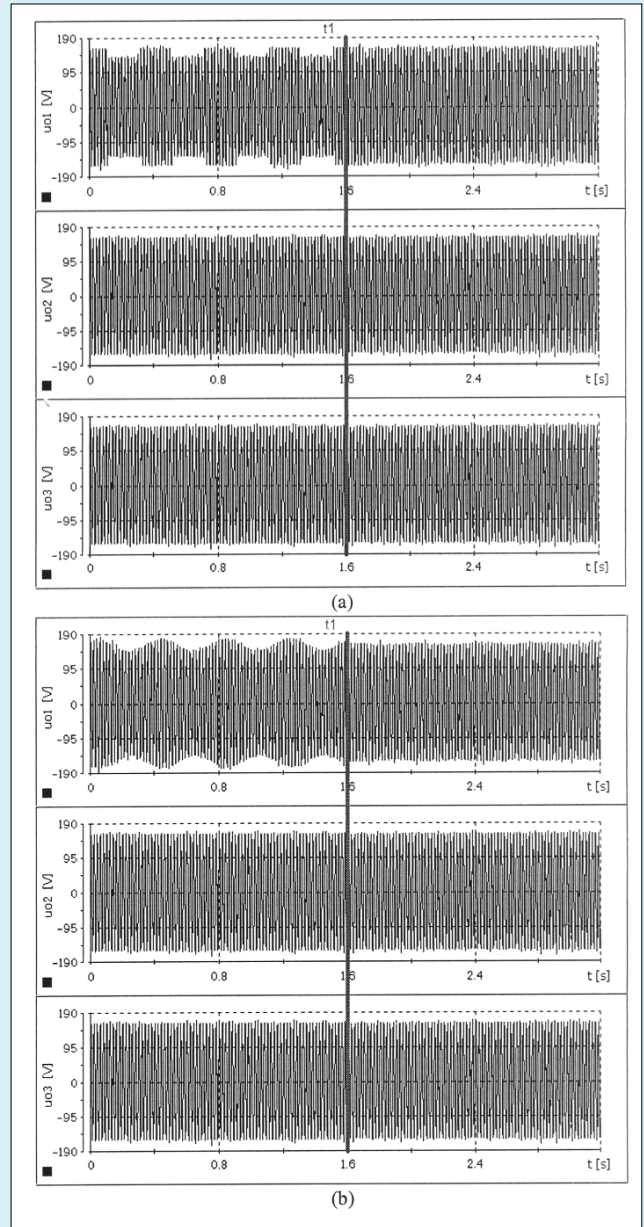
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