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PRACTICAL ISSUES IN FREQUENCY DISTURBANCE RECORDER DESIGN FOR WIDE-AREA MONITORING

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Summary: To maintain power system operation in a balanced and stable condition, the frequency deviation and the rate of frequency change information are highly desired in monitoring and protection applications of the power grid. How to obtain frequency information more accurately and efficiently has been the topic discussion for decades. PMUs (Phasor Measurement Unit) are the most widely-used devices for measuring phase angle differences and they also provide very accurate frequency information. However, the high installation cost of PMUs limits their applications for wide area control and stability analysis of power system. Thanks to commercial GPS receivers and the fast developments in Ethernet networks, an affordable wide area, quasi real-time, GPS synchronized frequency measurement is now possible. This paper introduces a portable networked Frequency Disturbance Recorder (FDR) device, which can be used at any 110V wall outlet and transmit measured frequency data remotely via the Ethernet. The practical issues and challenges of the device design and implementation are analyzed and discussed. Based on these low cost FDRs, a US-wide Frequency Network (FNET) has been implemented at Virginia Tech and some power system monitoring applications are being developed by taking fully advantage of the FDRs.

Key words:
Power system
Wide-area monitoring
Phasor analysis
Frequency tracking

1. INTRODUCTION

Frequency is one of the most important parameters for power system operations. In the past several decades, many kinds of frequency estimation algorithms have been proposed. Zero-crossing Techniques [1, 2] may be the most straightforward method with minimized circuits and low computation load. However, in those techniques, the measurement accuracy is heavily affected by noise on the signal. Least Square Approximation [3] [4] can suppress the noise effects by adjusting the coefficient of a pseudo-inverse matrix, but for a large frequency deviation range, the errors introduced are also large. For small frequency deviation, ±5Hz , the leakage effect of Fourier transform can be used to estimate the frequency deviation based on a linear relationship between leakage coefficient and frequency deviation [5]. The leakage effect technique is easily implemented, but its accuracy suffers a lot from non-fundamental components. In addition, an extra zero-crossing detector is necessary since this technique works only for a sinusoidal waveform. Kalman Filter Technique[6] is ideal for noise immunity during measurement. But the assumption that the probability density function of the state vectors is know is not always true, and high variance will introduce an unnecessary response delay. Phasor Angle Analysis[7] is a highly accurate and robust computation technique with minimum system requirements for implementation, and it is the most ideal algorithm for add-in functions for existing devices or low cost design.

In this paper, a brief investigation of the Phasor Angle Analysis algorithm is given in Section 3. The FDR system architecture and block diagram are given in Section 4. In Section 5, some practical issues encountered during the FDR design progress are discussed, and some possible improvement solutions for these issues are proposed. Section 6 provides an example demonstrating FDRs applications for monitoring purposes.

2. ALGORITHM REVIEW – PHASOR ANGLE ANALYSIS

Assuming a pure sinusoidal waveform $x(t)$ at nominal frequency is given by:

$$x(t) = \sqrt{2}X \sin(2\pi f_0 t + \theta) \tag{1}$$

where:
X RMS value of the signal, and
θ Initial phasor angle.

Assuming Nf_0 is the sampling rate used to obtain the discrete value of this signal, and N is the number of samples per cycle, then the *rth* phasor of *x(t)* is equal to:

$$\overline{X}^{(r)} = Xe^{j\theta}e^{j\frac{2\pi}{N}r} \tag{2}$$

The recursive calculation can be applied to obtain the $(r+1)th$ phasor.

$$\overline{X}^{(r+1)} = \overline{X}^{(r)} + j\frac{1}{\sqrt{2}}\frac{2}{N}\left(x_{N+r+1} - x_{r+1}\right)e^{-j\frac{2\pi}{N}r} \tag{3}$$

If the input signal is a pure sinusoidal waveform, $x_{N+r+1} = x_{r+1}$ for all r, then:

$$\overline{X}^{(r)} = \overline{X}^{(r-1)} \text{ for all } r \tag{4}$$

However, in a real power system, even one in a steady state condition, the frequency of the input voltage, f, could slightly deviate from the nominal frequency f_0. The input signal can be rewritten as:

$$x(t) = \sqrt{2}X \sin\left(2\pi\left(f_0 + \Delta f\right)t + \theta\right) \tag{5}$$

and the new *rth* phasor can be expressed as [8]:

$$\begin{aligned}\overline{X}^{(r)}_{f_0+\Delta f} &= \overline{X}^{(r)}_{f_0} e^{j\frac{2\pi\Delta f}{N60}r} e^{j(N-1)\frac{\pi\Delta f}{Nf_0}} \frac{\sin\frac{\pi\Delta f}{f_0}}{N\sin\frac{2\pi\Delta f}{Nf_0}} \\ &- \overline{X}^{*(r)}_{f_0} e^{-j\frac{2\pi\Delta f}{Nf_0}r} e^{j(N-1)\left(\frac{2\pi}{N}+\frac{\pi\Delta f}{Nf_0}\right)} \frac{\sin\frac{\pi\Delta f}{Nf_0}}{N\sin\left(\frac{2\pi}{N}+\frac{\pi\Delta f}{Nf_0}\right)}\end{aligned} \tag{6}$$

If $\Delta f = f - f_0$ is relatively small, the second term of (3.6) can be neglected[8, 9], and (3.6) can be simplified to be:

$$\overline{X}^{(r)}_{f_0+\Delta f} = \overline{X}^{(r)}_{f_0} \frac{\sin\frac{\pi\Delta f}{f_0}}{N\sin\frac{2\pi\Delta f}{Nf_0}} e^{j(N-1)\frac{\pi\Delta f}{Nf_0}} e^{j\frac{2\pi\Delta f}{N60}r} \tag{7}$$

If φ_r and φ_{r+1} are defined as the phasor angles of the *rth* and *(r+1)th* phasor respectively, the relationship between the frequency deviation and phasor angles can be easily obtained:

$$\frac{d\psi}{dt} = \lim_{t\to 0}\frac{\psi_r - \psi_{r-1}}{t} \approx \frac{\psi_r - \psi_{r-1}}{1/Nf_0} = 2\pi\Delta f \tag{8}$$

so

$$f = f_0 + \Delta f = f_0 + \frac{1}{2\pi}\frac{d\psi}{dt} \tag{9}$$

and

$$\frac{df}{dt} = \frac{1}{2\pi}\frac{d^2\psi}{dt^2} \tag{10}$$

In the above analysis, in order to determine the relationship between the phasor angles and frequency tracking, the second term of (3.6) is considered to be 0. However, if we define:

$$Y = \frac{\sin\frac{\pi\Delta f}{Nf_0}}{N\sin\left(\frac{2\pi}{N}+\frac{\pi\Delta f}{Nf_0}\right)} \tag{11}$$

and plot Y versus Δf with $N=24$, as shown in Figure 1, it can be noticed that the Y term is not always so small that can be ignored, especially when $|\Delta f|$ gets large.

In $\Delta f = f - f_0$, f is the real frequency of the input signal; f_0 is the assumed nominal frequency of the input signal, and the associated sampling rate for the signal is $f_s = Nf_0$. From Figure 1, one can note that when Δf is zero, the Y term is zero; and the smaller $|\Delta f|$, the smaller the $|Y|$ term. In other words, the more closely the assumed nominal frequency f_0 to real frequency f, the smaller the errors that will be introduced to frequency estimation. Hence, if one uses the previous estimation frequency as the assumed nominal frequency to form a new sampling rate, i.e., resampling the signal again, and takes the second frequency estimate, the $|\Delta f|$, i.e., accuracy of frequency estimation, can be improved. When and if necessary, the resampling schemes can be carried out several times in order to obtain the desired accuracy.

3. SYSTEM OVERVIEW

Based on the frequency estimation algorithm discussed in section 2, the Frequency Disturbance Recorder (FDR) was designed and implemented. Figure 2 shows the system block diagram.

This cost-effective and portable measurement device takes the voltage signal from 110V outlets, and provides a GPS synchronized, close to real-time, frequency measurement data from flexible locations to one or multiple data service and monitoring centers. The FDR consists of four main parts: main computation unit, digital signal conditioning unit, GPS receiver, and Serial to Ethernet converter.

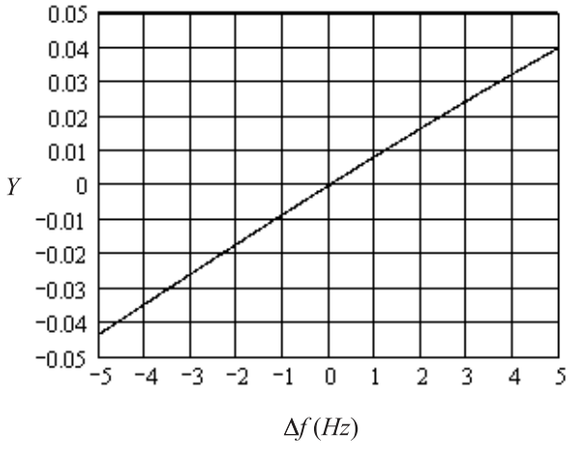

Fig. 1. Y term versus

The main computation unit is MCU/DSP/PC based, where the frequency estimation algorithm, GPS synchronization, and other communication functionalities are implemented. The digital signal conditioning system takes and scales down the input voltage, and runs A/D conversion and advanced digital filtering; it provides real and clean input data suitable for further frequency calculation. In the MCU/DSP version, the embedded serial to Ethernet converter makes the device networked, hence for different data collection and analysis applications interfaces, the remote control and access to the devices becomes more flexible.

The whole design is functionally extendable, and its high frequency estimation precision of ±0.0005Hz meets most application requirements for wide area power system monitoring and control.

4. IMPROVEMENTS AND ISSUES IN THE FREQUENCY DISTURBANCE RECORDER DESIGN

Different challenges and issues emerged during the system design and implementation of the frequency disturbance recorder. This section discusses the challenges, practical issues, and some possible solutions to the problems encountered.

Sampling rate

It is very important to determine a proper sampling rate for the Frequency Disturbance unit. The measurement accuracy could be jeopardized if there are not enough samples depicting the real input signal, but if you have too many samples the system could be slowed down by too much sampling processing time.

As discussed in section 2, a big part of built-in errors of the algorithm comes from the assumption that the Y term defined in is zero. Assuming the frequency deviation is within ±5Hz, and plotting Y term versus the samples per cycle, N, Figure 3 is obtained. This figure is very helpful for the selection of proper sampling rate.

In can be noted that, for each value of Δf used in Figure 3, the Y term remains fairly stable when N is larger than 24. In other words, an increase of the sampling rate will not help much for the error reduction of the Y term, if the value of N is already larger than 24.

On the other hand, a lower sampling rate means less processing time, hence better real-time performance. So when almost the same accuracy can be achieved, the least samples per cycle are preferable.

A/D conversion

The input voltage digitization is also an important factor for high precision frequency estimation. The analog to digital converter, ADC, is the main component for the input voltage digitization process. In general, the ADC accuracy depends on the two types of conversion errors: quantization and non-linearity. The quantization errors are defined as the difference between the analog signal and the closest sample value to represent it. Quantization error is due to the finite resolution of the ADC, and it is an unavoidable and generally, the magnitude of the quantization error at the sampling instant is between zero and half of one LSB. Quantization errors could also be considered as noise added to an otherwise perfect sample value and its effect is to limit the precision with which a digital sampled signal could represent the original analog signal. This inherent limitation of the ADC process is often expressed as a Signal-to-Noise ratio (SNR),

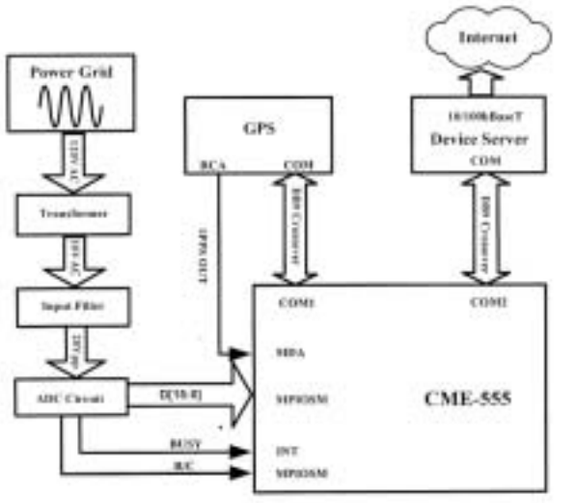

Fig. 2. FDR System Block Diagram

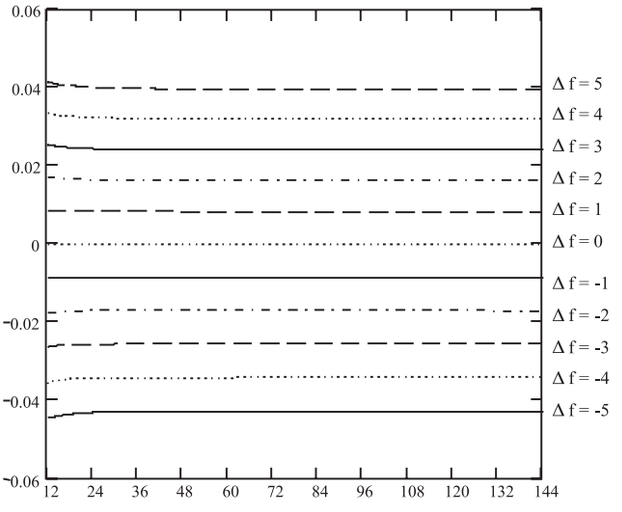

Fig. 3. Y term effects caused by various sampling rates for different

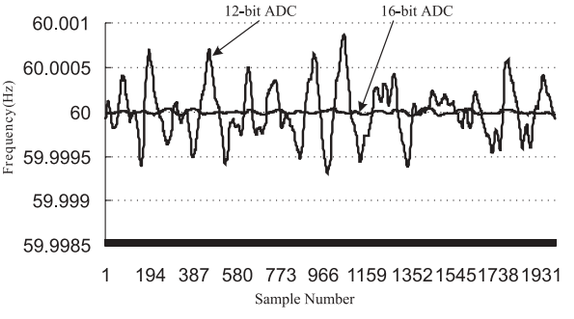

Fig. 4. Quantization noise effects for frequency estimation of different bits ADCs

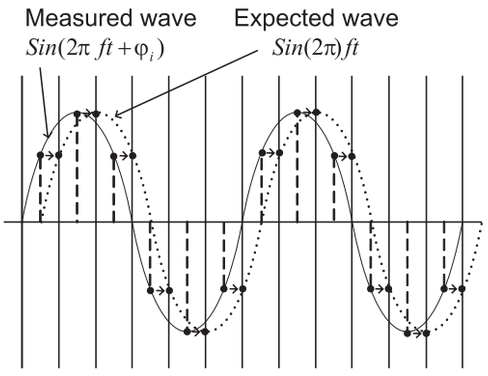

Fig. 5. phase shift caused by unstable A/D conversion signals

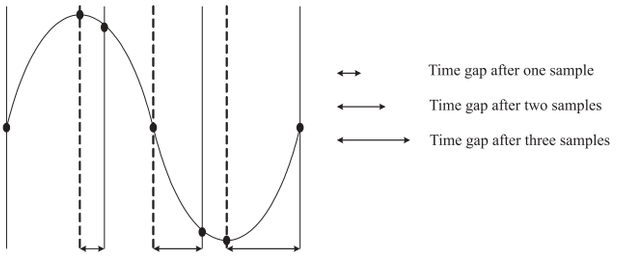

Fig. 6. accumulated phase shift caused by unstable A/D conversion signals

which is the ratio of the RMS signal to RMS noise, which quantization error generates. In terms of the dB scale, the ideal SNR of an R bits ADC is approximately SNR = 6.02R + 1.76 (excluding delta-sigma converters)[10]. Thus, a 16-bit encoding yields a theoretical SNR of 98 dB. Based on this approximation, the quantization noise effects on frequency computation can be estimated, which provides very helpful information for ADC selection. From Figure 4 it can be concluded that a 16bit ADC matches the system accuracy requirement better than a 12bit ADC.

All ADCs suffer from non-linearity errors due to their physical imperfections, causing their output to deviate from a linear function (or some other function, in the case of a deliberately non-linear ADC) of their input. These errors can sometimes be mitigated by calibration or prevented by testing.

Static Phase shift

Ignoring the dynamic phase shift due to the unbalance between the load and generation in transient conditions, some other sources of steady phase shift could exist because of the hardware/software limitations of a real system.

The original algorithm is based on an assumption that the input voltage is a pure sinusoidal waveform and it is digitized by a constant sampling rate. In other words, the algorithm depends heavily on the accuracy of the sampling instants to obtain the right phasor angle. Hence, stability of the A/D clock is crucial to the accurate frequency measurement. In the real world, however, the trigger signal for sampling is only accurate within a satisfactory range. The period and duty cycle of the triggering pulses are controlled by computer program or other electronic devices, and they are only close to the ideal value. In the implementation of frequency measurement device, the A/D conversion trigger pulses could not be exact, and the trivial difference between pulses results in phase shift, which distort voltage waveform samples, as shown in the Figure 5.

If there is any accumulated difference from pulse to pulse for the sampling, the phase shift effects could be even worse. Figure 6, show cases where the voltage waveform samples are very far away from the samples expected by the algorithm.

There are a number of problems which could cause a non-ideal A/D conversion. One way to get a non-ideal conversion is using a sampling scheme based on the Pulse Width Modulation (PWM) output of MPC555 (Motorola 32-bit microcontroller) as the ADC conversion trigger pulse. According to the MPC555 manual, the frequency of PWM pulse is determined by the following formula:

$$f_s = \frac{F_{sys} / PSL}{PERR} \tag{12}$$

where:

F_{sys} — the system frequency 40Mage Hz,
PSL — the Clock pre-scalar, and it's set to 2 in this case,
PERR — the PWM period register value (integer).

Assuming 1440 sample per second (24 samples per cycle for a 60 Hz system) is the desired sampling rate for frequency estimation, the closest sample rates from the PWM output are 1440.092Hz and 1439.885Hz according to , due to the integer requirement of PERR. If one uses the sample rate of 1439.885Hz with the pulse train being regenerated every second synchronized with one Pulse per Second of GPS, there is an abnormal sample at the end of each second as shown in Figure 7. Ignoring other effects and errors, the sampling interval of this abnormal sample can be calculated and it is a constant for a specified system.

To deal with this kind of phase shift, the backup sampling scheme shown in Figure 10 is proposed here.

In this proposal there're two A/D converters used for voltage data sampling, one is the main ADC, and the other is the backup ADC. The two ADCs have the same sampling rate, 1440Hz in this case. At the beginning of each second, the main ADC will be reset and begin the new sampling sequ-

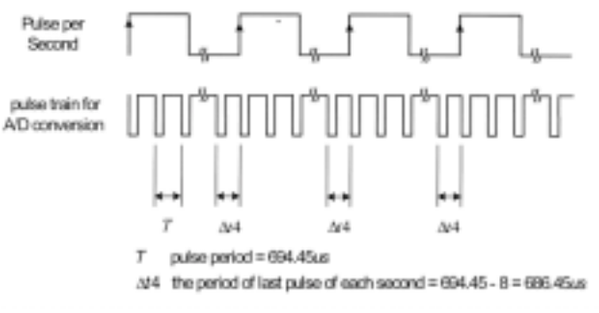

Fig. 7. Pulse Train for ADC Conversion Triggering

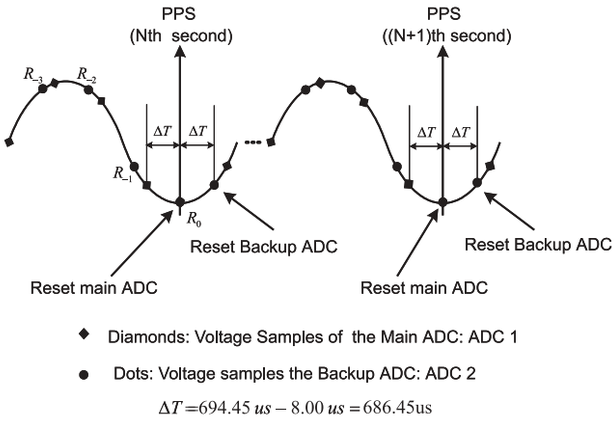

Fig. 8. Backup Sampling

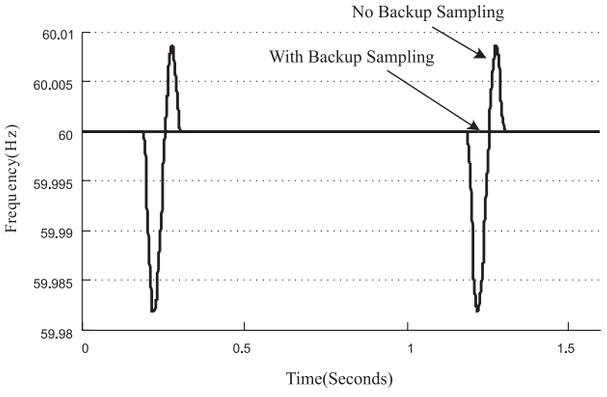

Fig. 9. Measurement results of a 60Hz sinusoidal waveform with the 5% 5th harmonic component

ence for the new second. And 686.45us after main ADC starts sampling, the backup ADC will be reset for sampling. By doing this, the sampling data of main ADC will be synchronized with the PPS exactly for each second, and the backup ADC can provide the no-phase-shift voltage samples for compensation of the phase shift in the first frequency result of each second.

According to the simulation results in Figure 9, by using the backup sampling scheme, the spikes caused by the phase shift, can be almost eliminated even for a none pure sinusoidal input.

Amplitude swing and Harmonics effects

The original algorithm assumes that the input voltage waveform is pure sinusoidal. However, in some transient conditions, the voltage waveform of the real power system may experience amplitude and phase distortion. Some of the causes of such distortions are sudden load variations, transient faults, and line switching. Considering the actual voltage waveform under amplitude swing as having the following form:

$$x(t) = \sqrt{2}X\sin(2\pi ft) + \sqrt{2}Xm\sin(2\pi f_m t)\sin(2\pi ft) \quad (13)$$

where:

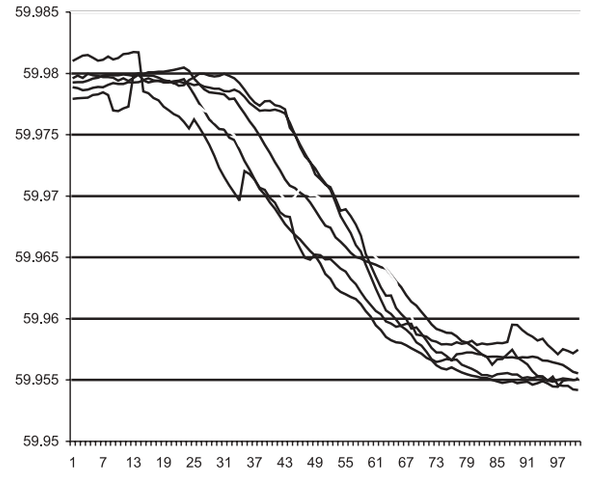

Fig. 10 Frequency curves of EUSS event on Aug. 4, 2004. (At the frequency of 59.975Hz, the order from left is: VT, UMR, ABB, ARI, UFL and MISS)

Fig. 11 . Estimated event location with triangulation analysis

X — RMS value of the signal,
f — fundamental frequency,
m — modulation index, and
f_m — the modulation frequency.

Typically, in a real system the modulation index will be less than 10% while the modulation frequency will be around 1Hz. At the nominal frequency, 60Hz, the estimation error of the frequency is a function of modulation index and modulation frequency, and the gradual effects of the voltage swing are presented in the frequency estimation. More detailed effects of the voltage swing of 10% modulation index and 1 Hz modulation frequency are shown in the Table 1.

Table 1. Errors introduced by amplitude swing of 10% 1 Hz modulation frequency

F(Hz)	57	58	59	60	61	62	63
Max(10^{-3} Hz)	0.46	0.44	0.42	0.41	0.41	0.42	0.42

Table 2. Maximum Measurement errors due to harmonics presence

Harmonic Components (%)	Maximum measurement error for different frequency (10^{-3}Hz)		
	$f = 57$	$f = 60$	$f = 63$
5% 3rd	0.0523	0	0.0592
5% 5th	0.0573	0	0.0771
10% 3rd	0.0593	0	0.0862
10% 5th	0.0693	0	0.122

The simulations results show that frequency estimation accuracy will not change much while the fundamental frequency changes, but the amplitude swing effects cause unacceptable errors in frequency measurement, which needs further study and research.

As it is known, the unfiltered low order harmonics will also be present in the voltage waveform for measuring purpose. The waveform with harmonic component while maintaining the constant operating frequency can be presented as:

$$X(t) = \sqrt{2}X\sin(2\pi ft) + \sum_{i=1}^{N} p_{2i+1}\sin\left(2\pi\left((2i+1)f\right)t\right)$$

where:

X — the RMS value of the signal,

f — the fundamental frequency, and

p_{2i+1} — the $(2i+1)th$ harmonic percentage.

Table 2 shows the effects of these harmonics on the frequency estimation calculation. The more harmonics contents the more maximum measurement errors are observed in the frequency estimation. Compared with amplitude swings, algorithm errors, and other implementation errors, harmonics effects are not so significant because the algorithm itself has a filtering effect for non-fundamental components in the input signal. Even with a more strict accuracy requirement, a simple band pass filter could be applied to eliminate the harmonics components and reduce the measurement errors.

Communication issues

Since wide-area applications are the main targets of FDRs, so the communication is one of the biggest concerns of FDR design.

As far as some specific real-time applications are concerned, such as network control and relaying[11], communication delay, reliability and security could be the bottleneck. Considering the communication delay, even with the Fiber-optic cables, the worst case delay could be above 150 milliseconds[12]. However, this limitation will not affect other possible applications, especially the post processing applications, such as monitoring and model verification.

Recently, the interfacing between FDR and conventional SCADA (Supervisory Control and Data Acquisition)/EMS (Energy Management Systems) become more and more desirable. Data redirecting could be the first and simplest way to try, however it could cause more communication delays and waste much network resources, the connection will be built up always once one communication channel is desired. A better solution is the IP multicasting over IGMP (Internet Group Management Protocol), which allows FDRs broadcaster content to a flexible large number of subscribers effectively. Through IGMP, clients may request to join or leave a certain multicast group at will, and the network traffic is sent only to the clients registered to a specific GDA (Group Destination Address).

5. APPLICATION EXAMPLE OF FDR

There are many applications in power system that could use the wide area, quasi real-time, GPS synchronized frequency measurement provided by FDRs [13-19]. The data can be used to:

— Verify system models and parameters used in simulations;

— Perform post-disturbance scenario reconstruction and track the sequence of events leading to an emergency;

— Understand the fundamental characteristics and mathematics of failure of complex systems;

— Provide wide-area information for improving power system control functions;

— Provide near real-time system status for analyzing the underlying causes of cascading events and system blackouts;

— Study how frequency disturbances travel as electromechanical waves in power systems “frequency wave” travel characterizes analysis;

— Develop algorithms to triangulate generator tripping location and predict trip amount in MW;
— Perform adaptive under-frequency load shedding algorithm using wide-area frequency as inputs;
— Improve FACTS/ESS control in inter-area low frequency oscillation damping;
— Improve ACE accuracy;
— Perform inter-area oscillation modes calculation and prediction;
— Control and coordinate wide area PSSS;
— Control and coordinate Distributed Generation (DG);

The Power Frequency Monitoring Network (FNET) is the wide area monitoring network built on the Client/Server architecture by strategically placing FDRs throughout the whole US. FNET provides frequency measurement data collection, data storage, web service and other information management functionalities.

Here is an example application of FNET. Power engineers have long recognized the finite travel time of electromechanical propagation of disturbances. With frequency information from FDRs in the Eastern system, the location of unexpected events can be estimated by triangulation. The amount of generation change can be estimated by frequency drop. On Aug. 4, 2004, a generator tripped and the frequency of Eastern system declined but the decline start time and the slope of the decline were different at different locations in Eastern system as recorded by the FNET shown in Figure 10.

Just before the event happened, the eastern system frequency was 59.98Hz, and the units of ARI, VT, UMR, and ABB first saw frequency drop at 14:23:8.8 (UTC); then units in MISS and UFL experienced frequency drop after 1 second; at the end, the frequency went down to 59.955Hz at 14:23:12.8 (UTC).

From the delay time difference and the amount of frequency decline, the event location was estimated. Fig.13 shows a dot near Calvin as the estimated event location, while the actual event location is the square spot on the right. The estimation error is fairly small, and could be affected by the frequency wave speed difference in different locations and directions.

The amount of tripped generation is proportional to the average rate of frequency drop and system inertia. A simple relationship of power imbalance, Δp with respect to measured frequency drop rate can be derived based on the previously recorded frequency change and the corresponding known drop amount. In this case, the estimated tripped generation was 786MW, while the actual tripped generation was around 870MW.

6. CONCLUSION

The design of low cost Frequency Disturbance Recorder (FDR) has been proposed and implemented. Based on the analysis of practical issues which affect the performance or accuracy of FDR, some improvements have been achieved to make FDR an ideal device for wide area monitoring. Taking the fully advantages of FDRs, Power Frequency Monitoring Network (FNET) make many power system monitoring and protection applications feasible.

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