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Realization of Picture in Picture System Based on TMS320DM642 Digital Signal Processor

1. Introduction

Autonomous vehicles and many kind of robots act within the human environment today. They are step by step becoming more common in the industrial plants, military plants tasks and hospitals. They are a subject of extensive research and development, scale of projects tends upward. Intelligence factor of contemporary autonomous robots are significant especially with comparison to computational power of existing processors, but the robot still can't perform all required task in heterogeneous of human environment. Robots have limited capability of obstacle detection and object recognition, computation time excludes robot real time reaction. It seems that development of fully autonomous robots capable act in diverse human environment must take some time. In meantime, we should develop system with limited autonomity – semiautonomous systems. The semiautonomous system can perform simple schematics tasks e.g. "go forward", "go to the obstacle" , "run until obstacle", "pass obstacle from the right" . The robot's operator link these tasks into logical sequence steps based on his grasp of the situation. It need full knowledge about the robot environment and obstacle at hand, it need full visual inspection of space around. In this moment we must bring into attention task of multi camera image transmission. Transmitted image should be useful and convenient for the operator, should present surrounding space at best to avoid driving errors and damage of expensive equipment. Lets we define the task: to build system that will be able process in real-time data from 2 to 8 cameras with resolution from 640×480 to 1000×1000 pixels and will be able combine images and send those processed data to the operator. The system should have to offer low power consumption and high performance to fulfill requirements of mobile devices. In this paper authors focus on using digital signal processor from to accomplish this task.

The rest of this paper are organized as follow: Section 2 describe short characteristic of selected digital signal processor (manufactured by TI). Section 3 present general concept of PiP system (Picture in Picture). Sections 4, 5 give software description. Finally, sections 6, 7 draw conclusion.

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2. General description DaVinci Video Processor

Texas Instruments (TI) [11] has wide range of processors to the totality of the solutions used in industry. These processors are used in home electronics, industrial and military space. The most interested members of TI processor is from the following groups [1]:

- DaVinciTM Digital Media Processors – Group DaVinci processors contains scalable, programmable chips System on Chip (SoCs) equipped with accelerators and peripherals. They are widely used for signal processing Video / TV. Processors in this series have a range of peripherals supporting action on the streams of images.
- Highest Performance TMS320C6xxxTM – family single- and multi-core digital signal processors with the highest capacities, designed for network applications, telecommunications and military. Basic subgroups are C64xTM, C67xTM, C647x.
- Power-Efficient/Performance TMS320C5000TM – C5x family offers low power consumption in standby mode and a relatively high-performance computing and advanced automatic power management. They are used in portable devices like music players, VoIP, GPS receivers and portable medical devices. This family of processors are less powerful than previous groups.

Davinci family has the large set of peripherals designed to process video signals so in the remainder of chapter is predestined to PIP application. The rest of the chapter describes processors from the DaVinci family [3][4]:

- Processor TMS320DM6467 is based on SoC technology, is used to transcode in real time, multi-wide format TV signals, high-definition (HD). Compared to previous generations of processors, DM6467 offers a 10-fold increase in concurrent, multi-wide format encoding, decoding and transcoding to H.264 HP@L4 (1080p 30fps, 1080i 60fps, 720p 60fps). It is used as a device for translation data streams from various types of telecommunication networks, digital media adapters, as a digital video recorder or digital video server in commercial buildings, IP STBs (set top boxes).
- Processors TMS320DM644x are highly integrated systems based on a hybrid multicore technology have in their composition general-purpose processor cores and ARM926 core of digital signal processor TMS320C64+. They are used in devices such as IP video phones.
- Processors TMS320DM643x/DM642x – are based also on the TMS320C64x +TM core. They are recommended for consumer devices, where low cost is critical. Application field includes safety devices, automotive safety devices alerting driver when crossing through lanes, or alerting before the collision, video-phones, robotics
- Processors TMS320DM64xTM – Overall DM64x family are designed for high performance data processing applications to imaging. They offer the highest performance for the most demanding streaming applications
- Processors TMS320DM3x – have a core of ARM9 processor and video subsystem (video processing subsystem – VPSS). Flag product from the family the DM335 processor is characterized by a low price and low power consumption. It is used in devices

for video display, which is not required compression and decompression. Is the best choice for devices such as IP camera, video-ringtone, portable media, etc.

– TMS320DM37x digital media processors – is the latest family of processors delivers solutions that combine low power consumption and best performance in the class of ARM processors and graphics accelerators.

Our choice is DM642 processor due in availability on market and relatively low price. Another factor is as existence of well prepared evaluation boards. Based on DM642 and evaluation boards we have prepared the prototype system, as well as target system.

3. Picture in Picture concept in Robot vision

PiP system is well known from television sets. PiP combines images from two channels and displaying them on a single monitor. One of the images is primary image and it is displayed in full screen. The second one is the secondary image that is reduced and displayed as a rectangle in one of the corners of the main image. The sound usually comes from the main image. Television sets typically operate on analog data [5, 6, 7, 8] and use specific chips. Such solution has one great advantage the price. The analog PIP chips cannot combine signals from 3 or more sources. It is impossible to chose destination rectangle of secondary image, all sources should be with same resolution (PAL, SECAM, HD) In our robotic application this set of restrictions is unacceptable.

For the purpose of robot guiding application [9, 10] authors extend the concept of a PiP as they can connect up to 8 cameras. An additional option is the possibility of combining cameras with different characteristics: for example, color and black/white cameras and cameras with different resolutions. Author's concept of the PiP system for mobile robot, it should be implemented as follows (Fig. 1).

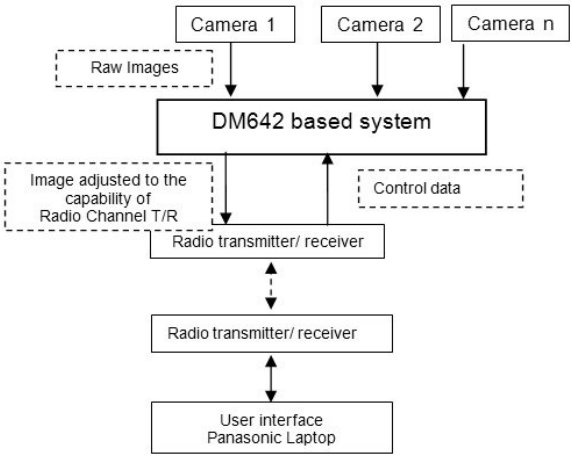

Fig. 1. Block diagram of target system

Fig. 2. User interface image composited from the different cameras

The composite image is displayed on the remote console attached to the system through radio connection. In prototype system Panasonic CF19 laptop acts as a console. The laptop is equipped with multiband multichannel radio communication systems and an touch screen. Images 2, 3, 4 are touch-active. Pressing them makes them the primary image. With this capability the robot's operator can choose between front or rear or side view camera or infrared camera. Number of secondary images displayed depends on number of cameras attached to the system. No more than four images are displayed at a time.

Target system has been build with a prototyping development method. First prototype of the system was build based on DM642 Evaluation Module (EVM) in the configuration shown in Figure 3. The board has two WATEC (WAT-202D) cameras attached to the VideoPorts. One camera plays role of the front camera other one the rear. Software solutions described in following sections utilizes this configuration.

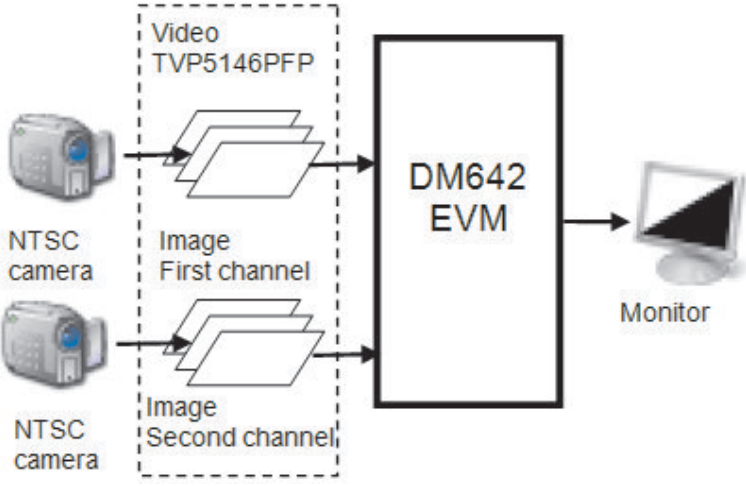

Fig. 3. Prototype system architecture

There are two methods of combining images into the compose signal depicted on Figure 2:

– the filling of the images by the processor action
– the filling of the images using Enhanced Direct Memory Access (EDMA) system, with minimal activity of CPU. Both method was implemented and compared according to the power consumption and scalability.

4. Processor's implementation of Picture in Picture

In Figure 4 are presented the main steps of the procedure for combining images from two cameras using a digital signal processor without the use of peripheral devices. Each of the following operations are performed by processor's ALU.

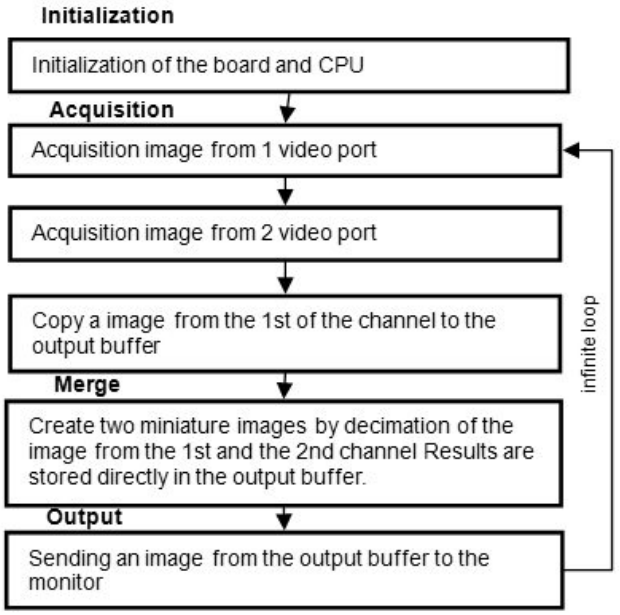

Fig. 4. Processor implementation of Picture in Picture

4.1. Initialization

The following tasks are performed in the initialization stage:

– Initializing DSP BIOS and library Chip Support Libraries (CSL),
– Initializing memory L2 cache,
– Enable caching in memory EMIF C0 i C1,
– Initialization module DMA,
– Initialization module FVID.

4.2. Acquisition

During acquisition step video data is acquired from the video ports. Two images are acquired using FVID module supplied by TI. Full description of module can be found in Driver Developed Kit [13].

4.3. Merging of images

In the next step primary image is copied into the output buffer. In general it is transferred to the output buffer with decimation required by output resolution adjustment but in prototype system decimation can be omitted as input cameras are in TV format. In the second step, two overlapped images are created. Image from the first channel is decimated and stored in the programmed part of the output buffer, than the second image is processed. Decimation paradigm is depicted on Figure 5.

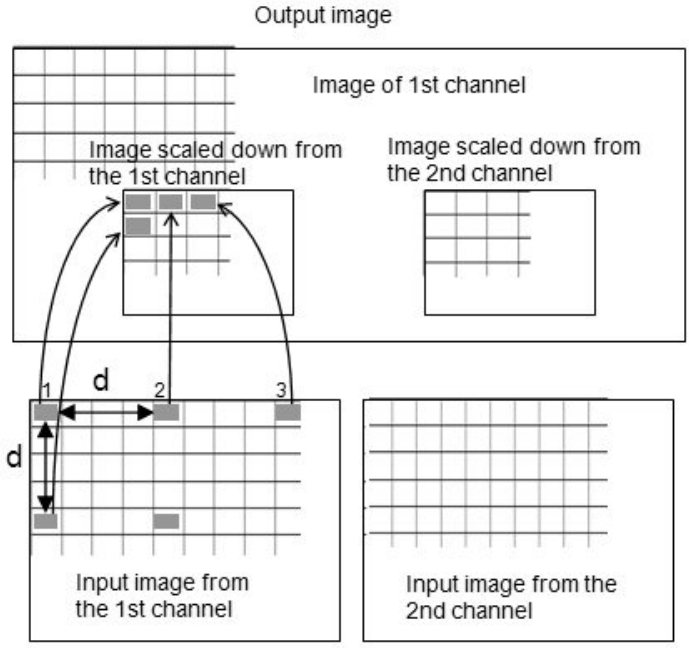

Fig. 5. Copy the selected pixels in the image of the 1st and the 2nd channel to the output buffer, d – number of pixels

4.4. Output

The last step is to send the image from the output buffer to the output port.

This procedure causes monitor attached to the DM642 EVM to show real-time image. On the entire screen is an image of the 1st channel. In addition, two smaller windows are displayed with images of the 1st and 2nd channel (Fig. 5).

This procedure consumes majority of processor time to simple movement of data from one memory location to another, so it can be subject of optimization.

5. EDMA based optimized PiP algorithm

In the Figure 6 we present main steps of optimized image merging procedure. Most important aspect of optimization is extensive use of EDMA channels to video data transfer. Enhanced Direct Memory Access system is burdened with block transfer tasks and frees up ALU to perform more advanced tasks.

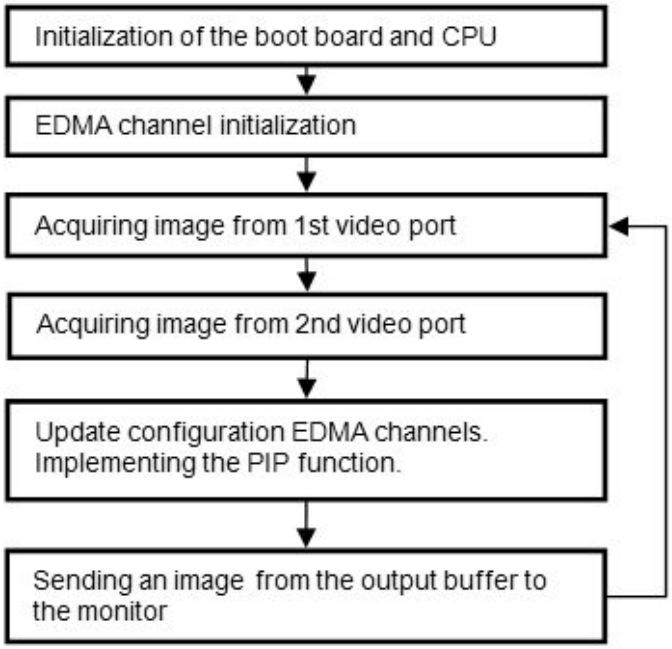

Fig. 6. Implementation of Picture In Picture with the EDMA controller

EDMA system implemented in TI processors can work independently from the ALU of processor. This feature makes it the another parallel computational system. The main task of the EDMA is to transfer block of data from one location in memory to another or even reconfigure other peripherals by writing to its configuration ports. EDMA has reach set of modes, and triggering event so it fits ideally to task of image merging (Tab. 1). DM642 processor has 64 independent channels in the EDMA system. Every channel can be configured on demand.

Table 1
EDMA configuration parameters

OPT	
SRC	
FRCMT	ELECNT
DST	
FRIDX	ELEIDX
ELERLD	LINK

EDMA Channel Options Parameter (OPT)
EDMA Channel Source Address (SRC)
Array/frame count (FRCMT), Element count (ELECNT)

EDMA Channel Destination Address (DST)
Array/frame index (FRIDX), Element count (ELEIDX)
Element count reload(ELERLD), Link address (LINK)

The most important register is the OPT register (Tab. 2). It defines mode of operation in bitwise mode.

Table 2
Channel Options Parameter (OPT)

PRI	ESIZE	2DS	SUM	2DD	DUM	TCINT	TCC
TCCM	ATCINT	ATCC	PDTS	PDTD	LINK	FS	

With it we can set:

PRI – priority level for EDMA events,
ESIZE – size of the element to transfer,
2DS, SUM – source address update mode,
2DD, DUM – destination address update mode,
TCC, ATCC, TCINT, ATCINT – transfer complete code and interrupt,
LINK – linking of EDMA channels into the sequences.

The process begins with an order issued by the processor to EDMA. Since then, the EDMA performs the following tasks in sequence:

Step 1 – it copies input buffer of primary image to the output buffer. Due to 3 separate planes of color image 3 separate EDMA channels performs this task

Step 2 – Decimation of secondary images. EDMA channel copies the data from the source block to the destination. Destination address increments with each data item. Source address is incremented by decimation factor (content of ELEIDX register) (Fig. 7).

Step 3 – Transfer from temporary buffers into the output buffers. At this stage EDMA overwrites a selected portion of the output buffer pixels with a temporary buffer created in Step 2.

Color image has component Y, Cr, Cb so every color channel is processed in parallel with different EDMA channels. Every set employs the above scheme. The end result is the output image shown in Figure 7.

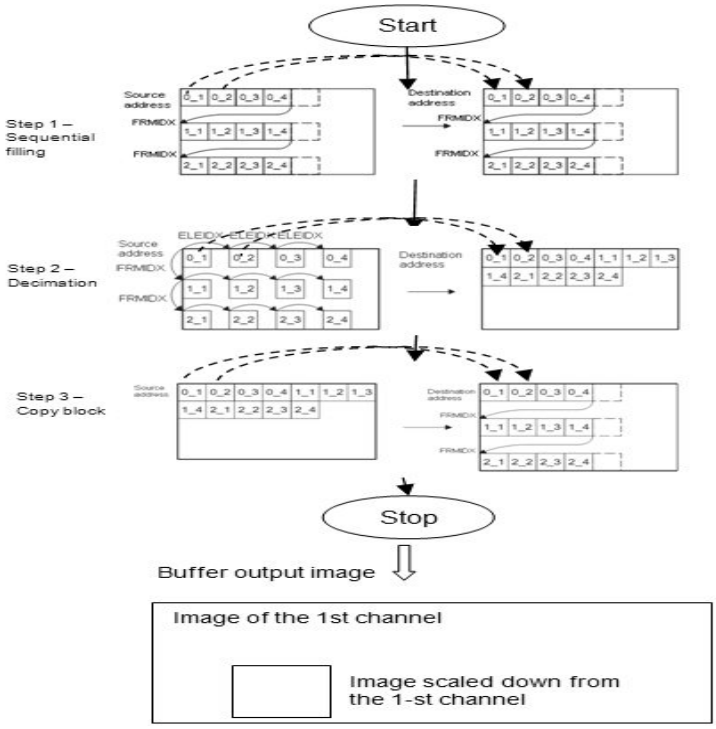

Fig. 7. Schematic image filling the output buffer for using the EDMA controller

6. EDMA configuration sets

In this chapter we present exemplar configurations of EDMA channels.
Step 1 – sequential filling

Table 3
Channel Options Parameter (OPT)

3	0	1	1	1	1	1	TCC	TCCM	0	0	0	0	1	1

Table 4
EDMA Channel Parameters

OPT	
Source address	
HEIGHT – 1	WIDTH / d
Destination address	
0	Don't care
Don't care	Link address

Step 2 – decimation

Table 5
Channel Options Parameter (OPT)

1	2	0	3	0	1	1	TCC	TCCM	1	ATCCA	0	0	1	1

Table 6
EDMA channel parameters

OPT	
Source address	
HEIGHT/d – 1	WIDTH / d
Destination address	
WIDTH * d	d
Don't care	Link address

HEIGHT, WIDTH – means respectively width and height of the component YUV.

7. Results

Figure 8 has been posted a screenshot of Picture in Picture achieved by the method described above.

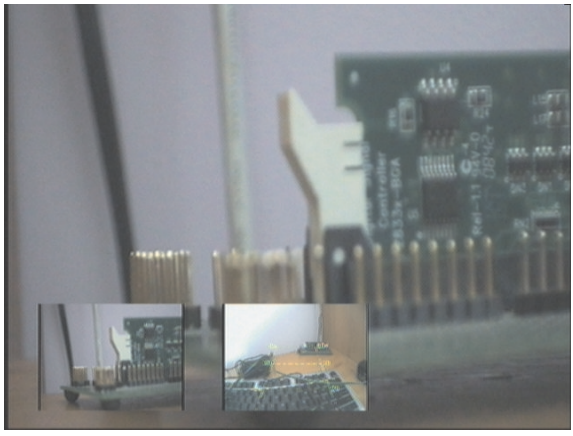

Fig. 8. The results of the system Picture in Picture on digital signal processor using the EDMA system

Both methods were compared in terms of CPU load. EDMA decrease CPU load by 50%. Below (Fig. 9 and 10) we present data collected by means of the CPU Load Graph.

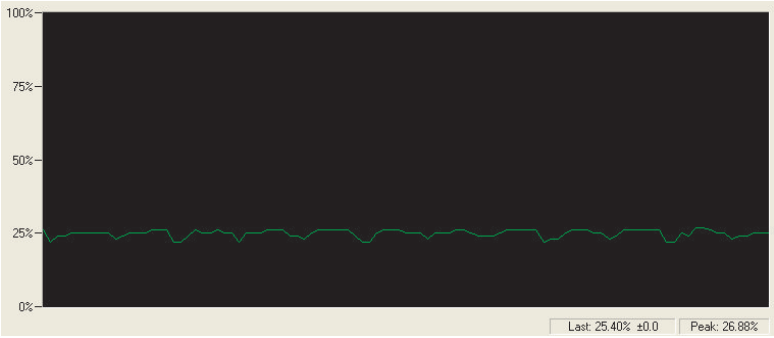

Fig. 9. CPU utilization with EDMA based PiP algorithm

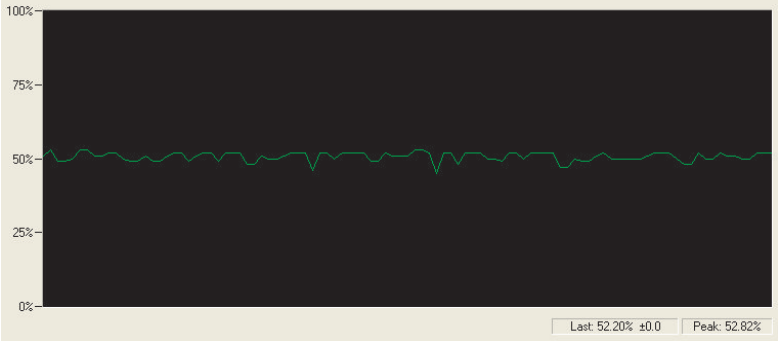

Fig. 10. CPU utilization whit processor based PiP algorithm

Of course further optimization in EDMA procedure are possible, but with this solution load of the system is about to 25% that's indicate that the system expansion up to 8 cameras is unthreatened.

The EDMA based software helps to reduce energy consumption and to suspend the CPU on idle time. It is important factor in battery powered systems. Current version of software do not idle the processor so the power consumption increases slightly The result has been measured using the Fluke 115 meter, the accuracy class is 0.01% (Tab. 7).

Table 7
Power consumption of the platform, platform DM642 Evaluation Module (EVM) for each of the implemented methods of implementing the PiP system

The method of realizing a system PiP	Current [A]
Processor	~0.23
EDMA	~0.24

8. Results

This article presents the implementation of Picture in Picture with using TMSDM 642 processor with 720 MHz processor. Two methods have been tested to implement this functionality: processor's method and EDMA method. Load of CPU with processor method indicates that the processor can process up to four cameras at a time. The EDMA hardware method allows you to increase system capability up to 8 cameras. The presented results show that the use of systems EDMA considerably less CPU usage while running the application and frees the CPU for a more advanced operations on the image.

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