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Performance and Stability Analysis of Series-Cascaded, High-Gain, Interleaved Boost Converter for Photovoltaic Applications

Research Article

C. Prasanna Kumar, N. Venugopal

Department of Electrical Engineering, PES Institute of Technology, Bangalore, India

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Abstract: Interleaved boost converters (IBCs) are cascaded in parallel in most of the applications. This novel approach connects IBC in series cascade. The IBC has an optimal operating duty cycle of 0.5. Normally, photovoltaic source voltage is low because of space constraints. In order to boost the source voltage, a conventional boost converter is replaced with series-cascaded IBC in this paper. The single-stage IBC also boosts the voltage to twice the input voltage. In the proposed converter, output voltage is about four times the input voltage with the same 0.5 duty cycle. A mathematical model is developed and simulated for the proposed work in MATLAB/Simulink platform. The output of the proposed circuit is analysed through fast Fourier transform to know the harmonic content due to the switching. The system is tested for stability with signal-flow graph modelling. The proposed work is realised using hardware and tested to validate the model.

Keywords: *series cascade • interleaved boost converter • high gain • stability • fast Fourier transform*

1. Introduction

Renewable energy sources (RES) such as wind and solar and geothermal power are becoming more popular because of increasing load energy demand and the environmentally friendly nature of these sources. The output voltage available from RES is variable and unregulated. Power electronic converters are needed to boost and regulate the voltages obtained from the RES. Many applications such as electric motor drive, uninterrupted power supply (UPS), aircraft, communication, medical equipment, electric vehicles and hybrid electric vehicles require more initial voltage and current as discussed by Cabral et al. (2013) and Van der Broeck and Tezcan (2006). The classical boost converter is not a preferred option for medium- to high-rated applications due to limitations on the duty cycle (D). The voltage and current stress on switching devices increase with D and also the reverse recovery problems of the power diodes as compared by Huber et al. (2009), Smith and Mc Cann (2014) and Wen et al. (2006). Interleaved boost converters (IBCs), with their superior performance, are replacing conventional boost converters in the last decade. The advantages of IBC are reductions in the size of the inductor, increase in efficiency, better transient response, reliability, suitability for operation at high temperature and higher power handling capability, which were analysed by Chen et al. (2001), Miao and Fang (2006) and Veerachary (2004). A recent study by Xu et al. (2009) suggests that a DC–DC boost converter without transformer overcomes the problem of circulating current and electromagnetic interference (EMI) for high rating applications. The voltage multiplier cells, which are a combination of diodes and capacitors, are arranged in order to obtain high output voltage with zero voltage switching and zero current switching. The diodes of IBC are replaced with silicon carbide (SiC) devices so that the reverse recovery problems are avoided, and metal oxide semiconductor field effect transistor (MOSFET) s are replaced by cool MOSFETs so that there is an improvement in the efficiency (Ho et al., 2011). An IBC with complementary metal oxide semiconductor (CMOS) technology and four phases is the two-phase coupled inductor bidirectional IBC.

* *Email: cpkme@yahoo.com; venugopaln@pes.edu*

This coupled IBC with direct or reverse coupled inductor has a limitation that its inductor may get saturated for high rating applications as described by Freitas et al. (2015).

The IBC with a duty cycle of 0.5 has the major advantage that inductor ripple current is almost zero. However, the boosted output voltage will be only twice the input voltage. When the source voltage is low, in order to increase voltage gain further, diode–capacitor voltage multipliers are used. However, the voltage multiplier may degrade the performance of the converter (Kim et al., 2011). The reverse coupled topology may reduce the effect of circulating current at the cost of a bulky and expensive filter. A high-value capacitance is required to ensure that the stored energy is supplied at a constant output voltage. The converter dual IBC can improve the capability of handling high-power analysis (Everts et al., 2012; Kim et al., 2014).

All systems with medium to high rating are designed to work in continuous conduction mode (CCM) so that current ripple can be minimised with proper selection of inductor and switching frequency. The primary advantage of CCM compared to discontinuous conduction mode (DCM) of operation is the minimisation of inductor current ripple and voltage ripple effects. In CCM operation, the voltage gain remains the same as that of the conventional boost converter (Chang et al., 2012; Zhang et al., 2012; Zhao et al., 2012).

The current source driver (CSD), with four switches connected in the form of a bridge and intermediate inductors used with the main switch of IBC interpretation (Zhang et al., 2014), uses digital signal processor (DSP) for closed loop control operation of converter. When the requirement of power rating is more than 300 W, average current mode (ACM) with classical boost is preferred. This has better efficiency, and its performance will be improved with pulse width modulation (PWM) control. It is concluded from simulation that coupled inductor does not have any effect on ripple current, but it has control over the circulating current. When the source is renewable, a converter other than IBC is not advisable since the converters introduce more ripple at the input during their operations (Jung et al., 2010; Rahavi et al., 2012; Zhang and Yu, 2013).

2. The proposed two-stage series-cascaded IBC

In order to minimise output voltage ripple and to increase the output voltage to nearly four times the input, a novel two-stage series-cascaded IBC is proposed. Figure 1 is the circuit diagram of the proposed two-stage series-cascaded IBC.

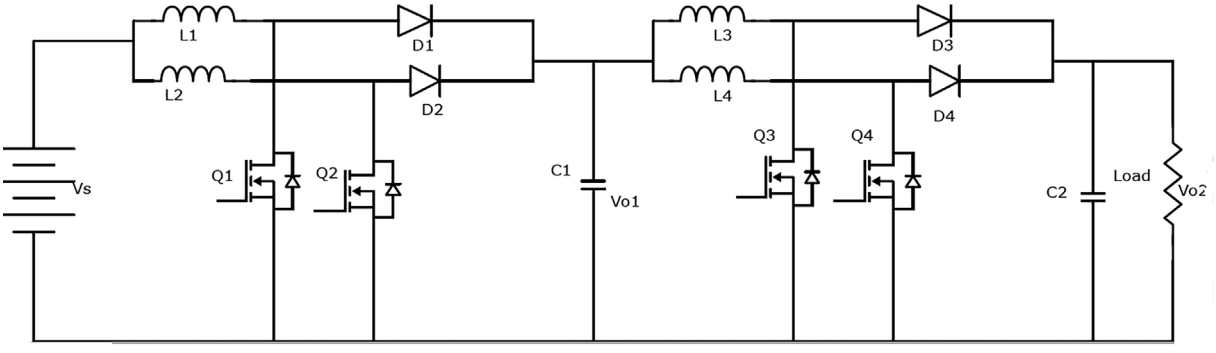

Fig. 1. Proposed two-stage series-cascaded IBC

In the proposed circuit, IBCs are cascaded such that the output of the first stage (V_{01}) serves as the input to the second. The output of second stage is high DC voltage (V_{02}). The capacitor at the output of stage 1 acts as a filter and as a DC link capacitor and also maintains a constant DC input to the stage 2. The gating control circuit is implemented separately for the two stages, and in each stage, the gating pulses should have a phase shift of 180°.

2.1. Operation of proposed circuit

The operation of the above circuit is divided into three modes of operation. The first two modes correspond to the alternative switching of the interleaved MOSFETs. The third mode is when both switches conduct simultaneously, that is in a case of duty cycle D >0.5. The case of non-conduction by either of the switches

(D<0.5) is not considered since only CCM operation has been considered for the IBC. The three modes of operation are as follows:

Mode 1: Q_1 is ON, Q_2 is OFF, D_1 is OFF, D_2 is ON and Q_3 is ON, Q_4 is OFF, D_3 is OFF, D_4 is ON.

The equivalent circuit diagram is shown in Fig. 2. The energy stored in the inductor L_2 from the previous switching interval is transferred onto the second stage, whereas the inductor L_1 stores energy from the DC input source through Q_1. Similarly, in the second stage, inductor L_3 stores energy from the output of the stage 1, whereas the energy stored in L_4 from the previous cycle is transferred onto the output side so as to maintain the DC link voltage, and this cycle repeats periodically. The expressions for capacitor voltages and inductor currents are obtained as given in equations (1)–(6). The input voltage is V_{in}; V_{01} and V_{02} are the output voltages of stages 1 and 2, respectively. The input current i_{in_1} is drawn from the supply, and i_{L_1} and i_{L_2} are the currents through L_1 and L_2, respectively. Similarly, currents through L_3 and L_4 are i_{L_3} and i_{L_4}, respectively.

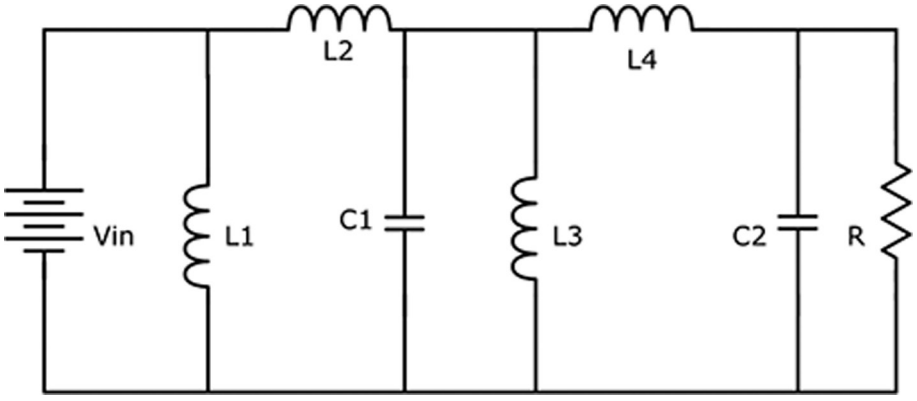

Fig. 2. Equivalent circuit for mode 1 of the operation

$$i_{L_1} = \frac{1}{L_1}\int V_{in}dt \tag{1}$$

$$i_{L_2} = \frac{1}{L_2}\int \left(V_{in} - V_{01}\right)dt \tag{2}$$

$$i_{L_3} = \frac{1}{L_3}\int V_{01}dt \tag{3}$$

$$i_{L_4} = \frac{1}{L_4}\int \left(V_{in} - V_{02}\right)dt \tag{4}$$

$$V_{01} = \frac{1}{C_1}\int \left(i_{L_2} - I_{in_2}\right)dt \tag{5}$$

$$V_{02} = \frac{1}{C_2}\int \left(i_{L_4} - I_{02}\right)dt \tag{6}$$

Mode 2: Q_1 is OFF, Q_2 is ON, D_1 is ON, D_2 is OFF and Q_3 is OFF, Q_4 is ON, D_3 is ON D_4 is OFF.

The equivalent circuit is shown in Fig. 3. This mode is complimentary to mode 1. The energy stored in inductor L_1 from the previous cycle is passed on to the second stage, whereas the inductor L_2 now stores energy from the DC input source. In the same way, in the second stage, inductor L_4 stores energy from the output of stage 1. The energy stored in L_3 from the previous cycle is transferred onto the output side so as to maintain the DC voltage. This mode is followed by mode 1, and the cycle repeats. The expressions for inductor currents and capacitor voltages are obtained as given in equations (7)–(12).

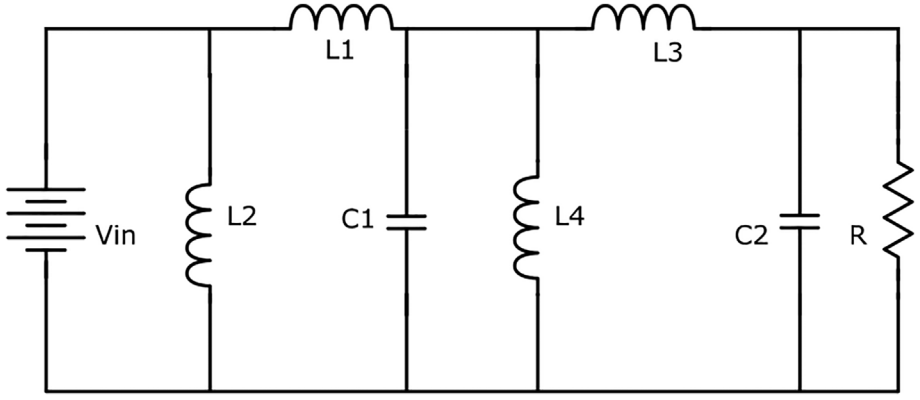

Fig. 3. Equivalent circuit for mode 2 of the operation

$$i_{L_1} = \frac{1}{L_1}\int \left(V_{in} - V_{01}\right)dt \tag{7}$$

$$i_{L_2} = \frac{1}{L_2}\int V_{in}dt \tag{8}$$

$$i_{L_3} = \frac{1}{L_3}\int \left(V_{in} - V_{02}\right)dt \tag{9}$$

$$i_{L_4} = \frac{1}{L_4}\int V_{01}dt \tag{10}$$

$$V_{01} = \frac{1}{C_1}\int \left(i_{L_1} - I_{in_2}\right)dt \tag{11}$$

$$V_{02} = \frac{1}{C_2}\int \left(i_{L_3} - I_{02}\right)dt \tag{12}$$

Mode 3: Q_1 and Q_2 are ON, D_1 and D_2 are OFF and Q_3 and Q_4 are ON, D_3 and D_4 are OFF

The equivalent circuit for this mode is shown in Fig. 4. When the duty cycle D is >0.5, the gating pulses for the interleaved switches may be such that there will be a certain duration during which both the switches Q_1 and Q_2 will be ON. In such a condition, the corresponding inductor current and capacitor voltage equations are obtained as given in equations (13)–(18).

$$i_{L_1} = \frac{1}{L_1}\int V_{in}dt \tag{13}$$

$$i_{L_2} = \frac{1}{L_2}\int V_{in}dt \tag{14}$$

$$i_{L_3} = \frac{1}{L_3}\int V_{01}dt \tag{15}$$

$$i_{L_4} = \frac{1}{L_4}\int V_{01}dt \tag{16}$$

$$V_{01} = \frac{1}{C_1} \int -\left(i_{L_1} - i_{L_4}\right) dt \tag{17}$$

$$V_{02} = \frac{1}{C_2} \int -\left(I_{02}\right) dt \tag{18}$$

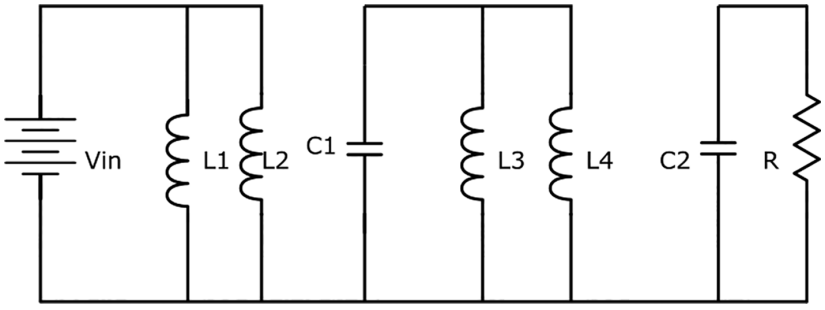

Fig. 4. Equivalent circuit for mode 3 of operation

2.2 Development of a novel mathematical model

With a use of above mathematical equations, the novel mathematical model is developed. The simulation of the schematic circuit on MATLAB/Simulink was observed to be highly dependent on the simulation solver employed and also on the simulation run time. In order to overcome this, the topology has been translated into a mathematical model using the mathematical expressions derived from the various operating modes of the circuit. To realise the developed mathematical model, only the blocks from the Simulink tool have been used, which makes the topology independent of both simulation solver and the runtime. It is to be noted that the mathematical model so developed is at a steady state. The proposed work simulation circuit is shown in Fig. 5. The result from the simulation of the above mathematical model is presented, and it also verifies the design of the proposed cascaded IBC.

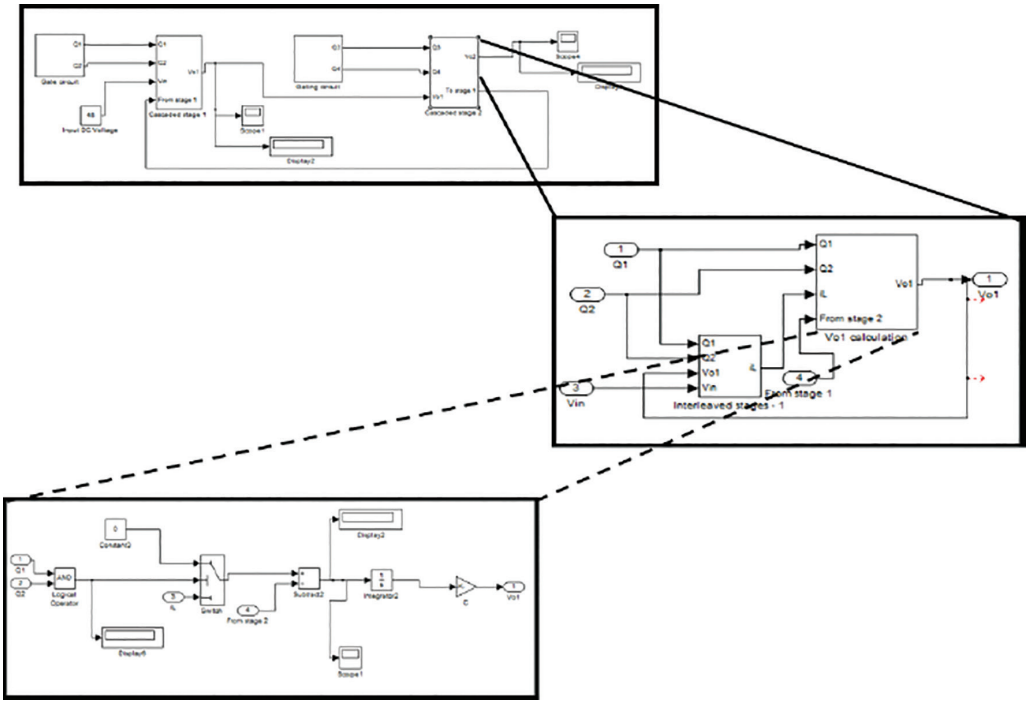

Fig. 5. Overview of the mathematical model developed on MATLAB/Simulink

2.3 FFT analysis for output voltage

Harmonics are those frequency components that are superimposed on the original/main frequency component. Harmonics can be either even or odd. Presence of harmonics in any electrical system is always detrimental in many ways. It overheats the components, causes the malfunctioning of the devices and causes overall deterioration in the power quality of the system. In the case of a DC–DC converter, the output should be free from harmonics, whatsoever the order; hence, the harmonic analysis of the output voltage waveform is carried out; the technique of fast Fourier transform (FFT) is used. FFT is an algorithm used to compute discrete Fourier transform at a much faster rate. It basically transforms waveform from the time domain to frequency domain. With this technique, it is possible to estimate the amplitude of fundamental component and the harmonics to a fair accuracy.

The simulated output voltage is subjected to FFT analysis to find the harmonic content in the output voltage waveform. It is carried out on MATLAB/Simulink environment using the FFT block set. The fundamental frequency chosen is 40 kHz. A sampling time of 1 μ sec is chosen, and the waveform is analysed up to 12th-order harmonic component. It has been found that the output voltage is free of any harmonic component and has a pure DC voltage of magnitude about 200 V at zero frequency. The harmonic spectrum of the FFT analysis is shown in Fig. 6.

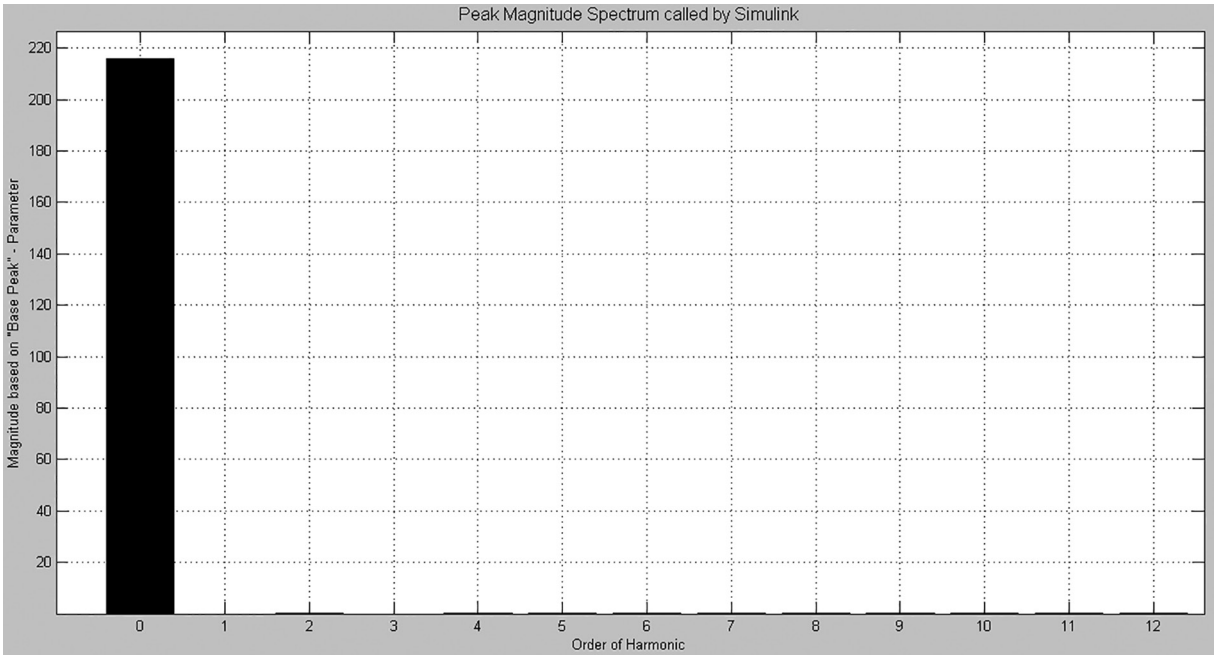

Fig. 6. Harmonic spectrum from FFT analysis of the output voltage waveform

2.4 Signal-flow graph modelling and stability analysis

It is desirable to estimate the stability of the converter in an open loop in order to select the closed loop gain. To do so, the transfer function is the essential ingredient in any stability analysis technique. Henceforth, to find the transfer function of the proposed topology in the open loop, the method of signal-flow graph is selected.

2.4.1 Signal-flow graph modelling

To model the DC–DC converters, the most popular approach is the state-space averaging technique. However, this technique becomes very complicated, especially for converters like the current one that has more number of passive components and non-linear switches. Added to this, the linear model from the state-space approach suffices for only small signal stability analysis and not for either the large signal stability analysis or the steady-state analysis. Thus, a non-linear method of signal- graph (SFG) of non-linear modelling approach proposed has been

used in the present work. This specialised method for modelling PWM converters offers many advantages. To name a few, i) multi switch converters can be modelled with ease and ii) it is possible to draw the small signal model, large signal model and also steady-state models from the unified SFG non-linear model.

The generalised algorithm followed in developing the SFG model for the proposed topology is summarised as follows:

- The order of the nodes in the SFG is in the order of the elements connected in the circuit, such as inductors and capacitors.
- In case of inductive element, voltage node is drawn first and then the current node, and for a capacitor, the current node is first followed by the voltage node.
- Circuit loop equations are written for individual loops using Kirchhoff's voltage law.
- At junctions, the parallel branch currents are obtained using Kirchhoff's current law.
- The inductive and capacitive node forms a forward path transmittance of –1.
- The switching function depends on the operating modes of the circuit.
- The unified SFG for two-stage cascaded IBC is developed using two different unified SFGs for a two-cell topology-unified SFG model for cascaded boost converter and unified SFG model for IBC.
- Then, the resulting unified SFG for the proposed topology is solved for transfer functions. Forward paths are identified, and loop gains are found. The transfer function from this SFG is found using the following standard expression of Mason's gain formula:

$$T,F = \frac{P_k \times \Delta_k}{\Delta}$$

where P_k is gain of the kth forward path, Δ is a determinant of SFG (loop gains) and Δ_k is the Δ for all those loops that are not touching the kth forward path.

The transfer function obtained using the above algorithm is as follows:

$$T,F = \frac{a+b}{\left(s^4 * c\right)+\left(s^3 * d\right)+\left(s^2 * e\right)+\left(s * f\right)+g}$$

where $a = R \times L_2 \times L_4 \times k_1^2$, $b = R \times L_1 \times L_3 \times k_2^2$, $c = R \times L_1 \times L_2 \times L_3 \times L_4 \times C_1 \times C_2$, $d = L_1 \times L_2 \times L_3 \times L_4 \times C_1$, $e = (R \times L_1 \times L_3 \times L_4 \times C_2 \times k_2^2) + (R \times L_2 \times L_3 \times L_4 \times C_2 \times k_1^2) + (R \times L_1 \times L_2 \times L_4 \times C_1 \times k_1^2) + (R \times L_2 \times L_3 \times L_1 \times C_1 \times k_2^2)$, $f = (L_1 \times L_3 \times L_4 \times k_2^2) + (L_2 \times L_3 \times L_4 \times k_1^2)$ and $g = 0$.

With these expressions, the open-loop transfer function of the converter is developed. Using this transfer function, a Bode plot is obtained from MATLAB.

2.4.2 Stability analysis

Any system is said to be stable if it has a positive gain margin (GM) and phase margin (PM). In addition, for a stable system, the phase crossover frequency is found to be more than the gain crossover frequency. The Bode plot is obtained for the proposed topology in the open loop. It is shown in Fig. 7. It is clear from the plot that both GM and PM are positive, and also, the phase crossover frequency is greater than the gain crossover frequency. Hence, it can be concluded that the system in the open loop is stable.

3. Simulation of proposed series-cascaded IBC

The proposed topology, which has been designed as per the requirements, is implemented on MATLAB/Simulink. Simulation is carried out in both schematic environments and using the mathematical model; the simulation results are tabulated in Table 1.

Figure 8 shows the simulation circuit with Simulink; waveform of the output voltage of both the stages is obtained using mathematical model as shown in Fig. 9. It shows an average value of around 109 V and 216 V for the two stages, respectively, and a ripple of <0.01 V and almost same values are obtained with circuit connection as shown in Fig. 10.

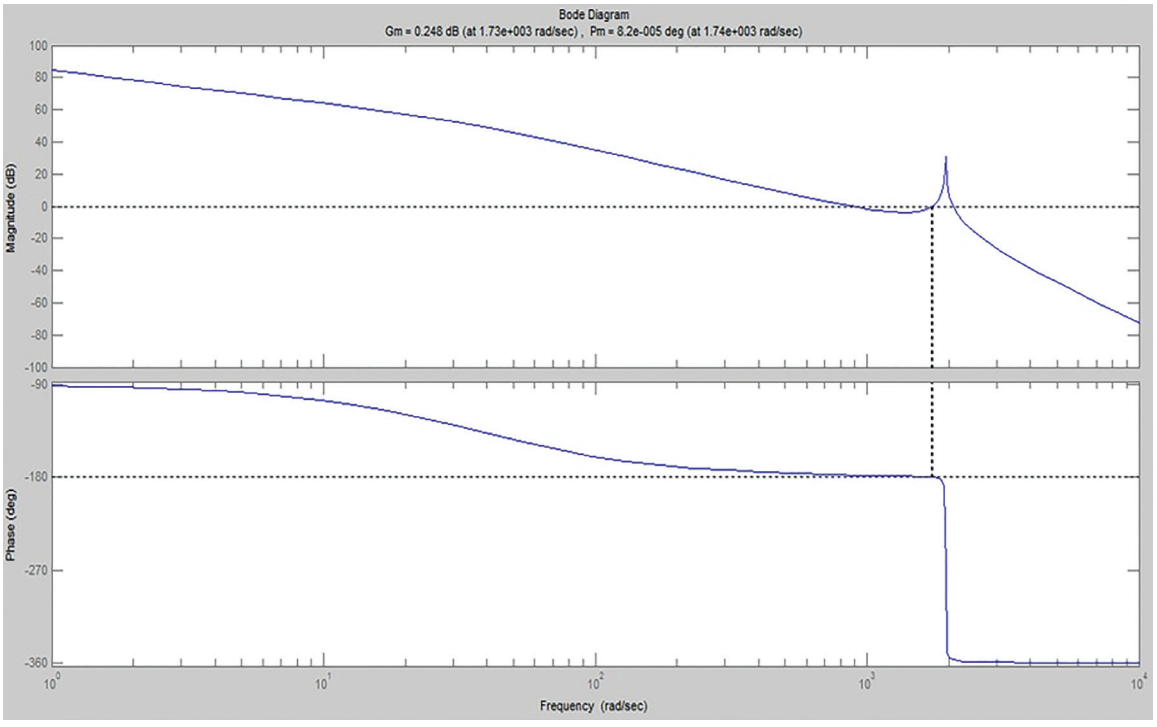

Fig. 7. Bode plot of the converter system showing magnitude plot and phase plot

Table 1: Values obtained from simulation

Simulated parameter	Simulated value
Stage 1 Output voltage, V_{01}	109 V
Stage 2 Output voltage, V_{02}	216 V
Stage 1 Inductor currents, i_{L_1} and i_{L_2}	4.6 A (average)
Stage 2 Inductor currents, i_{L_3} and i_{L_4}	2.2 A (average)
Stage 1 Inductor current ripple, Δi_{L_1} and Δi_{L_2}	0.4 A (peak–peak)
Stage 2 Inductor current ripple, Δi_{L_3} and Δi_{L_4}	0.2 A (peak–peak)
Output voltage ripple	0.01 V (peak–peak)

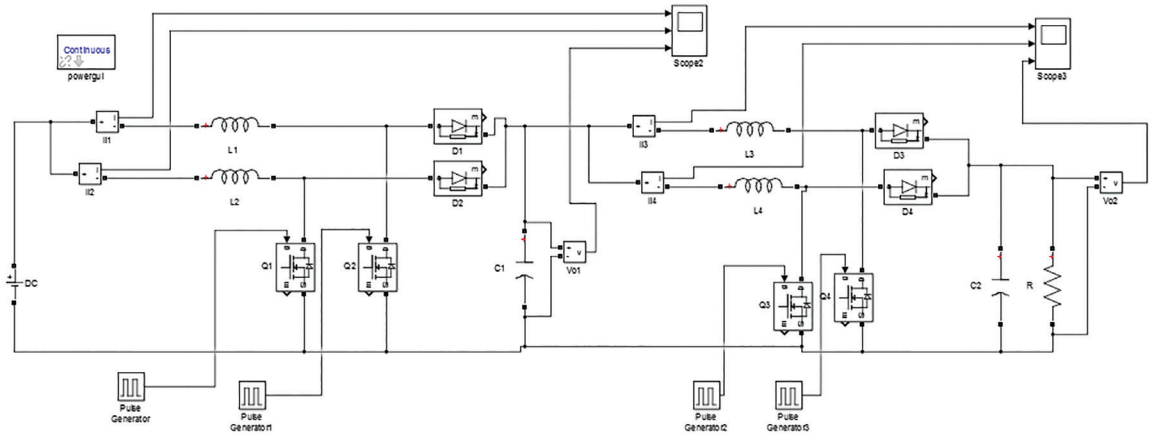

Fig. 8. Simulation circuit of proposed series-cascaded IBC

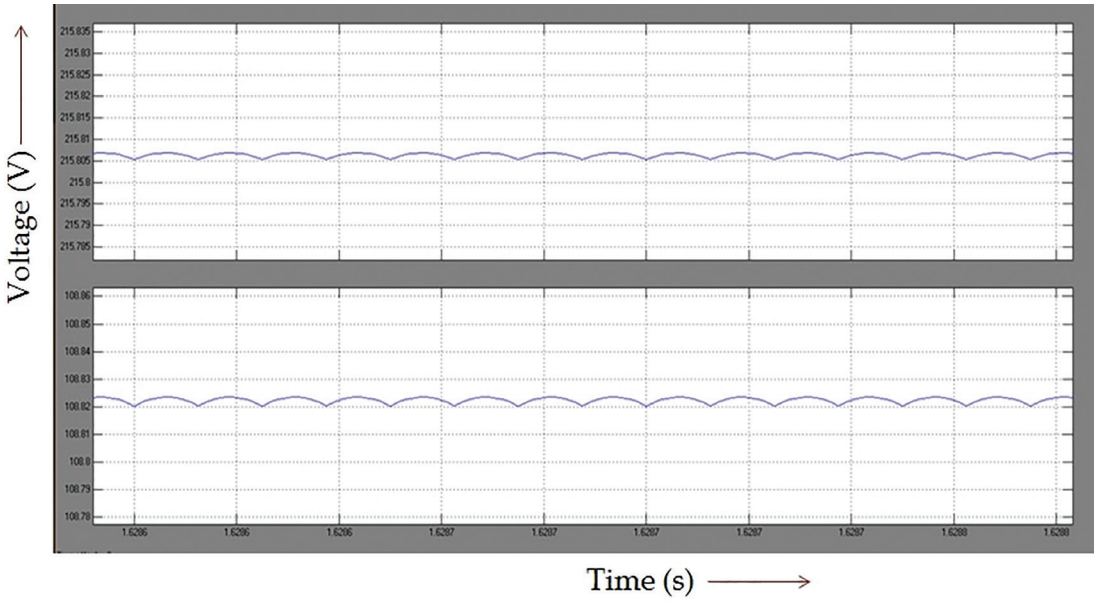

Fig. 9. Simulated output voltage of nearly 109 V and 216 V with mathematical model

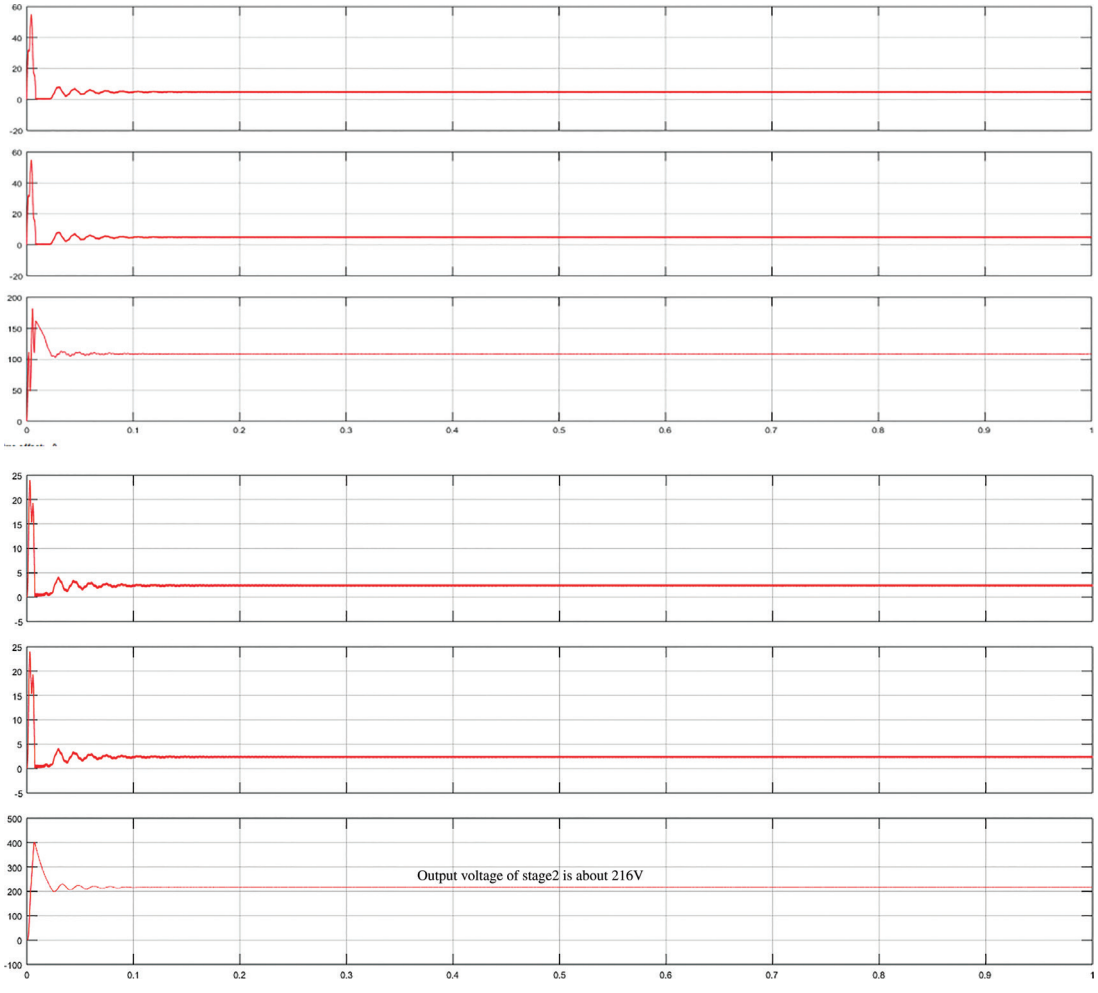

Fig. 10. Simulated output voltage of stage 1 about 109 V and stage 2 about 216 V with Simulink model

4. Hardware implementation

The laboratory prototype for the proposed two-stage cascaded IBC has been developed and tested. The laboratory setup for the hardware implementation is shown in Fig. 11. Table 2 represents the components selected for hardware development. Figure 12 shows the output voltage waveform of Stage 1, and Fig. 13 shows the output voltage waveform of Stage 2. Both the waveforms show the amplitude of around 112 V and 220 V, respectively. Figure 14 shows the hardware tested up to 180 W.

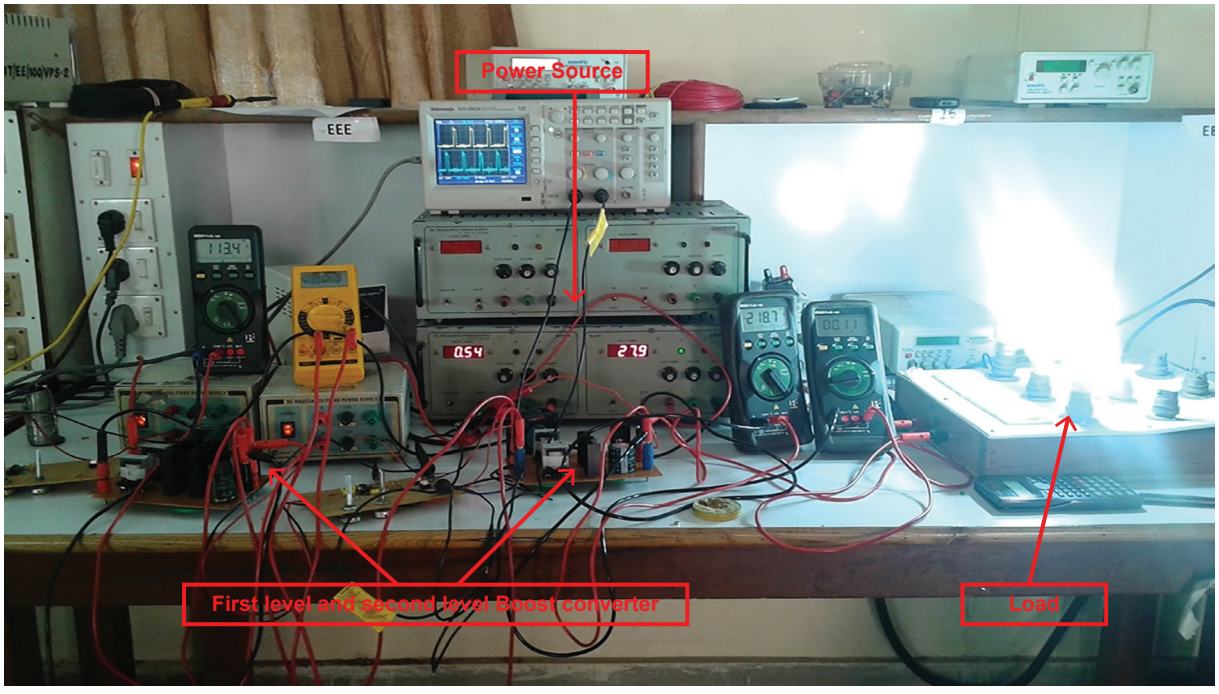

Fig. 11. Hardware implementation of proposed work

Table 2: Components chosen for hardware implementation

Component type	Component selected
Stage 1 Power MOSFET	IRF250N
Stage 2 Power MOSFET	IRFP450
Power diode	MOSPEC U16C20
Stage 1 inductor	1.5 mH, 6 A each
Stage 2 inductor	6 mH, 4 A each
Capacitor	220 μF, 400 V each
PWM IC for closed-loop control	SG3525
Driver IC	TLP 250

Table 3 gives the voltages of calculated, simulated and output obtained from the hardware.

5. Conclusion

A two-stage series-cascaded IBC has been proposed for the conversion of low-input DC output voltage to a high-input DC output voltage. The converter has been designed for a prototype output voltage of 220 V from the 55 V

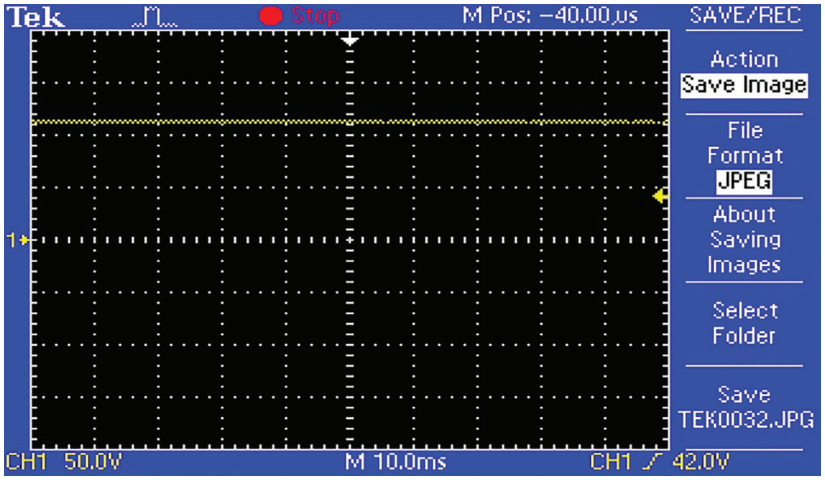

Fig. 12. Output voltage of Stage 1 obtained is about 110 V

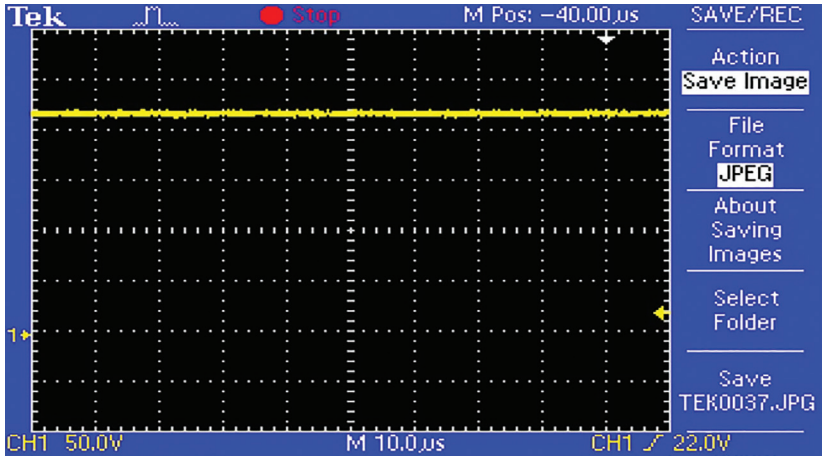

Fig. 13. Output voltage of Stage 2 obtained is about 220 V

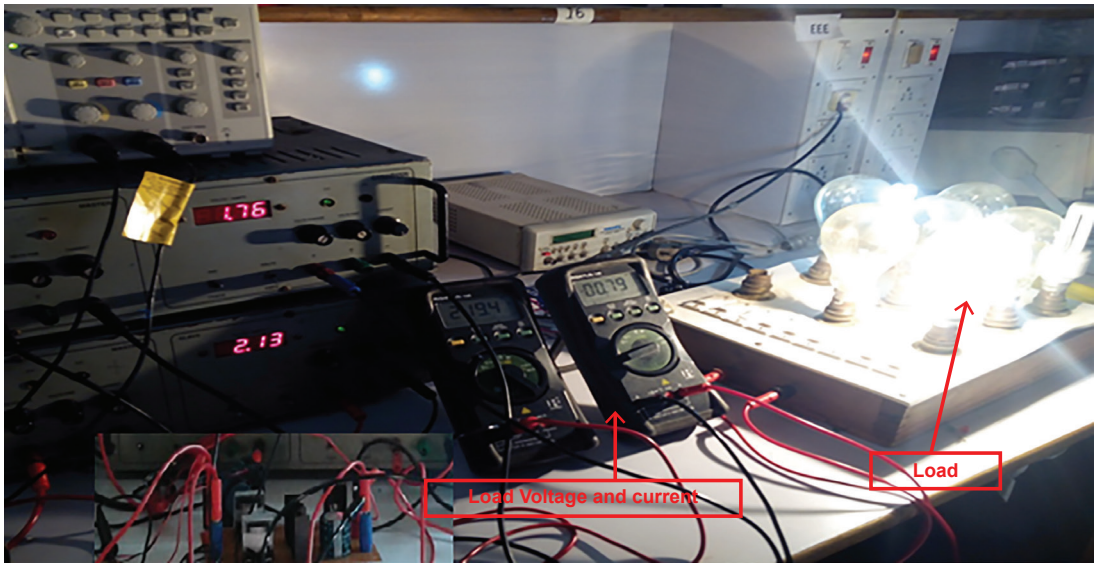

Fig. 14. Hardware prototype tested about 180 W

Table 3: Comparison between theoretical, simulated and practical values

Parameter	Theoretical value	Simulated value	Hardware result
Input voltage considered (V)	55	55	51
Stage 1 output voltage, V_{01} (V)	110	108.8	113
Stage 2 output voltage, V_{02} (V)	220	215.8	219

input. The topology is simulated on MATLAB/Simulink schematic environment. A novel mathematical model has been developed to verify the circuit design. A non-linear SFG has been developed for the converter, and consequently, Bode plot of the converter with open loop is obtained. It has been found that the converter is stable with positive gain margin and phase margin. The designed topology has been implemented on hardware in a laboratory environment, and upon testing, it has been verified that the results from hardware implementation agree with the simulation results, which in turn comply with the designed theoretical values.

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