Low-Delay Dispersion Comparator for Level Crossing Analog to Digital Converters

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***Abstract*—This paper presents a cost-effective technique for reducing the delay dispersion of the conventional comparator for level-crossing Analog-to-Digital Converters. Only three transistors, representing a variable driving-current block (VDCB), have been added to the conventional comparator circuit. The VDCB attempts to control the charging behavior of the difference amplifier' output node. The added block incurs small area overhead and low power consumption compared with the previous works. The proposed circuit has been implemented in MOSIS 130nm technology. The simulation results indicate that the overdrive-related propagation delay dispersion of the proposed technique is reduced to 23% of its counterpart in the conventional comparator. The active area of the proposed circuit is 140.2 µm2 and the power consumption is 227µW at 200MHz. For the sake of scalability check, the proposed circuit is also designed and simulated using 45nm technology. The simulation results came in the same direction, which implies the scalability of the proposed circuit.**

***Index Terms*—comparator, propagation delay dispersion, level-crossing ADCs.**

I. Introduction

ANALOG-TO-DIGITAL converters (ADCs) are important building blocks which are widely used in nearly all kinds of electronics, which enable the interfacing between the actual (analog) world and the digital processing environment. In modern life, electronic equipment is frequently used in different fields such as communication, transportation, entertainment, etc. Data converter circuits (ADCs/DACs) are very important components in electronic equipment. Since most real world signals are analog, these two converting interfaces are necessary to allow digital electronic equipment to process the analog signals. The requirements for low-power and small area ADC have been the driving forces of developing the level-crossing ADC (LC-ADC). The idea of a level-crossing analog-to-digital converter (ADC) has been presented in several articles [1]-[6]. In contrast with the conventional ADCs, where the input signal is regularly sampled with a given clock (constant time intervals), then the samples are quantized to approximate levels with digital numbers as shown in Fig. 1. The process introduces level quantization noise.

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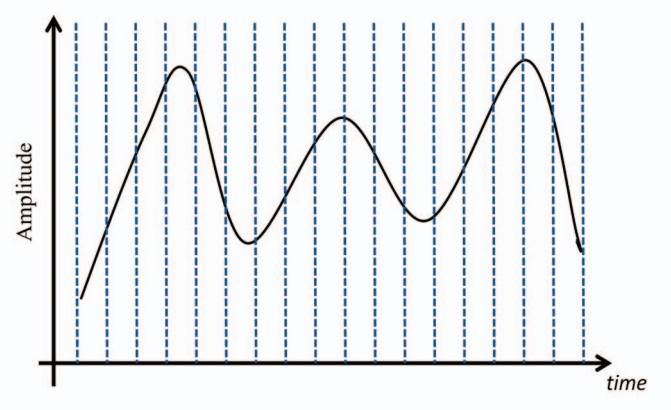

Fig. 1. Conventional ADC sampling of signal.

In contrast, in LC-ADC the sampling occurs at the moment when the input signal crosses a given threshold voltage level as shown in Fig. 2. The time between two successive crossings samples is measured with a precise time measurement unit. The conversion results of a LC-ADC are thus composed of "accurate" digital codes for the voltage magnitude, which is free from level quantization noise, and timing information representing the time intervals between crossing. The approach has some interesting properties such as absence of quantization error in the voltage domain (quantization noise), since the sample is taken exactly at the moment when the input signal crosses the sampling level. The second is the absence of aliasing due to absence of the main clock. In addition, the design is mostly digital, therefore, it occupies smaller area and consumes lower power compared with the conventional ADCs. MATLAB simulations show that using only 16 threshold levels (4 bits), it is possible to achieve signal to noise and distortion ratio (SNDR) that is equivalent to 9~10 effective bits of a conventional ADC [2].

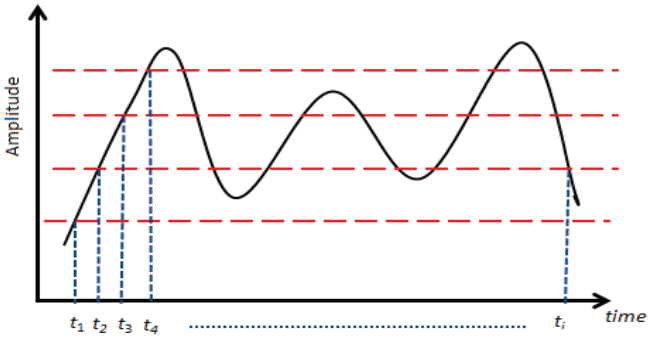

Fig. 2. Level-crossing sampling of signal.

LC-ADC features make it attractive for many applications. For examples, in signal processing field; it can be used for interfacing temperature, vibration and pressure sensors. Also, it useful for hand held devices since it consumes low power; it results in increasing the time between successive battery charges of the hand held device. Other important applications are in the field of ultrasound measurements and biomedical engineering.

In fig. 3 the conceptual block diagram of LC-ADC is shown. It has two main blocks: the comparator(s) and the Time-to-Digital Converter (TDC). The performance of both these blocks highly influences the overall timing performance of the LC-ADC. The comparator outputs are connected to asynchronous logic, which produces start and stop signals for the TDC each time the signal crosses a new threshold level. The TDC is used for measuring the time between two successive crossing events (start and stop signals).

With the existence of picoseconds resolution TDC [7]-[14] the comparator timing performance becomes a bottleneck of the design of high speed LC-ADCs.

In LC-ADC applications, comparator propagation delay dispersion is one of the important specifications. Where the delay is defined as the time required for the output to reach 50% point of a transition after the input signal (V_{CMP}) crosses the reference voltage (V_{REF}) ignoring the offset voltage.

Studying of the delay characteristics of the conventional comparator, it is noticed that the propagation delay varies with mainly three factors, namely, the slope of input signal, common-mode level, and the input overdrive - the difference between input reference and compared signal- (ΔV_{OVD}). This variation in propagation delay is called delay dispersion. The harmful effect of large delay dispersion is a non-recoverable signal distortion during the reconstruction process of the captured signal. Thus, the comparator delay dispersion can be seen as a limiting factor for the LC-ADC performance. In other words, it decreases the signal to noise (SNR) of the output of LC-ADC. Therefore, for high-speed LC-ADC a comparator with low delay dispersion is necessary. There are some trials to attack the comparator delay dispersion issue in literature.

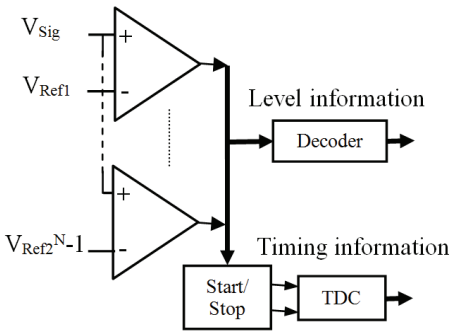

Fig. 3. Conceptual block diagram of level-crossing ADC.

In [15], a comparator circuit had been developed to decrease the delay dispersion. However, the resulted comparator delay dispersion could not be decreased below 87 PS for an input frequency range from 3 to 10 MHz. In addition, the relatively large area and high-power consumption of the comparator make it not so attractive for on-chip high-speed signal measurement applications. In [16], a conventional comparator is used, but due to the large delay dispersion of the conventional comparator, the input signal bandwidth is limited to 300 KHz. In [17], a feed forward techniques is used to compensate the delay dispersion of the conventional comparator. the techniques shows small dispersion compared with the previous designs, however, the area overhead might be limiting factor for on-chip applications. The authors in [18] have presented a low delay-dispersion comparator. The technique incurred small area overhead compared with the previous works but still the delay dispersion is relatively large and the power consumption as well.

In this paper, a low delay-dispersion, low-power, yet, cost-effective comparator is proposed. The conventional comparator is modified by adding a variable driving current block (VDCB). The modification an addition of only three transistors, which represents minimal area overhead while effectively reduces the delay dispersion.

The rest of the paper is organized as follows. Section II introduces the root causes of delay dispersion in the conventional comparator. Section III introduces the proposed technique. Sections IV, V and VI show the simulations results and comparison, effect of process variation then layout of the proposed comparator. The theoretical impact of the proposed technique on the performance of LC-ADC is presented in Sections VII followed by the conclusion.

II. Delay Dispersion in the Conventional Comparator

The propagation delay can be defined as the time required for a device to react to a change in the input signal and produce the corresponding output signal. In a comparator, it means that it is the time required to switch the output state from LOW to HIGH, or vice versa, when an input signal crosses a given reference level. The propagation delay in conventional comparator varies depending on many factors such as the input overdrive (the difference between the input reference and the compared signals), the common-mode level and input signal slew rate (signal derivative at the moment when it crosses the threshold level). The difference between highest and lowest value of the propagation delay is called propagation delay dispersion. Assuming that the comparator is operating in a stable temperature conditions, the propagation delay (τ_{pd}) can be given by:

$$\tau_{pd} = f(\Delta V_{OVD}, V_{CM}, S) \quad (1)$$

where ΔV_{OVD} is the input overdrive voltage, V_{CM} is the common mode level and S is the slope of the input signal. Fig. 4 shows the schematic diagram of the conventional comparator. In this paper, the effect of inputs voltage difference (ΔV_{OVD}) and the common mode levels are only considered in our study. The effect of input signal slope is not considered in this work. The conventional comparator of Fig. 4 is designed using 130 nm and 45 nm technology. The effect of the common mode level (V_{CM}) and the input overdrive (ΔV_{OVD}) on the delay variation is studied by SPICE

simulation. Fig. 5 and Fig. 6 shows the results. A according to the Fig., the results clearly indicate that the propagation delay (τ_{pd}) varies with both input overdrive and common mode level. However, the delay is affected by input overdrive more strongly than common mode level. The variation in propagation delay is called delay dispersion. These characteristics make the conventional comparator unsuitable and not attractive for level-crossing ADC working at high frequency. That is, the delay dispersion behavior of the conventional comparator introduces a non-recoverable timing error in the reported data timing information. Consequently, it decreases the SNR of level-crossing ADC or limits the highest frequency of the signal that can be processed by such ADC.

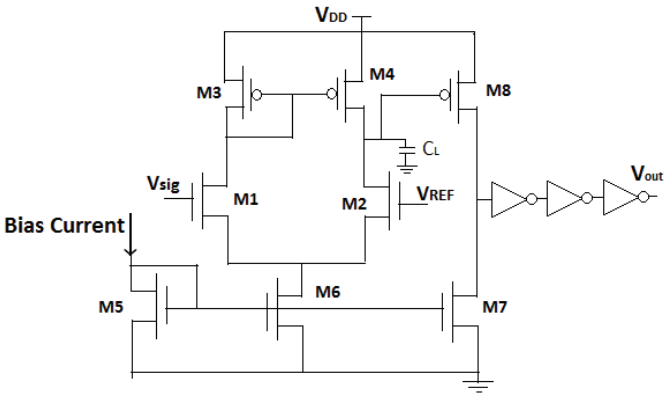

Fig. 4. Schematic diagram of the conventional comparator.

By studying the circuit of conventional comparator, the delay variation is caused mainly by the first stage difference amplifier represented by the transistors M1~M6. The overdrive-caused delay dispersion is mainly due to the variation of charging rate of the load capacitance (C_L) of transistor M4, which is represented by intrinsic drain capacitances M4 and M2 and the gate capacitance of M8. If ΔV_{OVD} is large, the charging current, which is supplied by M4, is also large. Therefore, the rise time of this node voltage is short and vice versa. The criterion is shown by the simulation in Fig. 5 and Fig. 6. The dependence of propagation can be represented by:

$$\tau_{pd} \alpha \frac{C_L \Delta V}{I_{L1}} \quad (2)$$

where ΔV is the voltage to be reached by the output of difference amplifier and C_L is the node equivalent capacitance and I_{L1} is the charging current which can be given by Equation 3

$$I_{L1} = I_{M4} - I_{M2} \quad (3)$$

The formula reveals that controlling the charging rate of C_L can result in better delay characteristics of the comparator.

III. Delay Dispersion Reduction Technique

Based on the formula given in (2), a technique to reduce the delay dispersion of the conventional comparator is proposed in this paper. The conceptual block diagram of the proposed technique is shown in Fig. 7. It is composed of a conventional comparator (represented by difference amplifier stage) followed by a variable driving-current block (VDCB). The role of the VDCB is to feed current component which is inversely proportional with the input overdrive voltage (ΔV_{OVD}). As a result, it keeps nearly constant charging current into C_L. The schematic diagram of the proposed circuit is shown in Fig. 8. The first stage of the conventional comparator (the difference amplifier) is modified by adding a variable driving current block (VDCB). The added block is composed of three transistors.

As it is explained in the Section II, the main reason of the overdrive-caused delay dispersion is that the load capacitance of the difference amplifier (C_L) is charged with a current proportional with the overdrive voltage ΔV_{OVD}. The target of added transistors M9~M11 (VDCB) is to keep the charging current as constant as possible regardless the value of ΔV_{OVD}. As shown in Fig. 8 the VDCB is controlled such that if ΔV_{OVD} is large, which means that the intrinsic charging current (I_{M4}) is also high, it supplies small additional charging current (I_{M11}). On the other hand if ΔV_{OVD} is small (I_{M4} is small) it supplies high I_{M11}. Since C_L is charged by the summation of I_{M4} and I_{M11}, the variation of charging rate of C_L will be

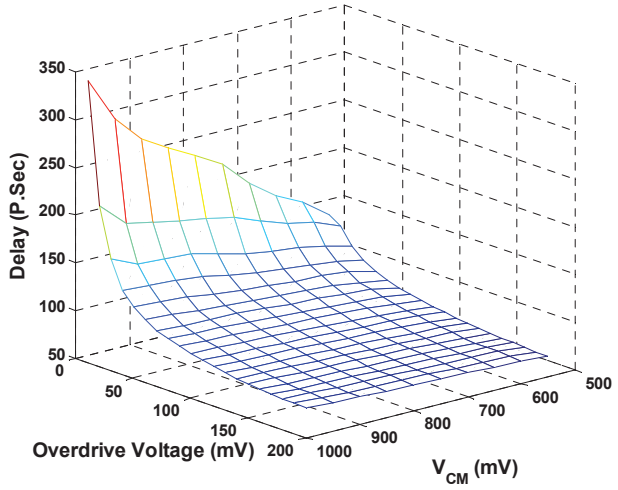

Fig. 5. Simulation results of delay variation of conventional comparator versus overdrive voltage (ΔV_{OVD}) and common mode level (V_{CM}) in 130nm technology.

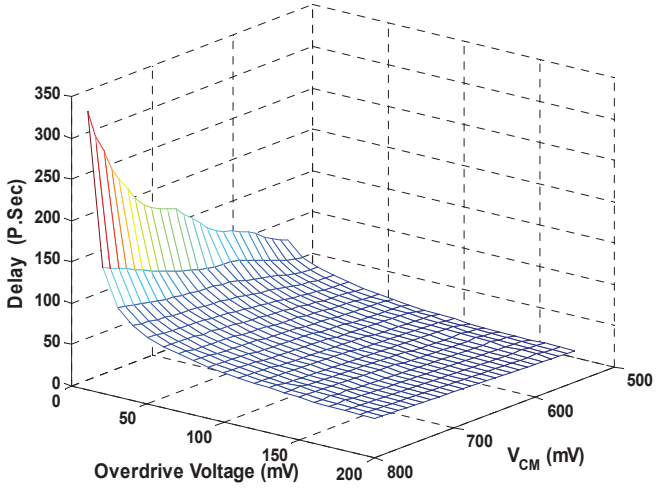

Fig. 6. Simulation results of delay variation of conventional comparator versus overdrive voltage (ΔV_{OVD}) and common mode level (V_{CM}) in 45nm technology .

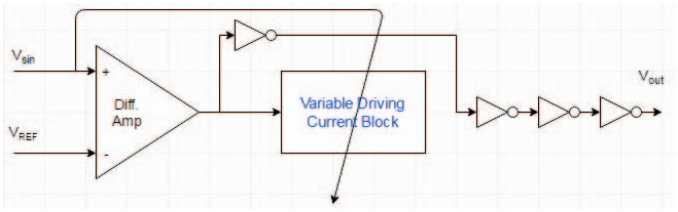

Fig. 7. Block diagram of the proposed technique.

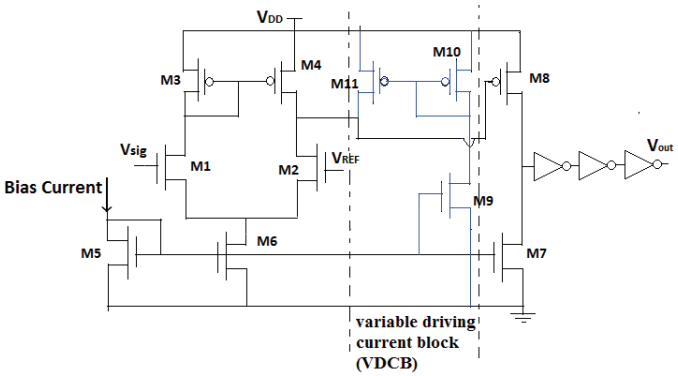

Fig. 8. Schematic diagram of the proposed technique.

smaller than the case of charging only with I_{M4}. Therefore, the overall delay dispersion will be also smaller than its counterpart of the conventional comparator. With the VDCB, the propagation delay time can be expressed in the formula (4).

$$\tau_{pd} \alpha \frac{C_L \Delta V}{I_{L2}} \quad (4)$$

where I_{L2} is given by Equation (5)

$$I_{L2} = I_{L1} + I_{M11} \quad (5)$$

The operation of the VDCB can be explained as follows; the width of M11 is selected such that when ΔV_{OVD} is zero, M11 works at the edge of saturation region. As ΔV_{OVD} increases, I_{L1} increases, however, the source to drain voltage of M11 (V_{SD11}) decreases moving M11 to triode region. Consequently M11 is unable to mirror all current of M10 which means that the current component supplied to C_L by M11 (I_{M11}) decreases. As a result, I_{L2} becomes almost constant because the increase in I_{L1} is compensated by decrease in I_{M11}. Since the propagation delay depends on I_{L2}, as indicated by Equation (4), delay dispersion of the whole circuit is decreased. In summary, VDCB is adjusted to compensate the variation of charging rate of C_L caused by the variable overdrive.

Another important benefit of the added circuit is that it helps reducing the delay dispersion caused by variation of the common mode level. It is noted from Fig. 5 and Fig. 6 that as the common mode level increases the delay also increases. This is due to the reduction of the intrinsic charging current. The additional charging current caused by VDCB is increased as the common mode levels increases and hence it partially compensates the reduction of the I_{M4}.

IV. Simulation Results and Comparison

The technique has been implemented in 130nm and, for the sake of checking the technique scalability; it is also simulated using 45nm technology. The preliminary layout of the proposed technique in MOSIS 130 nm technology is shown in Fig. 9. The optimized design shall be smaller.

The simulation results of the propagation delay variation versus the input overdrive (ΔV_{OVD}) with different common mode voltage are shown in Fig. 10 and Fig. 11 for 130nm and 45nm technologies respectively. The Figures indicate that the delay dispersions caused by the variable overdrive and common mode level are reduced compared with their counterparts of the conventional comparator. The effects of the overdrive voltage (ΔV_{OVD}) on the delay variation are plotted at two different values of common mode level V_{CM} as shown in Fig. 12 and Fig. 13 for 130nm and 45nm technology respectively. These figures indicate that the delay dispersions caused by the variable overdrive and common mode level are decreased compared with their counterparts of the conventional comparator for the two technologies. More specifically, in 130nm technology, over the given range of ΔV_{OVD}, and common mode voltage levels, the delay dispersion of the conventional comparator is 277PS. While in the proposed design it is decreased to 64 PS. which is only 23% of the delay dispersion of the conventional design. The proposed

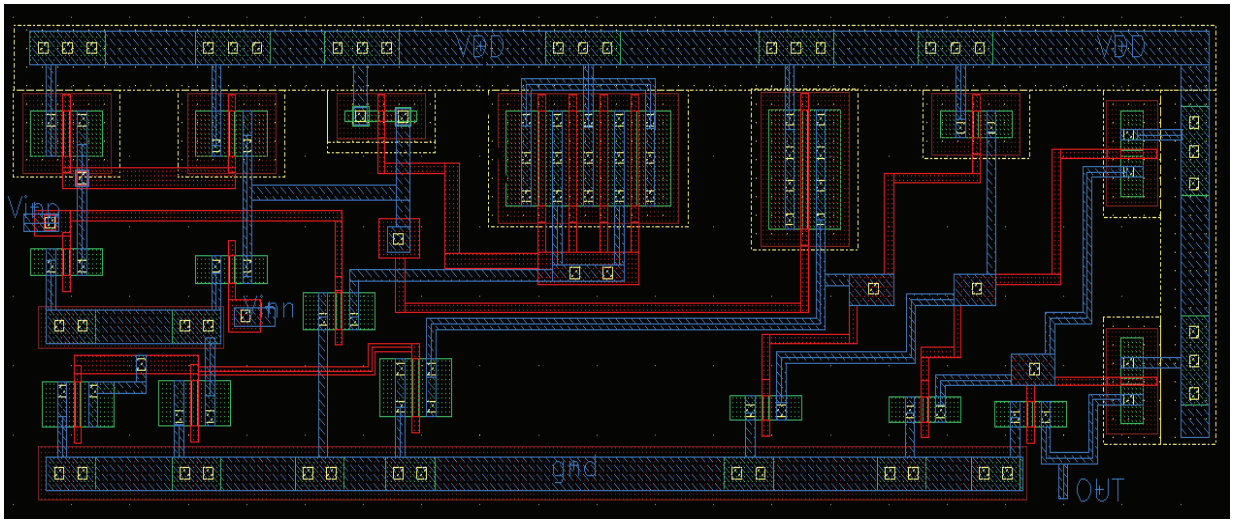

Fig. 9. Layout of the proposed technique.

technique is also designed and simulated in 45nm technology. The delay dispersion of the conventional comparator is 280PS. While in the proposed design it is decreased to 66 PS. which is only 23.5% of the delay dispersion of the conventional design. The results revel that the proposed design is scalable.

The proposed technique also reduces the delay dispersion caused by the common-mode level variations. The simulation results indicate that the delay dispersion due to common mode level variations of the proposed technique is reduced to about 24% and 25% of its counterpart of the conventional designs in 130nm and 45nm technologies respectively. The simulation results are shown in Fig. 14 and Fig. 15 for 130nm and 45nm technologies respectively. A comparison between the proposed and three previous works is shown in Table I.

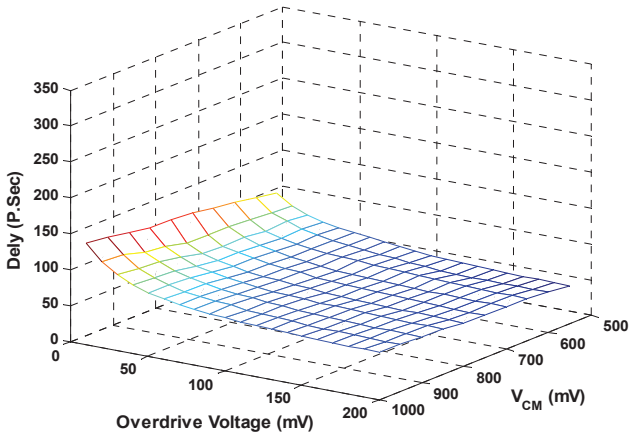

Fig. 10. Simulation results of delay variation of the proposed technique in 130nm technology.

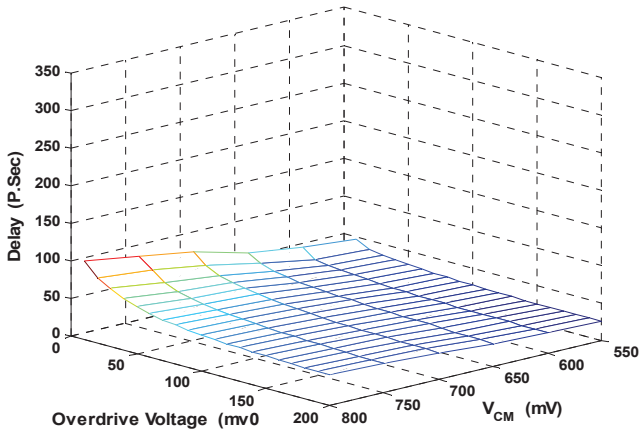

Fig. 11. Simulation results of delay variation of the proposed technique in 45nm technology.

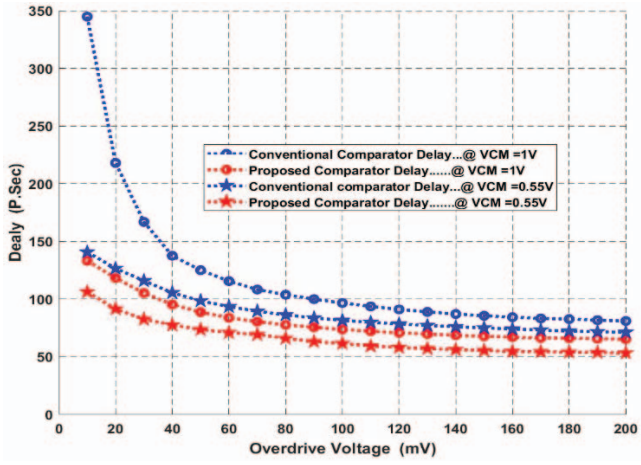

Fig. 12. Exemplar simulation results of delay variation of conventional comparator and the proposed comparator technique versus overdrive voltage (ΔV_{OVD}) @ V_{CM}=1V and 0.55V in 130nm technologies

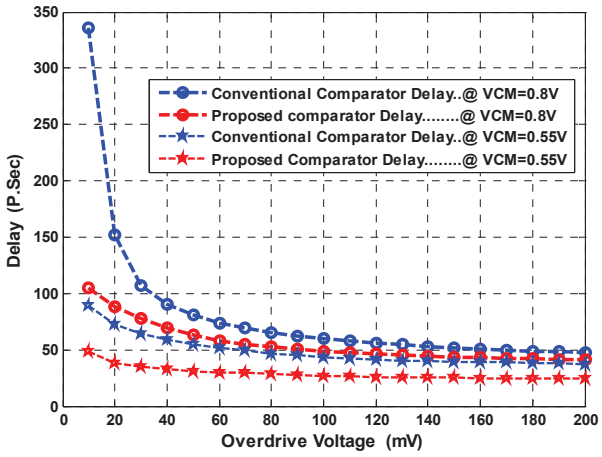

Fig. 13. Exemplar Simulation results of delay variation of conventional comparator and the proposed comparator technique versus overdrive voltage (ΔV_{OVD}) @ V_{CM}=0.8V and 0.55V in 45nm technology.

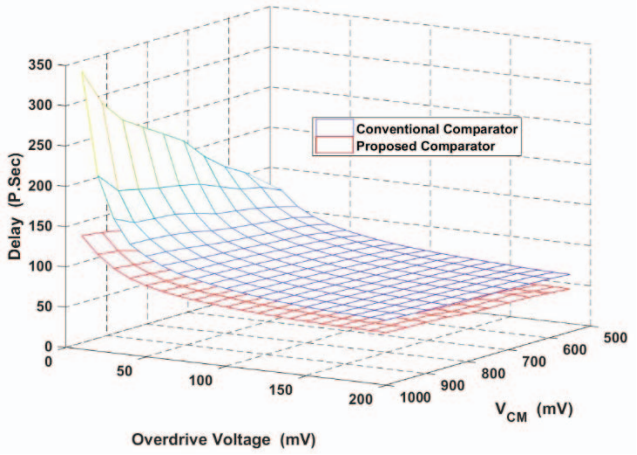

Fig. 14. Simulation results of delay variation of proposed technique & conventional comparator in 130nm technology.

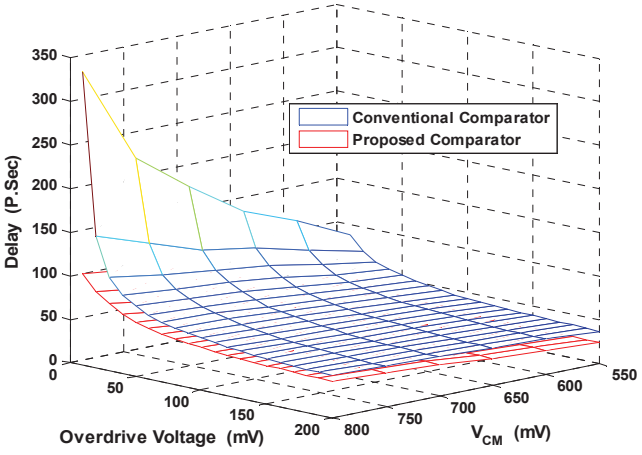

Fig. 15. Simulation results of delay variation of proposed technique & conventional comparator in 45nm technology.

TABLE I
COMPARISON WITH PREVIOUS WORKS

Parameter	This work (Simulation)		[15]	[17]	[18] (Simulation)	
Technology	45nm	130nm	0.35 µm	65 nm	45nm	130 nm
Power Consumption	195 µW @200 MHz	227 µW @200 MHz	9 mW @10 MHz	273 µW @ 200 MHz	220 µW @200 MHz	250 µW @200 MHz
Area overhead	~20%	~20%	>200%	~120%	~20%	~20%
Area	-------	140.2 µm2	37500 µm2	267.8 µm2	-------	140.2 µm2
Delay dispersion ΔTprop	66PS	64PS	87 PS	26 PS	75PS	75 PS
Delay Dispersion Percentage	23.5%	23%	33%	10%	26.7%	27%

V. EFFECT OF PROCESS VARIATIONS

The effect of process variations on the performance of the proposed tech is also studied. Monte Carlo simulations of the proposed technique are carried out assuming that the variation of 45nm technology is as given by [19]. Monte Carlo analysis is usually utilized to model random mismatch between different components due to process variation. For accurate statistical simulation, a certain model for each of these components in a particular processing technology should be formed by the manufacturing company. These models include the distribution of different important technological parameters of each component. These parameters are ΔV_{th} (threshold voltage variation), ΔW (width variation), ΔL (length variation). Since each of these variations is originated from many other independent stochastic variables., these parameters would ideally have a Gaussian distribution. Every Gaussian distribution is characterized by its mean value and the standard deviation (σ) from that mean. Design constraints would determine the mean value for a certain parameter, while σ is given by the manufacturer for a certain process technology. For modeling the impact of Vth variation in an MOS, a DC voltage source may be located in series with the gate terminal of the device which has a Gaussian distribution with zero mean value. The effect of process variations on the performance of the proposed tech is studied. Monte Carlo simulations of the proposed technique are carried out with 10% process variations. The results are plotted in Fig. 16 and Fig. 17. The results indicate that the average delay dispersion of the proposed technique is about 23% of its counterpart of the conventional design.

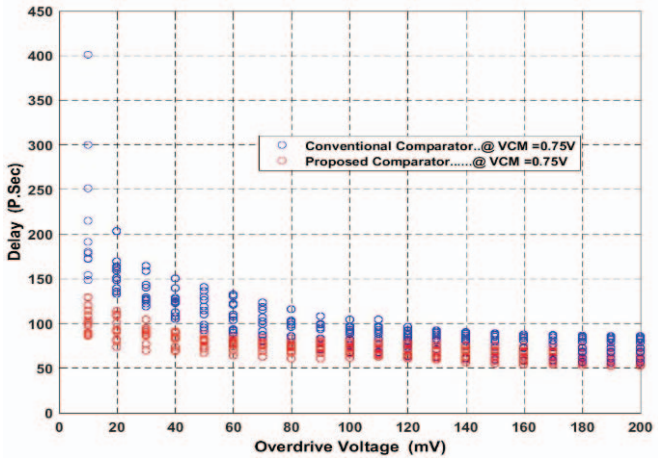

Fig. 16. Simulation results of the effect of 10% process variations on delay variation of Conv. comparator and proposed technique in 130nm technology.

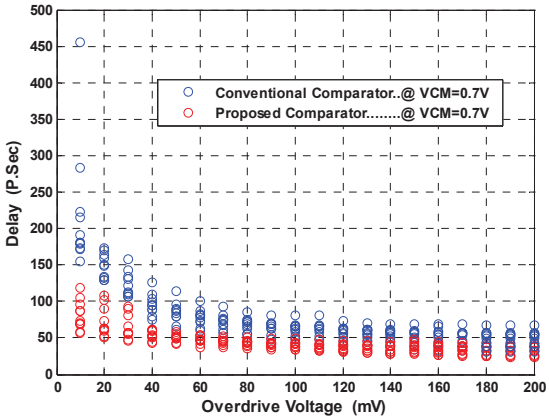

Fig. 17. Simulation results of the effect of 10% process variations on delay variation of Conv. comparator and proposed technique in 45nm technology.

VI. IMPACT OF THE PROPOSED TECHNIQUE ON THE PERFORMANCE OF LC-ADC

The main two components of LC-ADC are TDC and comparator. The signal-to-noise ratio (SNR) of LC-ADC' output is varied with timing accuracy of the system and the frequency of the input signal according to [7].

$$SNR = 20logR - 11.2 \text{ dB} \quad (6)$$

where R is the resolution ratio given by $R = 1/(f_{sig}\Delta T)$, f_{sig} is the frequency of the input signal ΔT is the timing resolution of the system. ΔT is determined by the worst one of two factors; the first is the delay dispersion of the comparator while the second is the resolution of the TDC-the minimum time that can be measured by the TDC. Since the timing resolution of TDC is around picoseconds [13]-[14], which is small compared with the delay dispersion of the conventional comparator, the bottleneck will be the timing uncertainty of the comparator. Therefore, ΔT in Equation (6) is determined by delay dispersion of the comparator.

According to the simulation results, using the conventional comparator, the timing resolution (ΔT_{Conv}) is 277 PS and 280 for 130nm and 45nm technologies designs respectively. On the other hand, using our design the timing resolution (ΔT_{prop}) is reduced to 64PS and 66 PS for 130nm and 45nm technologies.

Applying these values to Equation (6), using our design for 130nm and 45nm technologies would theoretically increases the SNR with 12.72dB and 12.55dB respectively higher than the case when using the conventional comparator for signals of the same frequency. Alternatively, keeping the same SNR, using the proposed comparator, the frequency of the signal

under test could be increased to 4.31X higher than its counterpart when using the conventional comparator. The comparison results are shown in Table II.

TABLE II
IMPROVEMENT OF SNR

Parameter	Conv. CMP 45nm	Conv. CMP 130nm	Prop. Tech. 45nm	Prop. Tech. 130nm
Delay Dispersion	280 PS	277 PS	**66 PS**	**64 PS**
Fixed Input Frequency	SNR_{Conv}	SNR_{Conv}	**SNR_{Conv} + 12.55 dB**	**SNR_{Conv} + 12.72 dB**
Fixed SNR	f_{sig}	f_{sig}	***4.3f_{sig}***	***4.31f_{sig}***

VII. CONCLUSION

This paper presents a technique for reducing the delay dispersion of the conventional comparator. The technique is implemented in MOSIS 130nm technology and, for the sake of scalability checking, it is designed and simulated in 45nm technology. The technique is useful for applications such as high-speed low-cost level-crossing ADCs and sampling head of automatic test equipment (ATEs). The technique occupies an active area of 140.2 μm^2 in 130 nm technology. The simulation results show that the overdrive caused delay dispersions in 130nm and 45nm technologies are effectively reduced to about 23% and 23.5% respectively of their counterparts of conventional comparator. The area overhead of the proposed technique is only three transistors, which is considerably small compared with the previous works. The power consumption of the proposed circuit in 130nm technology is 227µW @ 200MHz.

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