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New Design of a Boost Drive Circuit with an Energy Recovery Function for the Piezoelectric Jacquard Needle

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Abstract

Aiming at the technical bottlenecks existing in the current warp knitting machine control system such as jacquard drive circuit, the design method of self-boosting power supply circuit integrated with jacquard driver is proposed for the embedded warp knitting machine jacquard control system for miniaturization design. The voltage boost circuit designed can boost the low voltage from the input of the working power supply to the high voltage for the oscillation of the piezoelectric ceramic jacquard needles. Since the circuit adopts energy storage inductance instead of current-limiting resistor to optimize the driving circuit, it not only limits the forward charging current of the piezoelectric ceramic, but also effectively realize the energy recovery function. The effectiveness of the design method is verified by simulation.

Key words: warp knitting machine; self-boost power supply design; energy recovery.

dustry control.

patterns. It has become the latest frontier research hot spot in the field of textile in-

It is worth noting that the Piezoelectric

Jacquard Needle (PJN), the core mecha-

nism of jacquard warp knitting machines,

has encountered major technical bottle-

necks, for example: the complex system

structure, large volume, low integration,

the PJN drive circuit needing a dedicat-

ed high-voltage power supply, and the

large power consumption. Therefore, in

this study we offer a new design of the

boost drive circuit with an energy recov-

electronic jacquard quide bar

The piezoelectric jacquard warp knitting machine with the complex 3D jacquard function has become the development

direction of the new generation of high-

speed intelligent warp knitting machines. The key technology of the piezoelectric jacquard control system is to drive the

PJN quickly and independently accord-

ing to the requirements of the pattern design. The PJNs and cable, cover plate and positioning block form the Piezoelectric

Jacquard Needle Block (PJNB) (typically

E14, E16, E18, E24, L24 ((long shuttle)),

etc.). According to the model of the warp

knitting machine, different numbers of

PJNBs are combined into different types

of jacquard yarn combs. The warp knit-

ting machine piezoelectric jacquard control system independently controls every

PJN in jacquard yarn combs to shift or retain motion according to the pattern file

designed by CAD software, thereby re-

Design of embedded

ery function for PJN.

system, such as the electronic let-off device [1-4]; electronic traverse [5, 6], piezoelectric ceramic jacquard drive [7-9], intelligent detection (defective, broken yarn) [10, 11], and CAD system [12], as well as the 3D warp knitting machine [13-14] continue to improve and become more and more perfect. At present, for the jacquard warp knitting machine [6-9]. which comprises a compact structure, a fast response speed, good insulation and distributed direct drive technology of piezoelectric ceramics are a new force, breaking through the limits of the horizontal movement of combing machinery and achieving a three-dimensional, rich and complex jacquard effect of warp knitting fabric. The jacquard warp knitting machine is a revolutionary change to the traditional electronic transverse jacquard, which can only generate regular



Figure 1. Structure of EEJGB.

Introduction

Warp knitting is a weaving process of textiles. Warp knitted fabric has the characteristics of firm wear resistance, an exquisite three-dimensional flower shape, high strength bearing capacity, superior breathability and moisture permeability, low carbon environmental protection and non-toxicity, and is widely used in clothing, the military, medicine, aerospace, and other fields. With respect to the warp knitting machine as a weaving machine for producing warp knitted fabric, the core module of its distributed control

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alising the jacquard function of the warp knitting machine.

Our previous work [15] proposed an embedded electronic jacquard system which an integrated MCU, pattern data storage, jacquard driver circuit, booster circuit and communication interface into the head of a traditional PJNB to form an Embedded Electronic Jacquard Guide Bar (EEJGB), as shown in *Figure 1*.

In EEJGB, the MCU can receive pattern files from the engineer station via the communication interface and store them in internal flash memory. The EEJGB may communicate with the CAD software and jacquard controller through the OPC Software Bus to be compatible with traditional systems.

In [15], the integrated chip HV507 is used to drive the PJNB. Since the HV507 with 64 push-pull outputs can only form 16 typical bridge drive circuits, it cannot effectively reconstruct the booster circuit with additional circuits. A dedicated independent high-voltage power supply (GRB24200D-1W, 24V input, 200V output) is used to power the HV507. Literature [15] is a preliminary attempt at EEJGB whose main content focuses on the design of the circuit system structure and serial communication strategy. In view of the shortcomings of literature [15], this paper focuses on the design of the self-boosting circuit module in the PJN drive circuit, and gives control timing based on the state machine. The self-boosting circuit module proposed is integrated with the driving circuit and has a simple structure. In addition, inductance is adopted to replace the current limiting resistance of the traditional driving circuit, which can not only limit the forward charging current of piezoelectric ceramics but also has an energy recovery function.

Usually, the EEJGB drives a PJNB consisting of 16 PJN, the drive circuit of which is shown in *Figure 2*. A guide needle with piezoelectric ceramic attached to its two sides and a glass fibre layer acting as an insulating barrier together form a PJN for warp knitting. The PJN utilises the inverse piezoelectric effect of the piezoelectric ceramic plates to achieve an offset effect. We first assume that the high-voltage operating power supply Vp is a constant voltage power supply, and its self-boosting process will be specifically described in the later self-boost power



Figure 2. Drive circuit of EEJGB.



Figure 3. Drive circuit with integrated self-boosting function.

supply design section. In the course of this work, every PJN is controlled by an independent dual-arm bridge. under the alternating control of $\overline{V_{3n}}$ and V_{5n} & $\overline{V_{4n}}$ and V_{6n} inputs of the Metal-Oxide-Semiconductor Field-Effect Transistor(MOS-FET) on the double-armed bridge; working voltage V_p is added alternately on both sides of the PJN so as to make it produce left or right deviation. Because of the capacitive effect of the piezoceramic, the PJN can remain in its offset position. The jacquard warp knitting machine is designed to make the PJNs shift left and right or remain motionless to form the desired pattern, which is derived from the cumulative offset of adjacent needles.

Design of drive circuit with integrated self-boosting function

Since the working voltage to drive the PJN is generally high at about 200 V, the conventional driving circuit is powered by an independent 200 V power supply, which requires not only additional cable

laying but also increased cost. In this paper, the drive circuit was completely redesigned and the self-boosting function integrated without changing the basic structure of the circuit. Since the driving principle of the 16 PJNs is the same, in order to simplify the description, the self-boosting working principle of the driving circuit is illustrated by taking the No. 1 Jacquard needle as an example, as shown in *Figure 3*.

The circuit model that drives a jacquard needle consists of six MOSFETs with \overline{V}_1 , \overline{V}_2 , \overline{V}_{31} , \overline{V}_{41} , V_{51} and V_{61} as inputs, 13 diodes $(D_1 \sim D_9, D_{i1}((i = 3, 4, 5, 6)))$ an energy storage inductor L, and 0 a PJN_1 . V_{DD} is the forward voltage of the diode D_7 , V_d the low-voltage power supply (usually the 24 V power supply commonly used in industry), and V_n is a high-voltage working power supply with zero initial energy storage, which can be viewed as a large capacitor. For convenience of presentation, the MOS-FET is turned on $(T_i = 1)$ when the input is high, and then turned off $(T_i = 0)$ when the input is low.



Figure 4. State transition diagram of the control logic of the drive circuit.



Figure 5. Simulation circuit diagram realised by Stateflow.

Control logic timing design of a PJN₁ drive circuit with an integrated self-boosting function

To facilitate the analysis, we first define the finite state machine of the control logic of the drive circuit as

$$FSM = \{S, A, C\}$$
(1)

Where, $S = \{S_1, ..., S_n\}$ is a set of *n* states; $A = \{A_1, ..., A_n\}$ a set of switching actions of MOSFETs in the state; and $C = \{C_1, ..., C_n\}$ is a set of transition conditions. The relationship of the above set is

$$S_i = \{A_i, P_i, C_i\}, i = 1, ..., n$$
 (2)

In order to facilitate the analysis and description of the state transition process, the following directed graph G is defined based on graph theory and *Equation (1)*

$$G = \{S, E\} \tag{3}$$

Where we abstract the drive circuit control logic state set S defined in *Equation (1)* as the vertex of the graph and abstract state transition condition set C as the edge weight set, then the edge set is defined as

$$E = \{E_1, ..., E_m\} = \{(S_i, S_j) | c_{ij} \in C_i\} \quad (4)$$

Where, $C_i \in C$ represents the set of conditions for the transition from the i-th state (vertex of the graph) to other states, c_{ij} the transition condition from state S_i to S_j , abstracted as the weight of the edge (S_i, S_j) ; $c_{ij} = 0$ indicates that the condition is not true, $c_{ij} = 1$ that the condition is true, and $c_{ij} = -1$ that there is no such side. A state transition diagram describing the control logic of the drive circuit is shown in *Figure 4*. The state functions, actions in states, and transition conditions between states are described in *Table 1*.

Initial boost state S₀

Before the driving circuit works, firstly the six MOSFETs are turned off by controlling the pulse signal, and the low-voltage power supply V_d is charged to high-voltage working power V_p through diode D_7 until $V_p \ge V_d - V_{DD}$. Where V_{DD} is the forward voltage of diode D_7 .

Charge boost state S₁

In this process, V_d continues to charge and boost V_p through the booster circuit until V_p reaches the rated high voltage V_p^* required for operation. V_p is detected in real time during the boosting process, and if $V_p \ge -V_p^*$, the charging boosting process ends. During the boosting process, the upper limit of the voltage applied to PJN_1 is V_{PJN}^U . When condition $V_p \ge V_p^*$ is satisfied, if x = 0, S_1 transitions to the left offset state S_2 ; otherwise if x = 1, it transitions to the right offset state S_4 .

PJN₁ left offset state S₂

Assuming that the rated drive voltage that meets the process requirements is V_{PJN}^* , then according to the state machine operation process shown in *Figure 4*, the 6 MOSFETs are turned on and off in an orderly manner through control pulses, and the high-voltage working power supply is controlled to positively charge PJN₁ (inverse piezoelectric effect), up to $V_{PJN} \ge V_{PJN}^*$, and maintain the left offset movement state for α ms according to the process requirements. The charging process needs to guarantee $i_L \le I_{UL}$.

PJN₁ energy recovery state S₃

In state S_3 , PJN₁ returns to the equilibrium position from the left offset position and recovers the energy stored in the piezoelectric ceramic to the high-voltage power supply V_p . When V_{PJN} is detected as zero, the state of the high-voltage power supply V_p is judged: if $V_p < V_p^*$, S_3 transfers to S_1 (the high-voltage working power supply V_p is charged and boosted at S_1 to supplement the loss caused by driving the PJN left-biased operation); otherwise if $V_p \ge V_p^*$, S_3 is transferred to S_4 .

PJN_1 right offset state S_4

Similar to state S_2 , the rated drive voltage of PJN₁ is V_{PJN}^* . According to the state machine operation process shown in *Figure 4*, the 6 MOSFETs are turned on and off in an orderly manner through control pulses, and the high-voltage working power supply V_p is charged in reverse (inverse piezoelectric effect) until $V_{PJN} \leq -V_{PJN}^*$, and the right offset movement state β ms is maintained according to the process requirements. The charging process needs to guarantee $I_L \leq I_{UL}$.

PJN_1 energy recovery state S_5

Similar to state S_3 , PJN₁ returns to the equilibrium position from the right offset position and transfers the energy stored in the piezoelectric ceramic to the high-voltage power supply V_p . When V_{PJN} is detected as zero, the state of the high-voltage power supply V_p is judged: if $V_p < V_p^*$, S_5 transfers to S_1 (high-voltage working power supply V_p is charged and boosted at S_1 to supplement the loss caused by driving the PJN right-biased operation); otherwise if $V_p \ge V_p^*$, S_5 is transferred to S_2 .

Simulation analysis

MATLAB software was used to verify the simulation. The drive circuit with an integrated self-boosting function built by MATLAB/simulink is shown in *Figure 5*. The drive circuit timing control model, built using MATLAB/Stateflow simulation design, is shown in *Figure 6*.

Assume that V_d is 24V, $C_p - 3$ uF, C_{PJN} - 30 nF, L - 300 mH, $V_{PJN} - 200$ V, V_P - 230 V, $I_{UL} - 10$ mA $V_{PJN} - 0.1$ V, and the forward voltage V_{DD} and resistance of the diode $D_1 : D_9$ are 0.7 V and 0.05 Ù. The FET resistance Ron and snubber capacitance of the MOSFET are 0.1 Ù and 1×10^{10} F. Both α and β are 4 ms.

Table 1.	Information	table of state	transition	diagram
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Function	State	Substate	Action	Transfer condition	
Initial	S ₀	/	$\begin{split} A_0 &= \{ T_1 = 0, T_2 = 0, T_3 = 0, \\ T_4 &= 0, T_5 = 0, T_6 = 0 \} \end{split}$	$c_{0,1} = \{V_p \ge V_d - V_{DD}\}$	
Charge boost for V _p	S ₁	S ₁₁	$\begin{split} A_{11} &= \{ T_1 = 1, T_2 = 0, T_3 = 1, \\ T_4 = 0, T_5 = 1, T_6 = 0, \\ y &= 1 \} \end{split}$	$\begin{split} c_{11,12} &= \{V_{PJN} \geq V_{PJN}^U\} \\ c_{11,13} &= \{I_L \geq I_{UL}\} \end{split}$	
		S ₁₂	$\begin{split} A_{12} &= \{ T_1 = 1, T_2 = 0, T_3 = 0, \\ T_4 = 1, T_5 = 0, T_6 = 1, \\ y &= 0 \} \end{split}$	$\begin{split} c_{12,11} &= \{V_{PJN} \leq -V_{PJN}^U\} \\ c_{12,13} &= \{I_L \geq I_{UL}\} \end{split}$	
		S ₁₃	$\begin{aligned} \mathcal{A}_{13} &= \{ T_1 = 1, T_2 = 0, T_3 = 0, \\ T_4 = 0, T_5 = 0, T_6 = 0, \} \end{aligned}$	$c_{13,11} = \{(I_L == 0) \land (y=1)\}$ $c_{13,12} = \{(I_L == 0) \land (y=0)\}$	
		/	/	$c_{1,2} = \{ (V_p \ge V_p^*) \land (x == 0) \}$ $c_{1,5} = \{ (V_p \ge V_p^*) \land (x == 1) \}$	
<i>PJN</i> ₁ left offset	S ₂	S ₂₁	$\begin{aligned} A_{21} &= \{ T_1 = 0, T_2 = 0, T_3 = 0, \\ T_4 &= 0, T_5 = 0, T_6 = 0, \} \end{aligned}$	$\begin{split} c_{21,22} &= \{I_L == 0\} \\ c_{21,23} &= \{V_{PJN} \geq V_{PJN}^*\} \end{split}$	
		S ₂₂	$\begin{aligned} A_{22} &= \{ T_1 = 0, T_2 = 1, T_3 = 1, \\ T_4 &= 0, T_5 = 1, T_6 = 0, \} \end{aligned}$	$\begin{split} c_{22,21} &= \{I_L \geq I_{UL}\} \\ c_{22,23} &= \{V_{PJN} \geq V_{PJN}^*\} \end{split}$	
		S ₂₃	$A_{23} = \{T_1 = 0, T_2 = 0, T_3 = 0, T_4 = 0, T_5 = 0, T_6 = 0, \}$	1	
		1	/	$c_{2,3} = \{after(\alpha, msec)\}$	
Return to equilibrium position (energy recovery)	S ₃	S ₃₁	$\begin{aligned} A_{31} &= \{ T_1 = 0, T_2 = 1, T_3 = 0, \\ T_4 = 1, T_5 = 0, T_6 = 1, \\ x = 1 \} \end{aligned}$	$c_{31,32} = \{I_L \ge I_{UL}\}$	
		S ₃₂	$A_{32} = \{T_1 = 0, T_2 = 0, T_3 = 0, T_4 = 0, T_5 = 0, T_6 = 0, x = 1\}$	$c_{32,31} = \{I_L == 0\}$	
		/	/	$c_{3,1} = \{ (V_{PJN} == 0) \land (V_P < V_P^*) \}$ $c_{3,4} = \{ (V_{PJN} == 0) \land (V_P \ge V_P^*) \}$	
<i>PJN</i> ₁ right offset	S4	S ₄₁	$\begin{aligned} A_{41} &= \{ T_1 = 0, T_2 = 0, T_3 = 0, \\ T_4 &= 0, T_5 = 0, T_6 = 0 \} \end{aligned}$	$\begin{split} c_{41,42} &= \{I_L == 0\} \\ c_{41,43} &= \{V_{PJN} \geq V_{PJN}^*\} \end{split}$	
		S ₄₂	$\begin{split} A_{42} &= \{ T_1 = 0, T_2 = 1, T_3 = 0, \\ T_4 = 1, T_5 = 0, T_6 = 1 \} \end{split}$	$\begin{split} c_{42,41} &= \{I_L \geq I_{UL}\} \\ c_{42,43} &= \{V_{PJN} \geq V_{PJN}^*\} \end{split}$	
		S ₄₃	$\begin{split} A_{43} &= \{ T_1 = 0, T_2 = 0, T_3 = 0, \\ T_4 = 0, T_5 = 0, T_6 = 0 \} \end{split}$	/	
		1	/	$c_{4,5} = \{after(\beta, msec)\}$	
Return to equilibrium position (energy recovery)	S ₅	S ₅₁	$A_{51} = \{T_1 = 0, T_2 = 1, T_3 = 1, T_4 = 0, T_5 = 1, T_6 = 0, x = 0\}$	$c_{51,52} = \{I_L \ge I_{UL}\}$	
		S ₅₂	$A_{52} = \{T_1 = 0, T_2 = 0, T_3 = 0, T_4 = 0, T_5 = 0, T_6 = 0, x = 1\}$	$c_{52,51} = \{I_L == 0\}$	
		/	/	$c_{5,1} = \{(V_{PJN}=0) \land (V_p < V_p^*)\}$ $c_{5,2} = \{(V_{PJN}=0) \land (V_p \ge V_p^*)\}$	



Figure 6. Finite state machine model.



Figure 7. Boosting process of high voltage working power.



Figure 8. PJN working process: a) waveform of V_{p} , b) waveform of voltage V_{PZF} , c) waveform of voltage I_L .

In the simulation process, first, after V_p is boosted to 23.3 V through the initial boosting state S_0 , the boosting state S_1 is entered, as shown in *Figure 7*. As can be seen from *Figure 7*, V_p reaches 230 V in 30 ms. PJN working process is shown in *Figure 8*.

Figure 8.a shows the swing cycle of PJN, which goes through the following five states: $S_2 \rightarrow S_3 \rightarrow S_1 \rightarrow S_4 \rightarrow S_5$, and Figure 8.b shows the voltage waveform of V_{PZT}. As can be seen from Figure 8.c, in the swing period of PJN, in addition to the stage where V_{PZT} is maintained at 200V in states S_2 and S_4 , the average current of I_L is 5 mA, and the duration is about 10ms. It can be seen from Figure 8 that the use of inductance instead of the current limiting resistor in the traditional circuit greatly reduces the loss of the circuit, and has the function of energy recovery through states S_3 and S_5 . Considering that the traditional drive circuit uses a 10 K current limiting resistor, the power loss is 0.25 W.

Conclusions

In this paper, we propose a new design of boost drive circuit with an energy recovery function for the PJN. The design of the new PJN driving circuit adopts energy storage inductance instead of the resistance in the traditional circuit working with piezoelectric ceramics, so that the circuit has the function of self-boosting, with no need for an external high-voltage working power supply, with only the necessity of a low-voltage power supply instead, effectively reducing the complexity of the circuit. In addition, the integrated design of the self-booster and energy recovery function improves the integration degree of the circuit, which provides a theoretical basis for the design of an embedded miniaturisation control system for the jacquard warp knitting machine.

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