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Intravenous glucose tolerance test hardware implementation

D. KULAKOVSKIS*, T. SLEDEVIČ, A. GEDMINAS, AND D. NAVAKAUSKAS

Department of Electronic Systems, Vilnius Gediminas Technical University, Naugarduko 41, 03227 Vilnius, Lithuania

Abstract. Blood glucose level monitoring and control is of utmost importance to millions of people who have been diagnosed with diabetes or similar illnesses. One of the conventional tests for measuring how the human body breaks down glucose is IVGTT, the Intravenous Glucose Tolerance Test. The difficulty of computing the models of glucose-insulin interaction presents an issue when attempting to implement them in embedded hardware. The Metabolic P (MP), contrary to other models, does not require solving differential equations to compute, thus it could be an effective modelling approach for real-time applications. The present paper proves that MP system methodology-based IVGTT implementation in the Field Programmable Gate Arrays (FPGA) technology is reasonably precise and sufficiently flexible to be used effectively in multi-user scenarios. Presentation of the state-of-the-art focuses on glucose-insulin interaction models, glucose monitoring systems and MP system implementation techniques. Methods for MP system computations and techniques for their implementation on FPGA, together with the original unified MP system implementation technique, have been presented in this paper. The results of an elaborate investigation into the IVGTT MP systems, as well as their single and unified MP implementation techniques have also been considered. It is shown that the techniques developed are applicable to all known IVGTT MP systems, and can achieve RMSE not higher than 15% using a word length of at least 32 bits. The novel MP system combined quality metrics and its pictorial representation allow the analysis of various implementation characteristics. Compared to the unified pipelined IVGTT MP system implementation technique, the developed unified combinational technique ensures a 2–3 times higher speed.

Key words: gate arrays, metabolic P system, implementation quality, glucose–insulin interactions.

1. Introduction

Electronic devices present new diagnostic and treatment possibilities in medicine [1]. The artificial pancreas device system is becoming more popular in the treatment of diabetes. Electronic medical devices that use glucose sensors are regarded as an effective method for monitoring and administering insulin, however, they can be further improved [2].

Diabetes refers to a medical condition which causes a high blood sugar, or blood glucose, level. The problem is experienced when human body fails to produce insulin or makes an insufficient amount, or fails to make good use of insulin [3]. There are two major types of diabetes: Type 1–2. In the case of Type 1 diabetes, the body fails to make insulin. Type 2, on the other hand, is when the body fails to produce or make good use of insulin well. Diabetes can be a cause of adverse health problems and can be hard to diagnose.

According to the report of the World Health Organization, in the United States 29 million people or 9.3% of the population have diabetes. Of the 29 million, only 21 million people have been diagnosed with said disease. This means a staggering 8 million people, representing more than 1/4 of the total number of the people with diabetes, have not yet been diagnosed. Globally, on the other hand, a total of 422 million people were living with diabetes in the year 2014. This is a reason to worry now that the figure had risen from 108 million in 1980, implying that the number of diabetic patients was dramatically increasing. Also, it is important to note that, among the patients aged 18 and above, the spread of diabetes had risen from 4.7% in 2008 to 8.6% in 2014 [4].

To avoid diabetes complications, there is a need for the individual to control the level of their blood glucose well. The only pathway that controls the blood glucose level is by keeping a check on the blood glucose level, whether in a hospital environment or at home [5]. It is only when knowing the level that one can know how to do this [6].

There are tools with which one can tell how the human body breaks down glucose. This process is referred to as the glucose tolerance test. The intravenous glucose tolerance test (IVGTT) is among the most common glucose tolerance tests. In this test, the vein is injected with glucose for a 3-minute period. Levels of insulin in the blood are taken just before injection then again at the first and third minutes after injection. These tests are performed with the aim of diagnosing diabetes. A high glucose level in the blood is an indication of diabetes [7].

In this article, an IVGTT based on the Metabolic P (MP) system [7] has been investigated. MP systems, contrary to P systems, use a single membrane in their computations; nevertheless, many biological processes have been successfully modelled by MP systems in software.

The first attempt to analyze MP system hardware implementation techniques was presented in [8]. Moreover, an original Very High Speed Integrated Circuit Hardware Description Language (VHDL) code generation tool that can be used to automate single MP system implementation in hardware, such as

*e-mail: darius.kulakovskis@vgtu.lt

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Field Programmable Gate Arrays (FPGA), was recently developed by the authors of [9]. It was discovered that the tool had worked adequately for a single system; however, the final decision is not trivial because sometimes several architecture alternatives have to be considered manually. Thus, the problem of finding the best implementation technique for multiple (different) MP systems remains unsolved.

This paper aims at studying the accuracy and flexibility of MP system methodology-based IVGTT implementation in the FPGA technology to be used effectively in multi-user scenarios.

The purpose of the investigation is to establish the quality characteristics of a system that is capable of processing many input signals of different subjects. The typical use case would be an edge computing system in a hospital environment [10] with sufficient throughput to service multiple patients simultaneously.

There exist a number of possible solutions to perform this task. The selected FPGA implementation is not claimed to be the most suitable for all cases, although it avoids certain disadvantages of other possible solutions. For example, alternative cloud solutions are possible [11], but they can suffer from reliability, security and privacy issues [12]. A locally based cloud would require expensive server infrastructure in the hospital, which may not be feasible in smaller or remote hospitals.

Another possible solution is implementation in a simple microcontroller-based device. It could perform the calculations required, but suffers from a lack of scalability when compared to FPGA with its intrinsic parallelism and is better suited for personal portable device use, as seen in other implementation cases [13].

The rest of the paper has been organized in four sections. The presented discussion of the state-of-the-art focuses on glucose-insulin interaction models, glucose monitoring systems and MP system implementation. Then methods for MP system computations and techniques for their implementation on FPGA, together with the original unified MP system implementation technique and its assessment procedure have also been presented in the paper. The results from an elaborate investigation of all six known IVGTT MP systems, their single and unified MP implementation, and the overall implementation quality have been considered in the last section.

2. Related work

The attempts at developing an artificial pancreas system have been made for about half of the century, but a reliable or clinically acceptable glucose regulator is so far unavailable [14]. However, a number of glucose-insulin interaction models have been developed. Some of them have also been implemented, or attempts have been made to implement them, in real-time hardware-based monitoring and control systems.

2.1. Glucose–insulin interaction models. Glucose-insulin interactions have been studied for a long time and a number of different models that predict these interactions are available. Generally, these models can be split into two categories [15]: physiological models that try to describe system dynamics using differential equations, and "black-box" models that use system identification techniques.

One of the oldest and most widely used is the Minimal model [16, 17]. The model consists of three differential equations predicting how glucose and insulin concentrations change over time. Other physiological glucose-insulin interaction models are an ordinary differential equation (ODE) model proposed in [18] and simplified in [19], a single explicit delay differential equation (DDE) model with [20] or without [21] insulin compartment split, and a two-delay DDE model [22].

The above-mentioned models use complex mathematical constructs like ODEs that are hard to implement effectively in hardware [15] or suffer from a lack of the accuracy needed for precise medical applications [23]. The proposed method using the MP system can be an alternative and a potential solution to these problems.

2.2. Implementation of glucose monitoring systems. An FPGA-based Fuzzy PD and PID controller for insulin pumps has been presented in [24]. For managing the movement of the infusion pump, fuzzy logic is used by the controller. Blood glucose levels are measured by a non-invasive photoglucometer sensor. The dynamics of the glucose and insulin concentrations are represented using a pair of models by Ackerman *et al.* [25].

In [26] a closed loop control system is discussed. An FPGA-based device utilizing fuzzy logic is used to implement an artificial pancreas. The dynamics of glucose and insulin concentrations are modelled with the use of Bergman's minimal model. The aim of this system is a continuous real-time control of glucose level in patients' blood by modeling glucose-insulin dynamics. Bergman's minimal model is also used in [27], where optimization in power consumption is attempted. Here it is discovered that a lot of energy can be saved by decreasing the voltage and frequency of the FPGA, because the sensor output frequency is a lot lower than maximum FPGA calculation frequency.

A similar artificial pancreas type system is also described in [28]. The main difference is the use of a different mathematical model that was developed using fractional calculus concepts. This model is also used to analyze glucose-insulin dynamics.

The third similar system is presented in [29]. This time the glucose-insulin interactions are calculated using a model developed by Tolic *et al.* [19] The digital differential analyzer algorithm is used for FPGA implementation of the mathematical model.

Another FPGA device for regulating insulin delivery in real time has been described in [30]. As a biosensor, pancreatic β-cells were used for monitoring the patient's blood glucose levels. Patient security and measurement reliability were important problems since incorrect insulin dosage could cause life threatening hypoglycaemia. To decrease the risk, parallel multichannel measurement and signal processing were used.

A simplified Cobelli's model for glucose-insulin dynamics was proposed in [15]. The difficulty of implementing differential equations in FPGA is a major factor for using model order

reduction methods to simplify the Cobelli's model. Root mean square error (RMSE) was used as a main assessment parameter for the implementation accuracy.

An FPGA controller with a recurrent high-order neural network is used for glucose level regulation in patients with Type 1 diabetes [31]. The neural network is trained using an extended Kalman filter and uses a control Lyapunov function to determine the insulin dose required. The implementation is evaluated using a computer simulated patient. The main evaluation parameters are RMSE and standard deviation.

FPGA implementation of artificial pancreas that focuses on fault tolerance is presented in [32]. The authors of this paper make a claim that to correct transient and permanent faults, a technique of dual modular redundancy can be employed. The faults can also be corrected by reconfiguring the FPGA. The reliability of developed medical devices was evaluated according to IEC safety standards.

The main evaluation parameters used in the mentioned implementation cases are calculation speed, accuracy, reliability, power and FPGA resource consumption. FPGA-based implementation provides fast and reliable glucose and insulin estimation, and ultimately assists further development of the artificial glucose level regulation system. FPGA is a promising efficient hardware implementation to be included in a low-power, robust and reliable closed-loop health monitoring system.

The FPGA technology enables programmable implementation of complex digital systems. FPGA is used as an ASIC replacement in low volume applications. Ability of reprogramming enables precise tailoring of implementation to the particular needs.

The main disadvantage of the implementation techniques shown in Table 1 is the less efficient modelling of glucose-insulin interactions. The models used rely on differential equations, neural models and fuzzy logic that can demand a lot of FPGA resources. The MP system approach should be tried to determine if it provides a more effective solution to glucose–insulin interaction modelling problem. One more issue with most of the reviewed techniques is a lack of standardized approach to quality evaluation. Quality criteria in the articles mentioned differ greatly and there is no standard way of evaluation. This makes complete quality comparison impossible, only in some cases individual criteria can be compared.

Table 1
Summary of other glucose monitoring systems

Implementation	Modeling method
[24]	model of Ackerman *et al.*
[26], [27]	Bergman's minimal model
[28]	fractional calculus based model
[29]	model of Tolic *et al.*
[15]	simplified Cobelli's model
[31]	neural network

2.3. Hardware implementation of MP system. MP system was first proposed in [33]. This theoretical paper demonstrates different than in P systems rewriting rules in membranes by defining a metabolic algorithm for computing the evolution of P systems [34] with some initial state and some reaction parameters, such as reactivities and growing factors. The metabolic algorithm is inspired by chemical reactions.

The Metabolic P system modelling of glucose-insulin interactions in the IVGTT was proposed in [7]. The following is an example of this MP system, of which there are several different variations:

$$\begin{aligned} &\rho_1 : \emptyset \Longrightarrow \gamma, && \psi_1 = 0.6; \\ &\rho_2 : \gamma \Longrightarrow \emptyset, && \psi_2 = 0.12\gamma + 1.6 \cdot 10^{-6}\gamma^2\iota; \\ &\rho_3 : \emptyset \Longrightarrow \iota, && \psi_3 = 49.9 + 0.1\gamma^3; \\ &\rho_4 : \iota \Longrightarrow \emptyset, && \psi_4 = 0.84\iota. \end{aligned} \tag{1}$$

The IVGTT MP system is distinguished by parameters of two types: rules (ρ) and regulators (ψ). Glucose (γ) and insulin (ι) interactions within the system are determined by the rules. The rules also determine the exact amount of each substance that is increased or decreased after each reaction. In case of this equation, the amount of glucose is changed when rules ρ_1 and ρ_2 are applied, and the amount of insulin is changed when rules ρ_3 and ρ_4 are applied. The regulators (ψ) determine the rate at which the rules are applied. The rate can either be constant (ψ_1) or variable according to function.

The MP system rules are constant for all IVGTT systems, but the regulators vary depending on which data set is modelled. Therefore, it is possible to adapt the IVGTT MP system for an individual patient, as is shown in [7].

The viability of implementing MP systems in hardware has been examined in [35]. In that paper it has been proven that metabolic P systems can be directly transformed to FPGA. Hardware implementation is suggested as a following systematic implementation method. Preliminary work on MP system implementation in FPGA was reported in [8].

Due to the specifics of MP systems, there are some important challenges when implementing them in FPGA. The floating-point requirement for precise MP system computation requires a large number of programmable logic resources. Using pipelined implementation, the reasonable load of arithmetic resources is hard to achieve in the prediction of insulin injection for a single patient, because of data dependencies in the model of the MP system [7]. Therefore, to reach the full computational load of the MP system, the interleaving technique must be applied. It means, that glucose-insulin interactions need to be computed for several patients on the same IVGTT MP system. Therefore, the requirement of maximum utilization can be achieved when the number of sequentially interleaved patients is defined by the number of clock cycles required to wait for completing a computation of a single patient. The delivery of the parameters to the MP system for a concrete patient needs to be scheduled respectively to signal the arrival to the arithmetic resource.

2.4. Main objectives of the paper. As seen in other discussed implementation attempts at glucose monitoring systems, the elaborateness of glucose-insulin interaction patterns are difficult to obtain. The embedded computers are limited in computational resources and power consumption. For these reasons the implementation must be effective and suitable for the task. In this paper, a new approach to glucose-insulin modelling will be used, namely, the IVGTT Metabolic P system. It does not use differential equations (as seen in Eq. (1)) like most other models, and promises to be an effective way of modelling glucose-insulin interactions in real-time applications.

The first objective of the paper is to create an IP Core for FPGA that is able to predict blood glucose levels based on a single MP system. It is important to operate in real time so that the device can be used to actively monitor patients and be able to support fast decision-making process by medical experts.

Another objective of the paper is to create an IP Core that is suitable for the aggregation of the results of multiple simultaneous MP system calculations in FPGA. As can be seen in other discussed implementation attempts, reliability is an important issue in the medical field. The use of multiple MP system calculations can help to better support a medical decision-making process.

Finally, a prototype of the implemented system is created and investigated. The prototype is based on FPGA partly because it is suitable for parallel computations of multiple patients at the same time, increasing the effectiveness of the system. The reconfigurability of FPGA is also important because, as shown previously, the IVGTT MP system can be tuned to individual patients by using personalized coefficients in MP equations, increasing prediction accuracy. The same prototype system based on FPGA can be easily reconfigured to support different patients by changing the MP system flux coefficients described in Table 2.

3. Methods

3.1. Methods for MP system computation. As stated in [33], the suggested algorithm "is inspired by a chemical reading of the rewriting rules". The equation:

$$\Delta\|S\| = \sum_{\rho \in P} \Delta_\rho \|S\|, \tag{2}$$

as defined in [33], proposes the transformation from rewriting rules to metabolic equations. To calculate the total molar variation of an object S, the contributions of all rules are taken into account and their effects on the concentration of S, where P is a set of rules in the P system, are summed up. In the same paper the following example is given. The set of rules:

$$\begin{aligned} &\rho_1 : S_A S_C \to S_A S_B, \\ &\rho_2 : S_B S_C \to S_A, \\ &\rho_3 : S_B S_B S_B \to S_B S_C, \end{aligned} \tag{3}$$

is linked to coefficients ψ_1, ψ_2 and ψ_3, can be transformed by applying Eq. (2) to metabolic equations:

$$\begin{aligned} \Delta\|S_A\| &= 0 \cdot \psi_1 \|S_A S_C\| + 1 \cdot \psi_2 \|S_B S_C\| + 0 \cdot \psi_3 \|S_B S_B S_B\|, \\ \Delta\|S_B\| &= +1 \cdot \psi_1 \|S_A S_C\| - 1 \cdot \psi_2 \|S_B S_C\| - 2 \cdot \psi_3 \|S_B S_B S_B\|, \\ \Delta\|S_C\| &= -1 \cdot \psi_1 \|S_A S_C\| - 1 \cdot \psi_2 \|S_B S_C\| + 1 \cdot \psi_3 \|S_B S_B S_B\|. \end{aligned} \tag{4}$$

Flux regulation maps and MP system (described in [36]) can be expressed by a construct:

$$M = (S, P, V, Q, \Psi, \nu, \mu, \tau, q_0, \delta), \tag{5}$$

where S is the set of substances, P is the set of reactions, V is the set of parameters, Q is the set of states, Ψ is the set of flux maps, ν is a natural number which specifies the number of molecules, μ is a function which assigns the mass, τ is the temporal interval, q_0 is the initial state and δ is the dynamics of the system.

MP system without the set of states (Q) and dynamics is called an MP graph [36]. MP grammar is the same object just without the elements τ, ν and μ.

In this article, six different MP systems [7] are investigated and implemented in FPGA. There are several different MP grammars of the selected IVGTT system. These grammars differ according to the the selected patient data. However, the underlying structure of all of these grammars is the same. The main difference is the coefficient values of the regulators. If a new IVGTT MP system was developed using different patient data, the basic structure would also remain the same.

The discussed underlying structure that contains four different regulators (where one is a constant) can be presented by the following expression:

$$\begin{aligned} \gamma_n &= \psi_1 - \psi_2(\gamma_{n-1}, \iota_{n-1}); \\ \iota_n &= \psi_3(\gamma_0, \ldots, \gamma_{n-1}) - \psi_4(\iota_{n-1}), \end{aligned} \tag{6}$$

where γ is glucose, ι is insulin and ψ are the flux functions that determine the rate of change of the substances.

The six different fluxes used in Eq. (6) are taken from [7] and summarized in Table 2 (see below).

Most of the previously discussed glucose-insulin interaction models employ differential equations or other more advanced mathematical constructs that require more hardware resources to implement directly or need to be approximated using look-up-tables. MP systems on the other hand can be effectively implemented in hardware by basic mathematical operations.

3.2. Techniques for metabolic P system implementation. The coding style, tools used, required speed and available resources suggest several alternative techniques for MP system implementation on FPGA: soft-core processor-based, high level synthesis or register transfer level.

The precision required for internal signals plays a significant role in FPGA computational performance. The floating-point arithmetic requires multiple clock cycles to acquire a result, and it is difficult to achieve high throughput compared to execution

Table 2
Fluxes of used IVGTT MP systems

MP	Fluxes
MP1	$\psi_1 = 0.6$ $\psi_2 = 0.12\gamma + 1.6 \cdot 10^{-6}\gamma^2\iota$ $\psi_3 = 49.9 + 0.1\gamma^3$ $\psi_4 = 0.84\iota$
MP2	$\psi_1 = 0.6$ $\psi_2 = 0.12\gamma + 1.6 \cdot 10^{-6}\gamma^2\iota$ $\psi_3 = 1.5 \cdot 10^{-5}\gamma^6 + 0.25\gamma^2_{-6} + 0.17\gamma^2_{-8}$ $+ 2.65\gamma_{-16} + 3.6\gamma_{-26}$ $\psi_4 = 0.65\iota$
MP3	$\psi_1 = 0.011$ $\psi_2 = 6.6 \cdot 10^{-5}\gamma\iota$ $\psi_3 = 0.5\gamma^2_{-4}$ $\psi_4 = 0.16\iota$
MP4	$\psi_1 = 0.056$ $\psi_2 = 5.2 \cdot 10^{-4}\iota + 8.1 \cdot 10^{-5}\gamma\iota$ $\psi_3 = 3.76 \cdot 10^{-6}\gamma^7 + 0.74\gamma^2_{-8} + 0.02\gamma^3_{-20}$ $+ 0.21\gamma^2_{-40} + 10^{-4}\gamma^5_{-68}$ $\psi_4 = 0.49\iota$
MP5	$\psi_1 = 0.12$ $\psi_2 = 0.02\gamma + 1.9 \cdot 10^{-4}\gamma\iota$ $\psi_3 = 0.04\gamma^3_{-2} + 3.3 \cdot 10^{-5}\gamma^6_{-6} + 0.44\gamma^2_{-20} + 0.04\gamma^3_{-24}$ $\psi_4 = 0.5\iota$
MP6	$\psi_1 = 0.11$ $\psi_2 = 6.2 \cdot 10^{-4}\gamma\iota$ $\psi_3 = 0.1\gamma^2_{-2} + 0.9\gamma_{-6} + 1.07\gamma_{-10} + 2.4 \cdot 10^{-4}\gamma^4_{-24}$ $+ 5.4 \cdot 10^{-7}\gamma^6_{-32} + 5.3 \cdot 10^{-8}\gamma^7_{-34}$ $\psi_4 = 0.4\iota$

on embedded ARM or even multi-core microprocessors, whose operating frequency is more than ten times that of an FPGA. Therefore, unsigned and fixed HDL libraries are often used for reasonable precision defining a preferred length for integer and fractional parts.

Depending on the RTL coding style, the MP system may be combinational with registers only on the output of the MP system, or perform computations in several clock cycles governed by internal sequential controllers. Different algorithm mapping methods can be used to compare and evaluate the developed IVGTT MP system implementation technique [37].

The following presented FPGA implementation has been performed by coding MP formulae in VHDL using two different described techniques. Then Xilinx ISE Desing Suite software is used for synthesis and programming file implementation. The resulting binary files are loaded on the FPGA development board. The input signals are simulated for the purpose of the research. Real glucose sensor signal processing would require extra FPGA resources and it is not the subject of the research presented in this article. The sensor drivers are required and some data buffers for input signals with extra controller are needed to equalize signals from different patients and deliver data to the MP system in a proper time.

3.3. Unified MP system implementation. The idea of the unified MP system implementation is to develop an MP system that is generic enough to cover all the above presented data fluxes of the IVGTT MP systems used. The inputs and arithmetic operations of IVGTT MP1–MP6 systems share a lot of similarities. This enables some operational logic branches to be turned on or off depending on the exact selected MP system type. The main advantage of the unified MP system application is when a few MP systems with different parameters are required to be implemented on a single chip. The type of MP system required for the calculation is chosen by changing the hardware description models input parameter. Unified MP system implementation has two different versions that are based on pipelined (UniPip) and combinational (UniCom) implementation techniques [38].

The unified pipelined MP system data flow graph is shown in Fig. 1. It has ten different trigger separated stages. This implements the generic IVGTT MP system equation presented in 6. The inputs of this generic MP system accept glucose values that can optionally be delayed depending on the selected MP system. The coefficient values c_i as well as the positions of the adders and multipliers are selected according to the MP system fluxes ψ_i presented in Table 2. The multiplexers are used to switch to the correct branch on each calculation stage. An unused branch can be disabled by multiplying its result by zero. This allows to achieve a unified structure by sacrificing one DSP operation. During the first 10 clock cycles, the data is filling the pipe structure. Then, the first values of glucose and insulin interaction are produced at the system output. These values are stored in shift registers with the depth of 10 that enable them to be used when required in the calculation.

The type of MP system can be switched during interleaved computation of the IVGTT system in 10 different stages. In this case, the constants and selected values of multiplexers must be updated after each clock cycle.

The structure of the unified combinational MP system implementation closely resembles the previously discussed pipelined implementation. The major change is that calculations are performed in one clock cycle, which means that on every clock cycle a different IVGTT MP system can be calculated. The biggest disadvantage of combinational approach compared to the pipelined implementation technique is the potentially lower maximum system frequency because all calculations are performed in one long logic chain during a single clock cycle. To achieve this, in the UniCom implementation the registers are inserted only on the output in the MP system (the structure of the UniCom is similar to UniPip presented in Fig. 1, but only with registers on the output in a data flow graph).

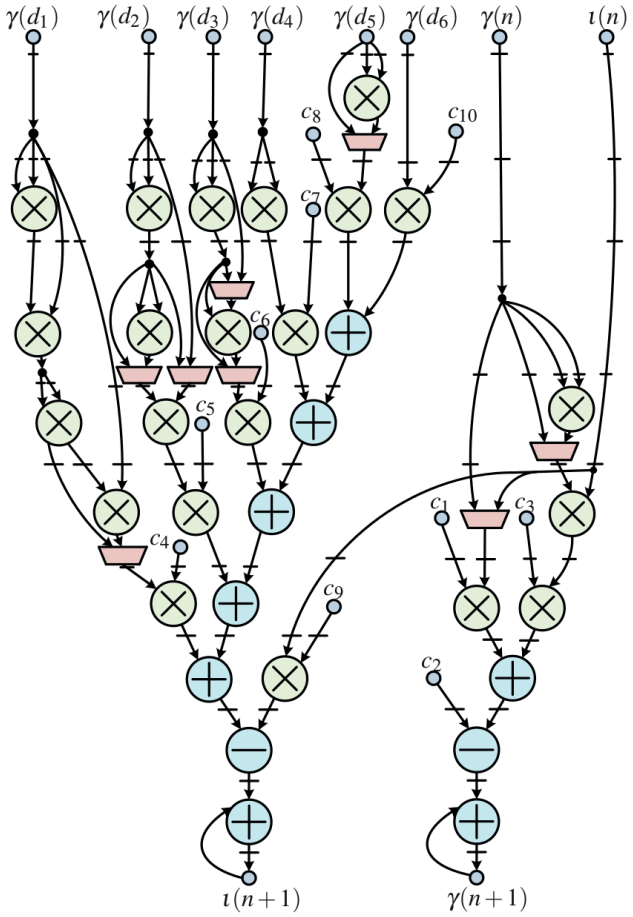


Fig. 1. Data flow graph for UniPiP IVGTT MP system

3.4. Investigation procedure. The described IVGTT MP system implementation techniques are investigated by the use of Zynq-7000 XC7Z020-1 chip on the development board of the Xilinx FPGA. The Zynq-7000 FPGA in total has 220 DSP slices and 53,200 LUTs. All MP systems are implemented in this FPGA using the presented techniques. The integer and fractional parts of the fixed-point arithmetic do not change for the duration of a single experiment. The calculation results are saturated when a value exceeds possible representation range.

3.4.1. Controllable parameters. The implemented system uses fixed point numbers. These numbers also differ in the integer and fractional parts, also called scaling point. That has a major influence on the accuracy of the results. The allocated number of bits for the binary word as well as its parts (integer and fractional) are tuned parameters that determine the suitable balance between accuracy and resource usage. The number of integer and fractional bits is selected by using an algorithm described in [9].

The last tunable parameter is the number and type of IVGTT MP systems implemented applying the unified method. The differing complexity and structure of IVGTT MP system types mean that each of them requires a different amount of resources and can negatively impact on the performance of unified implementation.

3.4.2. Assessment parameters. The overall MP system implementation quality Q_{MP} is defined by the five different normalized criteria $Q_i, \in [0, 100]$:

$$Q_{\mathrm{MP}} = \sqrt[5]{Q_{\mathrm{A}} \cdot Q_{\mathrm{T}} \cdot Q_{\mathrm{R}} \cdot Q_{\mathrm{P}} \cdot Q_{\mathrm{I}}}. \tag{7}$$

This expression of total implementation quality is only valid when the implementation meets the design constraints. This means that each of the five criteria must be greater than 0. As the Q_{MP} parameter depends on the design constraints that are determined by the selected FPGA, it can be used to select the most suitable chip for the implementation.

The quality of accuracy Q_{A} is an inverse value to the calculation error. It is determined by comparing the results to the reference point. The RMSE is normalized to achieve the same dimensions as other quality criteria:

$$Q_{\mathrm{A}} = (1 - E_{\mathrm{RMSE}}) \times 100\ [\%], \tag{8}$$

with normalized RMSE expressed by

$$E_{\mathrm{RMSE}} = \frac{\sqrt{\dfrac{1}{n_{\max}} \displaystyle\sum_{n=1}^{n_{\max}} (\tilde{x}(n) - x(n))^2}}{(x_{\max} - x_{\min})}, \tag{9}$$

where $x(n)$ is reference value at discrete time n, $\tilde{x}(n)$ is an approximated value at discrete time n, $n_{\max}$ is the total length of the approximation results.

For added reliability, the calculation accuracy is also estimated by comparing the normalized mean absolute error (MAE) expressed by:

$$E_{\mathrm{MAE}} = \frac{\dfrac{1}{n_{\max}} \displaystyle\sum_{n=1}^{N} |\tilde{x}(n) - x(n)|}{(x_{\max} - x_{\min})}. \tag{10}$$

The quality of throughput Q_{T} represents the number of clock cycles required for completing a computation. In this case it is represented as a percentage value:

$$Q_{\mathrm{T}} = \frac{f_{\mathrm{val}}}{f_{\mathrm{clock}}} \times 100\ [\%], \tag{11}$$

where f_{val} is value generation frequency (Hz), f_{clock} is clock frequency of the FPGA chip used.

The value generation frequency can be expressed as:

$$f_{\mathrm{val}} = f_{\max} / \tau, \tag{12}$$

where $f_{\max}$ is maximum clock frequency after the place and route stage (Hz), τ is one calculation latency.

The quality of resource usage Q_{R} is the percentage of FPGA resources used. All FPGA resources used are re-calculated to LUT equivalent units so that they can be added together:

$$Q_{\mathrm{R}} = \frac{N_{\max \mathrm{LUT}} - N_{\mathrm{eqLUT}}}{N_{\max \mathrm{LUT}}} \times 100\ [\%], \tag{13}$$

with the total resources used, expressed in LUT equivalent units

$$N_{\text{eqLUT}} \equiv N_{\text{LUT}} + w_{\text{DSP}} N_{\text{DSP}}, \tag{14}$$

where N_{LUT} is the number of logic resources used, N_{DSP} is the number of arithmetic resources used, N_{maxLUT} is the overall LUTs available.

The w_{DSP} coefficient in Eq. (14) is selected according to the architecture of the FPGA MP system model. The w_{DSP} coefficient represents the ratio of LUTs to other FPGA resources. For the Xilinx 7 series FPGA used in the investigation, $w_{\text{DSP}} = 196$ [39].

The quality of power consumption Q_{P} is the percentage of power consumed compared to the maximum available power of this FPGA model:

$$Q_{\text{P}} = \frac{P_{\text{TOCP}}}{P_{\text{TDP}}} \times 100\ [\%], \tag{15}$$

where P_{TOCP} is total on-chip power, P_{TDP} is thermal design power.

The P_{TOCP} is estimated using software developed by the FPGA manufacturer (Xilinx XPower Analyzer in case of Xilinx FPGA). The estimation takes into account the FPGA resource consumption, maximum frequency, ambient temperature and the P_{TDP} of the exact FPGA model used:

$$Q_{\text{P}}(T_{\text{env}}, N_{\text{LUT}}, N_{\text{DSP}}, f_{\text{max}}) = \\ = \frac{P_{\text{TOCP}}(T_{\text{env}}, N_{\text{LUT}}, N_{\text{DSP}}, f_{\text{max}})}{P_{\text{TDP}}} \times 100\ [\%], \tag{16}$$

where T_{env} is environment temperature (which should be kept constant for all experiments), N_{LUT} and N_{DSP} are FPGA resources used, f_{max} is maximum clock frequency.

The quality of interface complexity Q_{I} is the FPGA input-output block resource portion used. These resources are required to transfer primary values to the FPGA and retrieve the concluding result. The available amount of input-output blocks (IOBs) is limited by the specific FPGA model used:

$$Q_{\text{I}} = \frac{N_{\text{IOB}}}{N_{\text{max IOB}}} \times 100\ [\%], \tag{17}$$

where N_{IOB} is the amount of input-output blocks used, $N_{\text{max IOB}}$ is the total amount of IOBs available.

3.4.3. Procedural steps. Before starting the investigation, the previously presented MP systems are implemented in FPGA using the techniques described. It is important to note that the objective of the research was to compare the different techniques, without optimizing a particular implementation according to specific design constraints.

First, the suitable word length is determined by separately implementing all types of IVGTT MP systems. The lowest common word length that is suitable for all systems in selected by consulting the calculated RMSE and MAE values.

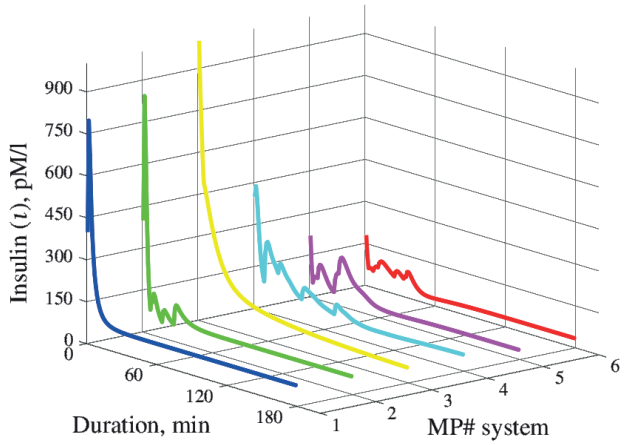
Then, the unified implementation is investigated by analyzing the number of consumed FPGA resources and the calculation speed. UniCom and UniPip implementation techniques are compared according to these metrics.

Finally, the complete quality of the implemented MP systems using the developed unified techniques is investigated to determine their overall suitability for use in real-world applications.

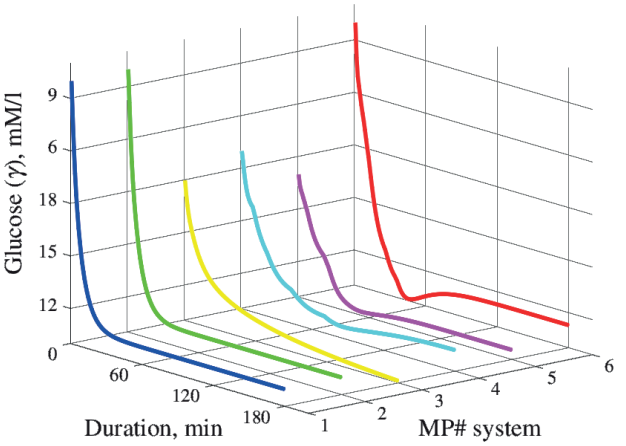
4. Results

4.1. Calculation accuracy investigation. The word length chosen for MP system implementation together with the complexity of the system directly affect the accuracy of the results. The same accuracy results are valid for all implementation techniques because the order of arithmetic operation remains the same despite the technique used. This means that the calculation accuracy shown in this section is compared only when using different word lengths, but not different implementation techniques.

Figure 2(a) presents the signal values of insulin and Fig. 2(b) for glucose. Table 2 contains the IVGTT MP systems that are used to receive these output signals. Double precision floating-point arithmetic according to IEEE Standard 754 is used to



(a) Insulin



(b) Glucose

Fig. 2. Output signal of MP1–MP6 system implementations

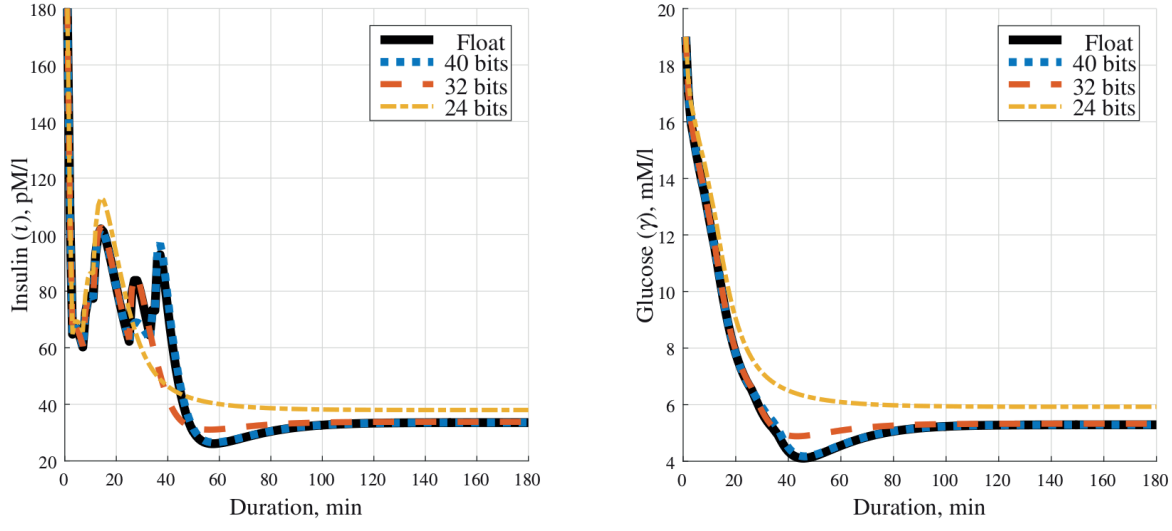
Table 3
Errors of insulin (ι) and glucose (γ) in IVGTT system implementation employing particular word lengths. Highlighted: RMSE of $< 15\%$ and MAE of $< 10\%$

MP	Error	18 bits		24 bits		32 bits		40 bits		48 bits	
		ι	γ	ι	γ	ι	γ	ι	γ	ι	γ
MP1	E_{RMSE}	0.04	0.01	0.01	0.01	10^{-3}	10^{-3}	10^{-3}	10^{-3}	10^{-7}	10^{-7}
	E_{MAE}	0.01	0.01	10^{-3}	0.01	10^{-3}	0.01	10^{-4}	10^{-3}	10^{-8}	10^{-7}
MP2	E_{RMSE}	0.10	0.03	0.10	0.01	0.10	0.01	0.07	10^{-3}	10^{-3}	10^{-3}
	E_{MAE}	0.02	0.01	0.02	0.03	0.02	10^{-3}	0.01	0.01	10^{-4}	10^{-3}
MP3	E_{RMSE}	0.38	0.87	0.26	0.63	10^{-3}	0.01	10^{-3}	0.01	10^{-7}	10^{-7}
	E_{MAE}	0.37	0.85	0.25	0.62	10^{-3}	0.01	10^{-5}	10^{-4}	10^{-8}	10^{-7}
MP4	E_{RMSE}	0.27	0.89	0.27	0.89	0.13	0.10	0.13	0.10	0.10	0.06
	E_{MAE}	0.25	0.87	0.25	0.87	0.06	0.08	0.06	0.08	0.05	0.03
MP5	E_{RMSE}	0.42	0.90	0.08	0.10	0.07	0.03	10^{-3}	10^{-3}	10^{-3}	10^{-3}
	E_{MAE}	0.40	0.88	0.06	0.06	0.04	0.03	10^{-3}	10^{-3}	10^{-5}	10^{-6}
MP6	E_{RMSE}	0.26	0.89	0.07	0.08	0.05	0.02	0.02	10^{-3}	0.01	10^{-3}
	E_{MAE}	0.25	0.88	0.05	0.07	0.02	0.01	10^{-3}	10^{-3}	10^{-5}	10^{-5}

calculate these results. These figures show that each different IVGTT MP system has output signals with varying magnitude and complexity which can have an effect on the accuracy of calculation performed using fixed word length in FPGA. The investigation focuses on the fixed-point implementation using 18–48 bit word lengths. Each IVGTT MP system is implemented separately.

The results of the accuracy investigation are shown in Table 3. As expected, some less complex IVGTT systems can achieve lower E_{RMSE} and E_{MAE}. The acceptable limits are 15% for normalized E_{RMSE} and 10% for normalized EMAE. The acceptable values are shown in blue in Table 2. MP1 and MP2 systems require at least 18b, MP3 and MP4 require 32 b, and MP5 and MP6 systems require 24 b word lengths (see highlighted values in Table 3) to be implemented accurately. This means that 32 b word length must be selected to reliably implement considered types of IVGTT MP systems in FPGA.

An example of insulin and glucose output signals is shown in Fig. 3(a) and Fig. 3(b) respectively. Contrary to the averaged errors in Table 3, it can be seen that the errors change over time and are not uniform. Not shown are 18 b and 48 b implementation cases, as they are either so inaccurate that their signals do not resemble other implementation cases or accurate enough to be almost identical to floating-point results. From the rest of the values it can be seen that in some intervals 24 b implementation accuracy is very high and in others it decreases considerably. Although the average error is acceptable, using higher word length can still be advantageous.



(a) Insulin (b) Glucose

Fig. 3. Output of MP6 systems implemented by fixed or double precision floating point arithmetics

Table 4
Detailed FPGA resource consumption of IVGTT systems implemented using different techniques

Length	Method	f_{max}, MHz	N_{DSP}	N_{LUT}	τ	N_{IOB}	P, mW	N_{eqLUT}	f_{val}, MHz
18 b	UniPip	145	6	665	10	78	162	1841	15
	UniCom	47	6	619	1	78	188	1795	47
24 b	UniPip	114	12	880	10	102	194	3232	11
	UniCom	40	12	818	1	102	223	3170	40
32 b	UniPip	65	84	4302	10	134	335	20766	7
	UniCom	13	84	4317	1	134	416	20781	13
40 b	UniPip	59	172	6005	10	166	430	39717	6
	UniCom	11	172	6312	1	166	521	40024	11
48 b	UniPip	56	220	12636	10	198	489	55756	6
	UniCom	10	220	12705	1	198	744	55825	10
64 b	UniPip	53	216	27207	10	262	587	69543	5
	UniCom	10	216	25838	1	262	1014	68174	10

4.2. Investigation of unified MP systems implementation. UniPip and UniCom IVGTT MP systems are implemented in FPGA. Each of these implementation cases can calculate any of the six different IVGTT MP systems. Table 4 shows a detailed comparison of resource consumption by these implementation cases. When a low word length of 18–24 b is used, FPGA resource consumption is much lower compared to 32 b implementation. In 18–24 b implementations most of the bits are assigned to integer part. This means that some very small numbers (like some constants in the IVGTT MP system) effectively become equal to zero. This causes some DSP operations to not be synthesized at all, which is the reason why the number of used DSPs is so low. Unfortunately, these implementation cases lack accuracy to be used in a reliable medical device, as shown in the previous section.

The difference in resource consumption of UniPip implementation and UniCom implementation is not significant. The DSP cell usage is identical in all cases. In half of the cases the number of used LUTs is lower for each implementation technique. However, the difference is very small, only up to 5% in some cases.

The value generation frequency is around 2 times higher in UniCom implementation, although UniPip implementation achieves up to 5 times higher maximum frequency. Although UniPip can theoretically calculate 10 different systems at the same time, it requires 10 calculations to produce the final result. This is by virtue of the latency specific to the implementation techniques: UniPip implementation has a latency of 10 clock cycles, and UniCom that of 1 clock cycle. The amount of used input-output blocks depends only on the word length used; therefore, it is the same with both implementation techniques. The UniPip implementation consumes less power than the UniCom implementation i.e. almost 20% less when 32 b word length is used.

4.3. Evaluation of complete IVGTT MP system quality. To select the most suitable implementation technique, complete MP system implementation quality (Q_{MP}) is determined. The formula presented in Eq. (7) is used to calculate the Q_{MP}. The constraints used for the calculation depend on the used FPGA model[1]. In this case the maximum power consumption is 4.9 W and the maximum frequency is 200 MHz.

Table 5 shows the complete quality values of both implementation techniques. 32 b word length is used in both of these implementation cases. This means that the accuracy Q_A and the interface complexity Q_I are also identical in both cases. The qualities of power consumption Q_P and resource usage Q_R are slightly higher when the unified pipelined technique is used. The quality of throughput is two times higher when the unified combinational technique is used. As a consequence of higher throughput, the complete implementation quality is higher when the unified combinational implementation technique is used.

Table 5
Quality estimates for 32b unified IVGTT MP system implementation techniques

Quality	UniPip	UniCom	Proportion
Q_A	95.74	95.74	1
Q_T	3.25	6.50	0.5
Q_R	78.44	78.42	1
Q_P	93.16	91.51	1.02
Q_I	33.00	33.00	1
Q_{MP}	37.59	43.02	0.87

When the UniCom technique is used to implement IVGTT MP systems using longer words for increased accuracy, the change in quality characteristics is shown in Fig. 4. When

[1]Zynq-7000. https://www.xilinx.com/support/documentation/data_sheets/ds187-XC7Z010-XC7Z020-Data-Sheet.pdf

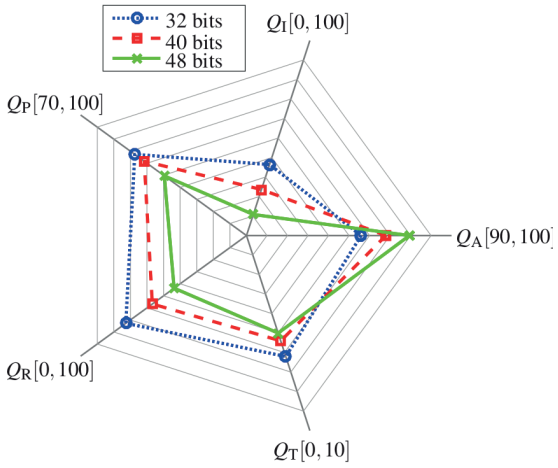


Fig. 4. Quality of UniCom implementation using various word lengths. The minimum and maximum values of each axis are shown in square brackets

longer words are used, the qualities of resource usage and interface complexity are greatly decreased. The improvement in accuracy, as shown in Table 3, is not very significant to warrant the use of these word lengths, although it can be desired in some cases where very high accuracy is required.

The other previously discussed implementation cases do not provide sufficiently detailed parameters about their FPGA implementation. This article is the first attempt to comprehensively describe the quality criteria of insulin-glucose interactions implemented in hardware. Therefore, only some of the investigation results can be compared.

In [15] the implementation of Cobelli's model achieves RMSE of not higher than 5%, which is very close to the quality of 32 b IVGTT implementation that has an average of 4.26% RMSE. In [31] the RMSE achieved is higher, i.e., up to 12% in the tracking phase, the number of logic elements used is 3.3 times higher, but the number of arithmetic resources used as well as power consumption are around 2 times lower.

5. Conclusions

The results presented in the paper confirm the following findings:

1. The novel FPGA implementation of MP systems techniques take into account all known IVGTT MP systems and ensure less than 15% RMSE if 32 bits word length is used.
2. The proposed MP system quality metric and its pictorial representation evidently separate different MP system implementation quality and let concentrate on quality aspects attributed to these systems.
3. The IVGTT MP system implementation way – unified combinational – guarantees 2–3 times faster execution in comparison to the unified pipelined approach.

The presented results prove that MP system methodology-based IVGTT implementation in FPGA technology is reasonably precise and sufficiently flexible to be used effectively in multi-user scenarios.

In further research, the use of a hybrid precision for MP system calculation in FPGA should be examined. This could potentially help to better optimize the balance between the calculation accuracy and other quality criteria.

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