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FPGA-BASED SYSTEM FOR IMAGE PROCESSING IN HIGH RESOLUTION INFRARED CAMERA

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Summary: In article a digital system for high resolution infrared camera control and image processing is described. The camera is built with use of bolometric focal plane array of size 640 by 480 detectors. Designed module controls the microbolometer Focal Plane Array (FPA), performs non-uniformity correction, bad pixel mapping and controls the process of displaying the thermal image. The system was designed in such a way, that signal processing algorithms, needed for specific tasks, can be implemented in it without hardware modifications. It was achieved by the application of a FPGA device and microprocessor unit, which both can be re-programmed inside the system. This scientific work is funded as a development project from science funds for years 2009-2011.

Keywords: thermal imaging, signal processing, image processing, FPGA

1. INTRODUCTION

Thermal cameras are more and more often used as observation devices in numerous areas, like security systems, military systems, reconnaissance, detection of chemical agents and many more. In all of the applications it is very important to obtain the accurate image of observed scenery. Because thermal cameras are quite common, they should be easy to operate. As a result, the methods for automatic analysis and processing of thermal image have to be implemented, which simplify the user interface by automatic setting of camera parameters. The applied methods should also enhance the capabilities of a thermal camera in detection and recognition of certain objects and phenomena, making it a more versatile tool than just an observation device. The actual methods implemented in a given device depend on the specific application and the type of analyzed data [1], therefore they couldn't be universal ones or chosen once and for all. Additionally, often the systems for thermal image processing and analysis must have compact size and low power requirements.

In high resolution cameras a robust and efficient image processing system is needed. In handheld and mobile systems the power consumption of such processing system is also a key parameter. Additionally a use of modern infrared image processing module in various types of cameras and applications should be possible without appreciable hardware changes. In infrared image processing module used in high resolution camera,

an amount of data to be processed is significant, but it has to be processed in well defined and short time. The processing delays of image processing modules have to be constant and low, and cannot accumulate in time. Low latency of operations can be obtained with use of parallelization techniques [11]. The amount of a data needed to be processed in thermal camera depends on the resolution of the camera and the frame rate. In Table 1 there is a comparison of data stream volume for three different standard video resolutions and several frame rates.

Table 1. Data stream volume and a maximum time of one pixel(detector) readout time for chosen frame rates and resolutions

Resolution	**Pixel (detector) count in frame**	**Pixel count read in one second and maximum detector readout time**			
		25 Hz	**30 Hz**	**50 Hz**	**60 Hz**
320×240	76 800	1 920 000	2 304 000	3 840 000	4 608 000
		520.83 ns	434.03 ns	260.42 ns	217.01 ns
384×288	110 592	2 764 800	3 317 760	5 529 600	6 635 520
		361.69 ns	301.41 ns	180.84 ns	150.70 ns
640×480	307 200	7 680 000	9 216 000	15 360 000	18 432 000
		130.21 ns	108.51 ns	65.10 ns	54.25 ns

Generally speaking, electronic circuitry of a thermal camera consists of three basic modules [2]: focal plane array module, control and image processing module, display module. General, simplified block diagram of thermal camera electronics is presented in Fig. 1. There is an A/D converter inside focal plane array proximity board, which transforms raw image signals into digital data, transferred further to control and image processing module. There are also analog power supplies with proper filtering and noise suppression circuits, providing all main voltages for Focal Plane Array (FPA).

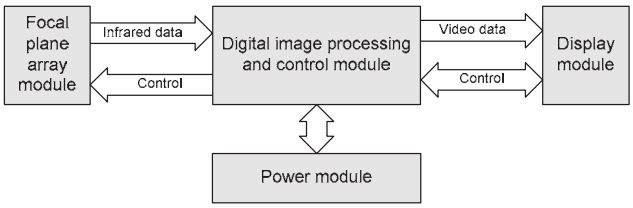

Fig. 1. Block diagram of an uncooled thermal camera

Control and image processing module is responsible for proper Focal Plane Array operation. For proper FPA operation a series of digital and analog signals has to be generated. Digital signals are used to set timing parameters of array, while analog signals are used to bias arrays internal readout circuit with proper voltage levels [3]. Maintaining proper levels of supplying voltages is very important when there is a need to work in the broad temperature range. Those voltages mostly determine the sensitivity of the detectors and the level of output signal. The voltages are driven by automatic microcontroller-based control unit. Microprocessor reads the analog signal from an array by

A/D converter, analyzes it and adjusts the voltage levels accordingly. The voltages are set by D/A converter, which communicates with the microprocessor over SPI bus.

Display module visualizes the video data in VGA format on CRT monitor, LCD or OLED display. RED, GREEN, BLUE video signals and line synchronization (HS) and frame synchronization (VS) pulses are generated by control and image processing module. Video signal is calculated from analog array signals converted to digital form, taking into account calibration coefficients stored in FLASH memory of control and image processing module. The digital video data are then converted back to analog form by a special block consisting of three D/A converters.

2. CONTROL AND IMAGE PROCESSING MODULE

The function of control and image processing module is to control all other camera blocks and to convert the data from detector array. The main operations performed by this module are: control of array module in order to read-out all the detectors, perform non-uniformity correction, bad pixel mapping and prepare data for the display module.

Control and image processing module was built around two main components: FPGA device and a microcontroller. FPGA device performs image data processing, which requires considerable amount of processing power. It deals with the generation of signals controlling array read-out, correction of the non-uniformity of detector response across the array, mapping of bad pixels and generation of input signals for display module. Microcontroller unit controls the camera and performs other tasks that do not require much processing power. Block diagram of control and image processing module with FPGA device is shown in Fig. 2.

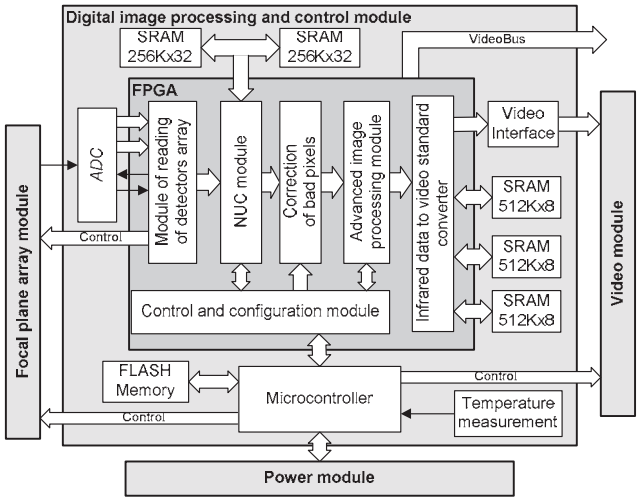

Fig. 2. Functional diagram of FPGA-based control and image processing module

The main role of a microcontroller is to supervise every stage of image processing. Its main tasks are:

- controlling the FPA supply voltages,

- FPA temperature measurement,
- ambient temperature measurement,
- shutter control,
- controlling of auto-calibration process,
- display configuration,
- modification of NUC (NonUniformity Correction) parameters,
- calculation of parameters needed to correct NUC coefficients.

To realize these tasks the STM32F103 microcontroller from STMICROELECTRONICS was chosen. This integrated circuit is a member of 32-bit ARM cortex family. The architecture of the cortex processor is designed to execute 32-bit program code with high efficiency. This type of microcontroller from STM has rich peripherals like 12-bit analog-to-digital converter, 32 timers and communication modules compatible with standards like SPI, I2C, CAN and UART. What is more, a STM32F103 microcontroller is rich in general purpose input-output ports and external memory interface. The external memory interface was used to access peripherals like memory or FPGA.

The EP2C35F672 device by ALTERA is the chosen FPGA type. This device combines processing efficiency with relatively small power consumption. It has a large number of I/O ports, 33 216 logic elements (LEs), 483 840 bits of RAM memory, four PLL circuits for the generation of required signals and 35 embedded hardware multipliers. It should be mentioned that those multipliers make it possible to design functional blocks in FPGA device capable of high-speed complicated calculations with low usage of logic elements and relatively small power consumption.

In every video processing system there is vast amount of data that has to be processed in a given time period [9, 11]. Those data have to be processed in real time without significant delays. It should be pointed out that because of continuity of image processing the introduced delays should be constant, no increase of delays over time is allowed. This means that parallel image processing has to be used.

In order to obtain useful infrared image from the focal plane array a series of image processing algorithms has to be used beginning with detectors nonuniformity correction, bad pixel replacement and ending with image displaying. To realize these image processing tasks in real-time, the following modules were implemented in FPGA device:

- FPA read-out,
- NUC correction module [4],
- bad pixel mapping module,
- image processing module,
- image display module.

2.1. VIDEOBUS

The VideoBus communication bus was implemented in FPGA for image data transfer between all functional blocks contained inside FPGA. As a result the execution order of image processing may be altered without the need to change the functional blocks. This provides considerable flexibility in the design of thermal image processing system. The VideoBus is accessible by a separate connector, which allows monitoring the operation of digital image processing module at every stage of image processing.

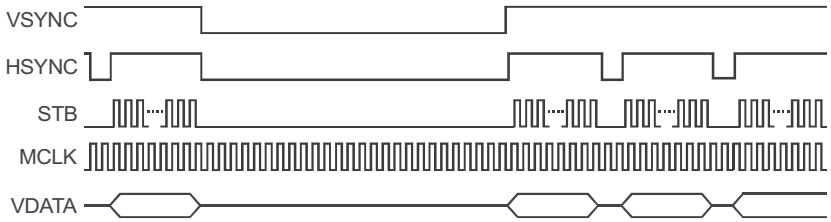

Fig. 3. VideoBus timing diagram

Image data bus consists of 14-bit data bus, vertical (VSYNC) and horizontal (HSYNC) synchronization signals and strobe signal (STB). Signal VSYNC is high during the transmission of the image frame, whereas HSYNC signal is high during consecutive row read-outs. The change of STB signal from low to high (rising edge) indicates that VDATA data bus contains valid (stable) video data for read-out. Those data are kept on VDATA bus as long as STB signal is high. Time characteristics of VideoBus data signals are presented in Fig. 3.

2.2. FPA READ-OUT MODULE

The main tasks of detector array readout module is generation of signals driving internal circuitry of detector array and interfacing with analog to digital converter connected to it. To achieve this there is a need to design a special digital machine which generates a series of signals connected to array via external IO interface. As a result sequence of signals form FPGA, the detector array starts to send analog signals read from consecutive detectors. This signal is a response of the detector and is proportional to the incident infrared radiation. FPA read-out module logic controlling readout process was realized as functional block in FPGA device. Its block diagram is presented in Fig. 4.

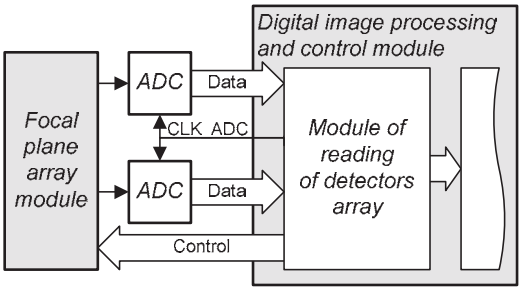

Fig. 4. Schematic of detector array read-out module

High resolution infrared arrays (640x480 and higher) have commonly more than one output, providing simultaneous readout from several detectors. For this type of arrays there is a need to interface to all outputs using several synchronized analog-to-digital converters. The digital signals to microbolometric array have two purposes. One is to provide proper timing during readout from detectors. To do this in UL 04 17 1 detector array a RESET, INT, MC are used [9]. These digital signals provided to array allow an access to analog signals from the detectors. The signals can be then read synchronously with CLK_VIDEO ADC.

The control circuit was designed to read out the data from all array detectors. The purpose of FPA read-out unit is to obtain digital representation of an analog detector output signal, proportional to the incident IR radiation. The data are then transmitted to the next camera modules over image data bus (VideoBus). Further data processing requires the conversion from analog VIDEO signal into digital form (DVIDEO). This conversion is performed by an A//D converter, which requires clock signal (CLK_VIDEO) for the controlling of the conversion process. Result of signal generation in detector array read-out module is shown on Figure 5.

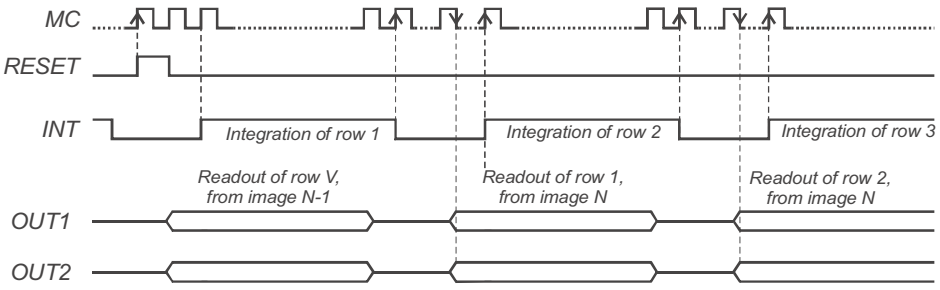

Fig. 5. Timing diagram of control signals for ULIS UL 04 17 1

To generate synchronization signals a module was realized with use of 5-state machine and two counters one for counting clock cycles during row readout, second to count rows in the frame. First counter is used to generate INT signal for row integration while second is used to generate RESET signals during frame initialization. These two counters are also used in generation of VideoBus signals like: VSYNC, HSYNC, STD, MCLK, VDATA0 and VDATA1. The characteristic feature of UL 04 17 1 microbolometer array is, that the signals on the output of array are delayed by the time of one row from the integration trigger signal. This is because of internal structure of the array; first the detectors are integrated and then are read and sent to external system. Example signals generated for UL 04 17 1 microbolometer array are shown on Fig. 6.

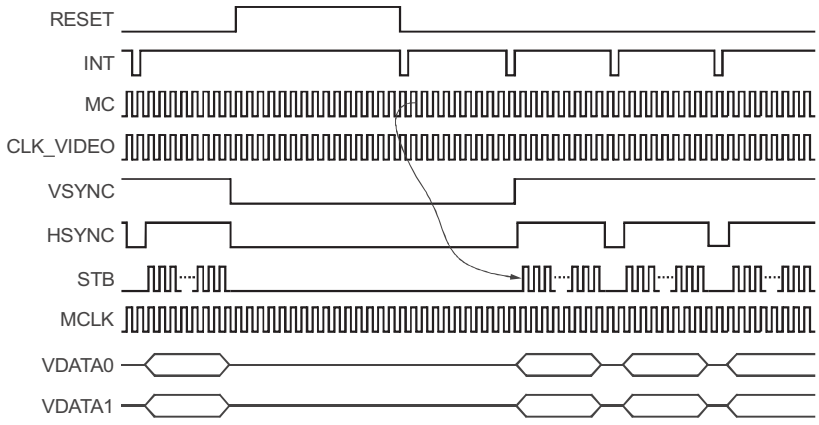

Fig. 6. Timing diagram of control signals for ULIS UL 03 04 1 microbolometer FPA with A/D converter latency taken into account

Used in this solution ADC converter AD9251 from ANALOG DEVICES has its own latency needed to process incoming analog signal equal to 9 clock cycles. This latency has to be taken into account in generation of VideoBus signals in this first module.

2.3. BAD PIXEL MAPPING MODULE

In every real array there are bolometers that do not function properly. The correction for those bad pixels is an important problem. Bad pixels are identified at the thermal camera calibration stage on the basis of their response. The data containing bad pixel locations are stored in memory. Each pixel is described by corresponding one-bit data, where "1" means bad pixel, which has to be corrected, and "0" means good one and no correction is necessary. The content of bad pixel memory determines if the pixel output is displayed, or not. In case of a bad pixel the value from the previous good one is displayed instead. The simplified diagram of the operation of bad pixel mapping module is shown in Fig. 7.

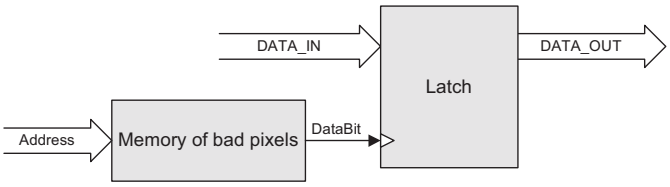

Fig. 7. Scheme of operation for bad pixel mapping module

2.4. IMAGE DISPLAY MODULE

To obtain optimised image quality of infrared image, a specially selected integration time of detector has to be used for readout procedure. This implies that the detector can generate a fixed frame rate which is different than frame rate of standard video output. A mismatch between data read-out frequency and output video frame rate can be overcome with use of special frame rate converter. In case of thermal camera the actual frame rate of video output is often higher than FPA read-out frequency. A special module has to be introduced, which is schematically presented in Fig. 8.

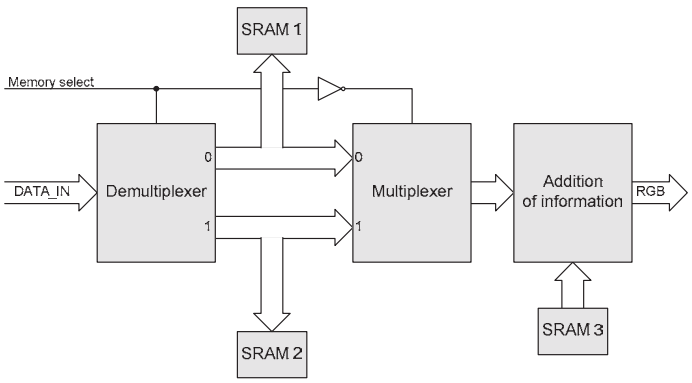

Fig. 8. Block diagram of image display module with additional information overlaying capability

Image display module uses two memories SRAM 1 and SRAM 2. The pixel signals are stored in one of them (e.g. SRAM 1). In the same time the data to be displayed are read from the other memory (in this case SRAM 2). When all of the image pixel data are read from an array, the Memory select signal switches the roles of SRAM 1 and SRAM 2 memories. Now data to be displayed are read from SRAM 1 and pixel data are written into SRAM 2.

Other function performed by image display module is overlaying additional information onto the output video stream. This superimposed information contains user interface controls and camera status data, for example battery level.

Image display module contains also VGA controller, which sends control signals to the display.

2.4. NUC CORRECTION MODULE IN FPGA

Microbolometer detector array exhibits certain non-uniformity of response of detectors to the same power of incident IR radiation [2, 5, 6, 8, 12]. Because of this non-uniformity a fixed pattern noise (FPN) can be observed in the output image, which degrades spatial Noise Equivalent Temperature Difference (NETD) of a thermal camera. Typical non-uniformity level for microbolometer arrays is about 8-10% (std/mean).

There are several methods for non-uniformity correction and most of them rely on digital processing of array output signal. The correction data, so-called NUC coefficients are determined during camera calibration against uniform IR sources.

Basic method of NUC correction is TPC (two-point correction) procedure. TPC algorithm is conducted according to the following formula [8, 14]:

$$N_{ij}^{*} = G_{ij} N_{ij} + O_{ij} \,, \tag{1}$$

where N_{ij} is the response of the detector at array coordinates (i, j) , G_{ij} and O_{ij} are the correction coefficients for gain and offset, respectively, and N_{ij}^{*} is corrected value of detector output signal. In case of TPC corrections the coefficients are given by [8, 14]:

$$\begin{aligned} G_{ij} &= \frac{N(T_H) - N(T_L)}{N_{ij}(T_H) - N_{ij}(T_L)} \\ O_{ij} &= \frac{N(T_L) N_{ij}(T_H) - N(T_H) N_{ij}(T_L)}{N_{ij}(T_H) - N_{ij}(T_L)} \end{aligned}, \tag{2}$$

where $N_{ij}(T_H)$ and $N_{ij}(T_L)$ represent digital values of detector response for high (T_H) and low (T_L) temperature of uniform IR source, $N(T_H)$ and $N(T_L)$ are the mean values of detector response for the temperatures T_H and T_L. Image data bus have width of 14-bit (defined by the resolution of an A/D converter) and NUC correction coefficients are 16-bit [5, 7, 8]. The structure of equation (1) implies that digital circuit for TPC correction has to perform one multiplication and one addition. In case of fixed point numbers the resulting coefficients should be re-scaled in order to increase accuracy. The block diagram of hardware module for TPC correction is shown in Fig. 9

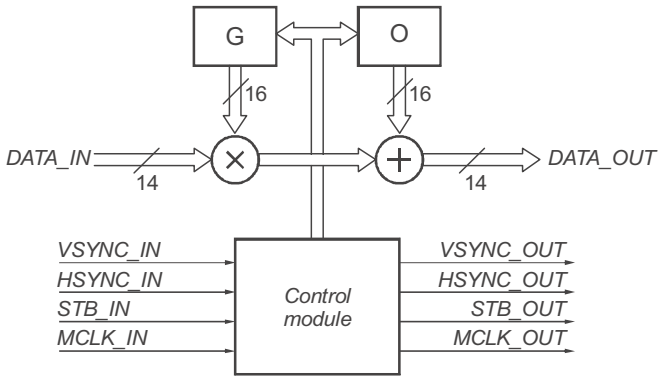

Fig. 9. Block diagram of hardware NUC module

Non-uniformity correction is performed „on the fly", which means that the time needed to perform the calculations is shorter than single detector read-out time. Additionally the input and output data format for the NUC correction module conforms to the VideoBus standard. Finally the NUC correction module was designed, which performs TPC correction, generates VideoBus output signals and memory address, where correction coefficients are stored.

a) b)

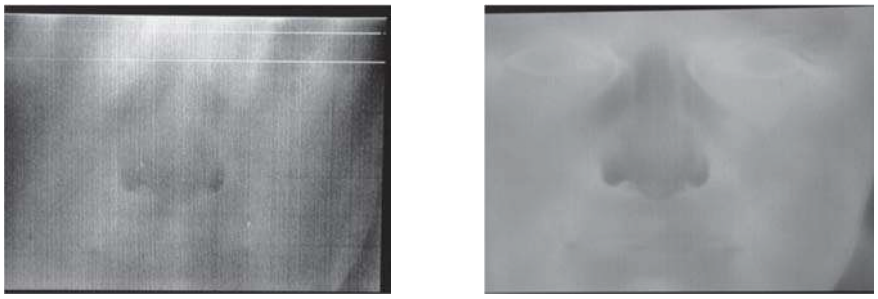

Fig. 10. Thermal image before (a) and after (b) NUC correction

NUC correction module was described in VHDL language as a parameterized entity. The designer can adjust such parameters as array size (rows and columns) and the length of data word for both input data and calculated correction coefficients. As a results such module can be applied for any given infrared focal plane array. There are two thermal images shown in Fig. 10. First image is obtained without, and the second one after the NUC correction performed by the designed module.

3. SUMMARY

On the basis of functional diagram presented in Fig. 2 the control and image processing module was designed and implemented in a FPGA device. As a result the elec-

tronic board for the read-out and image processing was manufactured on a multi-layer PCB.

The operation of the FPGA-based module was described in VHDL language using several complex finite-state machines. The designed machine use accordingly described internal counters for the switching of their states, by synchronous counting of core clock pulses. VHDL language was also used to define user interface. This interface is used for the setting of camera parameters and for the monitoring of the actual status, using several registers accessible via microprocessor. The additional module that generates simulated A/D converter data was implemented in the project for the testing of array read-out circuit. The project was simulated and then synthesized in ALTERA's Quartus II environment.

Microcontroller circuit was programmed using hybrid method, a mixture of assembler and C programming language. It combined the fast execution of assembler routines with compact code of C procedures in parts where the speed was not critical. The microprocessor with this software successfully controlled the camera with adequate effectiveness.

The simulations and laboratory tests [2, 5] conducted with the use of logic analyzer proved the flawless operation of the designed control and image processing. Simulated timing parameters are in accordance with dynamic parameters described in the specifications of FPA array read-out circuit.

The worst case analysis of timing parameters was also performed for all modules implemented in a FPGA device. Timing analyzer summary revealed that maximal total delay introduced by combinational circuits is 5.548 ns, and theoretical maximum frequency of the VideoBus is 68.1 MHz. These parameters are well above the actual needs as the real frequency of VideoBus in the designed FPA read-out module is only 6.25 MHz.

Additional advantage of the presented design is its flexibility, because the changes in the performed functions and algorithms can be done without hardware modifications. Furthermore, the modules implemented in the FPGA device were described using standard VHDL language, so they can be implemented in any programmable structure.

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MODUŁ DO PRZETWARZANIA OBRAZU Z MIKROBOLOMETRYCZNEJ KAMERY PODCZERWNIENI Z ZASTOSOWANIEM UKŁADU FPGA

Streszczenie

W artykule opisano uniwersalny cyfrowy system sterowania i przetwarzania dla kamery termowizyjnej z matrycowym detektorem bolometrycznym rejestrującym promieniowanie w zakresie widmowym w przedziale 8÷12 μm. Najważniejszym zadaniem systemu jest odczytanie sygnałów z poszczególnych detektorów matrycy oraz korekcja wartości wzmocnienia i napięcia przesunięcia charakterystyki czułości dla każdego detektora matrycy. Następnym zadaniem jest przetworzenie analogowych sygnałów z matrycy na postać cyfrową i ich zamiana na obraz termiczny. Dane odczytane z matrycy są przekazywane do następnych modułów kamery termowizyjnej za pomocą magistrali danych obrazowych. Układ sterowania odczytem jest ponadto wyposażony w magistralę sterowania za pomocą, której można ustawić parametry generowanych sygnałów dla matrycy mikrobolometrycznej. Parametry, które mogą podlegać zmianie to liczba obrazów odczytywanych w ciągu sekundy oraz czas całkowania sygnału z detektorów. W kolejnych modułach przetwarzania obrazu dokonywane są operacje takie jak np. korekcja niejednorodności detektorów matrycy, wykrywanie i usuwanie wadliwych pikseli, zaawansowane metody poprawy jakości obrazu, metody wspomagające wykrywanie i identyfikację obiektów. Dzięki zastosowanej architektury systemu możliwa jest adaptacyjna zmiana działania systemu bez konieczności stosowania znaczących zmian sprzętowych. Praca naukowa finansowana ze środków na naukę w latach 2009-2011 jako projekt rozwojowy.

Słowa kluczowe: Termowizja, przetwarzanie obrazu, FPGA