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A 128-CHANNEL HIGH PRECISION TIME MEASUREMENT MODULE

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Abstract

In the external target experiment for heavy ion collisions in the HIRFL-CSR, Multi-Wire Drift Chambers are used to measure the drift time of charged particles to obtain the track information. This 128-channel high precision time measurement module is designed to perform the time digitization. The data transfer is based on a PXI interface to guarantee a high data rate. Test results show that a 100 ps resolution with a data transfer rate up to 40 MBps has been achieved; this module has also been proven to function well with the detector through a commissioning test.

Keyword: high precision, time measurement, PXI, data transfer, commissioning test.

1. Introduction

The Cooling Storage Ring (CSR) project in the Heavy Ion Research Facility at Lanzhou (HIRFL) consists of a main ring (CSRm), an experiment ring (CSRe), and a radioactive beam line (RIBLL2) to connect the two rings [1, 2]. An internal target experiment for hadron physics and an external target experiment for heavy ion collisions are being built at the CSR complex. As for the external target experiment, it is composed of one Start Time Detector, one γ Detector, one Big Dipole, six Multi-Wire Drift Chambers (MWDC), three Time of Flight Walls (TOF Wall), one Neutron Wall, etc, as shown in Fig.1.

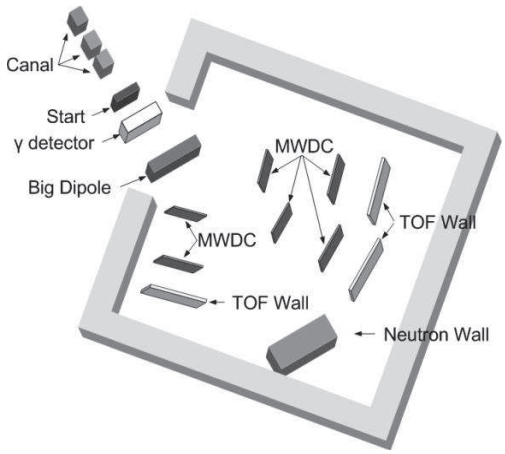

Fig. 1. Detector system of the CSR external target experiment.

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The MWDC is responsible for the detection of charged tracks [3]. Ionized electrons are generated when charged particles traverse through the MWDC; by measuring the ionized electrons' drift time, the track information of the particles can be obtained. Meanwhile, the energy loss, dE/dx, of the charged particles traversing the MWDC can be attained through charge measurement, which is used for particle identification [4].

Regarding the track information measurement, the position resolution is required to be better than 200 μm, in which the error contributed by the electronics should be less than 15% (30 μm). Considering the electrons' average speed of 5.5 cm/μs, the 30 μm position resolution corresponds to a time resolution of 545 ps [5]. Besides, the total number of the MWDC anode wires is up to 3264; therefore, a high density readout electronics architecture is necessary.

The MWDC readout electronics consists of two modules, a SFE16 front end module and a high precision high density time measurement module, as shown in Fig.2. The SFE16 front end module is connected directly to the MWDC. The SFE16 chips are employed to implement the Time-Over-Threshold (TOT) method [6, 7]–

converting the input charge information to a corresponding output pulse width. The TOT method consists in presenting the amplified and shaped detector signals to a comparator with a preset threshold. Signals above the threshold generate at the comparator output a logic pulse whose width is the Time-Over-Threshold. The SFE16 is a 16-channel integrated ASIC, with each channel composed of a charge-sensitive preamplifier, a pole-zero stage, two selectable filters, an amplifier, a discriminator and a "LVDS (Low-Voltage Differential Signaling) compatible" current driver [8]. The time measurement module imports the output signals of the SFE16 front end module through 5-meter cables based on LVDS. The LVDS can effectively decrease the common mode noise and the power consumption.

The measurement module is designed to integrate 128 high precision channels. To achieve this, the Very High Density Cable Interconnect (VHDCI) and the High Performance Time-to-Digital Converter (HPTDC) are adopted. As for the data transfer, the PXI (PCI eXtensions for Instrumentation) [9] structure is used in the system to guarantee a high transfer rate.

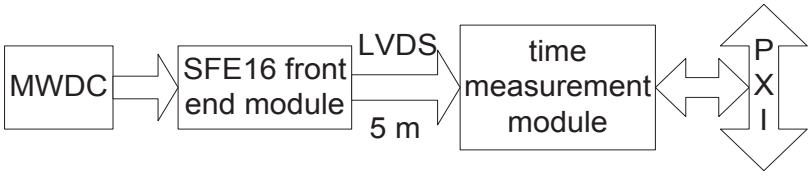


Fig. 2. Block diagram of the MWDC readout electronics.

2. Architecture of the time measurement module

The time measurement module is based on the 6U PXI standard. As shown in Fig.3, 128 signals (corresponding to the outputs of 8 SFE16 front end modules) are imported via VHDCI. After being buffered by the LVDS drivers, the signals are digitized by 4 HPTDC chips, which are controlled by an FPGA.As the four HPTDCs share the data bus to accomplish the data transfer with the FPGA, which can increase the routing branches and cause signal distortion, a bus transceiver is adopted to reduce this influence. The readout data of the three HPTDCs is transferred to the bus transceiver. The output of the bus transceiver and the fourth HPTDC readout data are connected together with the FPGA. This FPGA is also responsible for the data readout from the HPTDCs according to the trigger signal from the front panel or PXI bus, Non-Linearity correction, commands and data communication with the PC via a CPLD through the PXI interface, etc. The on-line modification of the FPGA logic can also be achieved with the PS configuration mode through this CPLD. A 40 MHz

system clock is distributed by a low jitter chip (SY89828) to the 4 HPTDC chips, as well as the FPGA and the CPLD.

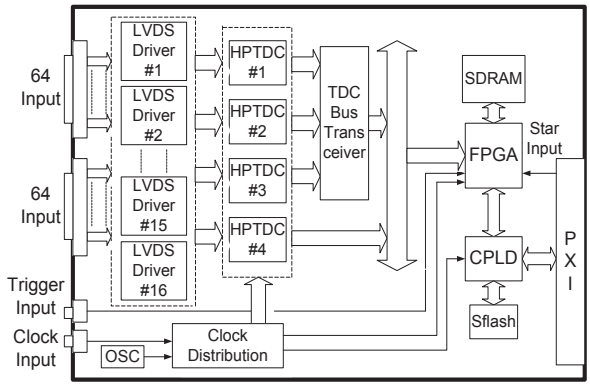


Fig. 3. Schematic of the time measurement module.

To achieve a good time resolution and system reliability, special care is taken on the signal integrity (SI), such as impedance match, the design of complete ground layers in the PCB (Printed Circuit Board), differential transmission of important signals, etc.The Very High Density Cable Interconnect (VHDCI 743370051, Molex Company) is employed to provide sufficient channel number in the limited PXI-6U panel width, with a good signal shielding between adjacent channels.

3. Time-to-digital conversion

The HPTDC is a high quality data driven TDC designed by the Micro electronics group at CERN (European Organization for Nuclear Research) [10]. Based on the time interpolation technique, an optimum time resolution of 25 ps can be achieved. It can work in four different modes - low resolution mode, middle resolution mode, high resolution mode and very high resolution mode, with corresponding time resolution of 781 ps, 195 ps, 98 ps and 24 ps, respectively.

In this system, the high resolution mode is selected for high-density purpose, with 32 channels integrated in each HPTDC, and a time resolution as good as 100 ps.

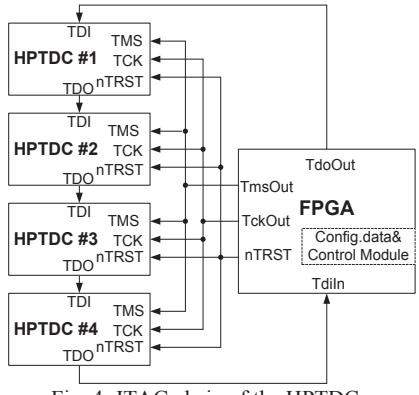


Fig. 4. JTAG chain of the HPTDCs.

To simplify the control of multiple HPTDC chips within one module, the 4 HPTDCs are assigned into a chain to receive the configuration data via a common JTAG (Joint Test Action Group) port. As Fig. 4 shows, the HPTDC receives the configuration data sequence via the TDI pin, and passes the data through the TDO pin to the next HPTDC. The control signals of the 4 HPTDCs, including TMS, TCK, nTRST, are combined together to connect with the FPGA.

As for the data readout, all the 4 HPTDCs are connected to a parallel readout interface. When a trigger signal is received, the HPTDCs output their corresponding data blocks to the FPGA in sequence with a token signal passing through the "Token Ring", as shown in Fig. 5.

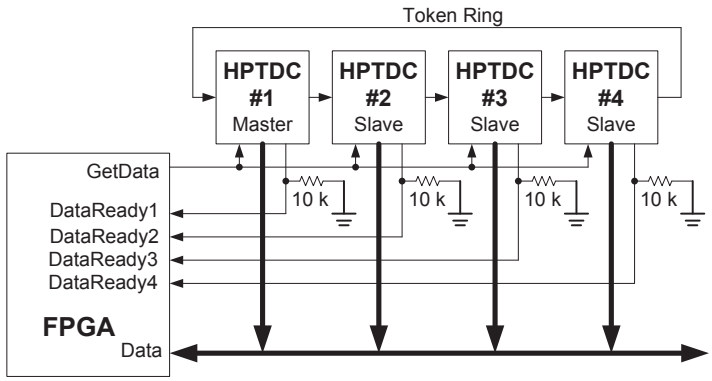


Fig. 5. Parallel readout with one master HPTDC and a simple readout controller.

As shown in Fig. 6, the FPGA receives the external trigger and passes it to the 4 HPTDCs through a common trigger signal line. Then the readout process is started by the first HPTDC which functions as a master; it asserts the 'DataReady1', generates a group event header and outputs the corresponding data section on the parallel interface. When the data transfer is finished by the first HPTDC, it will pass a token signal to the next HPTDC, followed by a similar process for the next 3 HPTDCs. After all the data is sent to the FPGA, a group event trailer is added by the first HPTDC to complete the whole readout process.

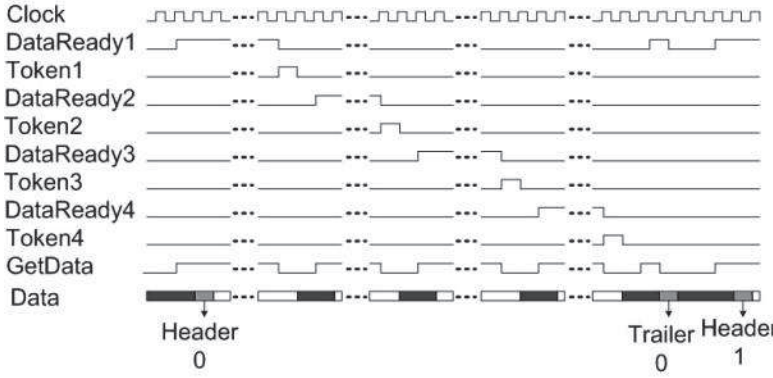


Fig. 6. Time sequence of the Parallel readout.

The overall readout is synchronized with a 40 MHz clock signal. When the FPGA observes the assertion of the 'DataReady', it asserts the 'get data' signal immediately and registers the data from the HPTDC. The 'get data' signal is checked by the HPTDC to determine whether the FPGA responds correctly. The 'DataReady' is a tri-stated signal, and it is in a high

impedance state when the HPTDC does not occupy the token signal; therefore, an external pull-down resistor of 10 kΩ is placed to maintain a low level. When the first HPTDC finishes the data transfer, it generates a token signal that starts the same transfer process of the next HPTDC.

4. Logic design

A single FPGA chip (EP2C20F484) is employed to process digital signal and transfer data. As mentioned above, the 4 HPTDCs are configured by this FPGA; the configuration data is imported into the FPGA from the PC via the CPLD through the PXI bus, and then written into the 4 HPTDCs. The output data are read out directly by this FPGA, and then processed by the INL (Integral Nonlinearity) calibration logic. The final data results are transferred to the CPLD and further to the PC through the PXI interface.

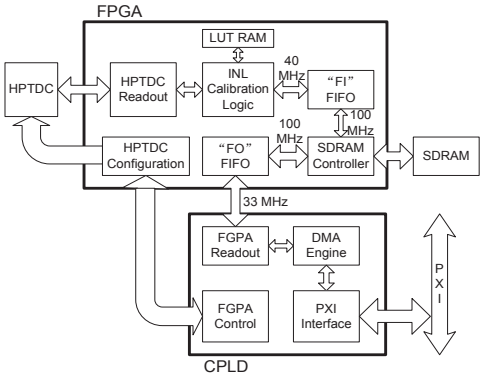


Fig. 7. Diagram of Logic design.

The HPTDC chip exhibits non-linearity which is caused by non-ideal topology, non-uniform parasitic reactance, spread of the device parameters and the 40 MHz clock crosstalk from the logic part to the time measurement part. When the HPTDC works in the high resolution mode, the INL deteriorates the resolution of the time measurement. In this system, a real time INL correction method based on the Look-Up Table (LUT) was developed [11]. The principle of INL compensation is that a sample falling in a certain bin of the TDC is corrected by subtracting the INL value of that bin.

To determine the non-linearity, the "code density test" [12] is adopted: The histogram or output code density is the number of times every individual code has occurred. After a sufficiently large number of signals are acquired, the DNL and INL will be measured.

If the TDC output code of the measured sample is C(i)TDC, and the INL(i) of this code is known, then the ideal value of the sample will be denoted by:

$$C(i)IDEAL = C(i)TDC - INL(i) \quad (1)$$

Because the INL is periodic over every HPTDC clock period corresponding to a repeating pattern of every 256 bins, a LUT of 256 depths is employed.

The corrected data is then buffered and transferred to the CPLD. Considering the time cost of the PXI transfer protocol, a SDRAM chip (MT48LC4M32B2) is used to guarantee no data loss during this process. This SDRAM works with a 100 MHz clock; therefore, two FIFOs ('FI' and 'FO') are used as the bridges between the SDRAM control logic and the 40 MHz/33 MHz data streams.

The 'FI' and 'FO' FIFO are both 4096 deep with a 32 bit width. As shown in Fig. 8, the 'FI' FIFO imports the data from the INL calibration logic, which is synchronized with the 40 MHz clock. When the read-used-word of the 'FI' FIFO is more than 256 words, the SDRAM control logic starts to read data from the 'FI' FIFO and transfer it to the external SDRAM. When the SDRAM stores more than 256 words and the write-used-word of the 'FO' FIFO is less than 3700, the SDRAM control logic begins to write the data to the 'FO' FIFO with a 100 MHz clock. Then the 'FO' FIFO is read by the CPLD with a 33 MHz clock.

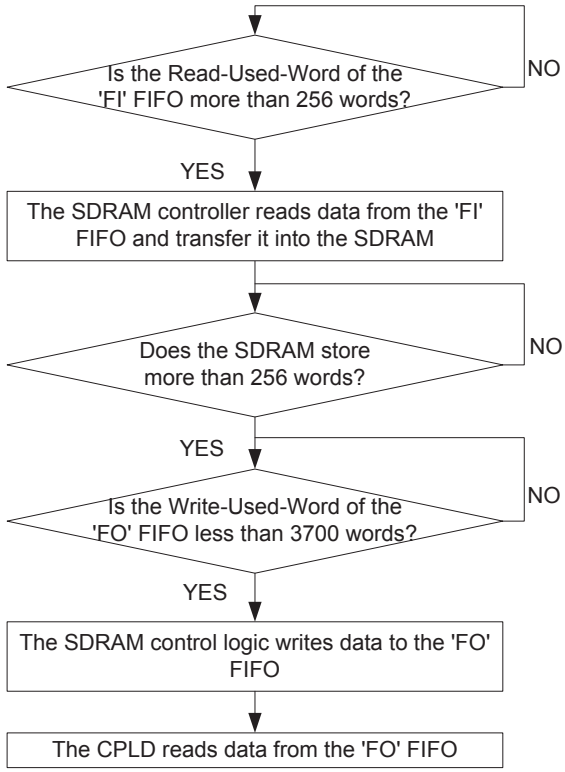


Fig. 8. State Machine of data buffer.

The CPLD functions as the interface between the FPGA and the PXI bus. To achieve a high transfer speed, the DMA (Direct Memory Access) method is adopted. With the use of the PCI core pci_mt32[13] provided by the Altera Company, a DMA engine is implemented for burst transfer. In fact, there exists time cost in the interval of adjacent DMA transfer process; therefore, with different DMA transfer length, the average transfer speed varies. We have conducted tests on this issue, which will be presented later.

5. FPGA On-line configuration

Two FPGA configuration modes are employed in this system - JTAG mode and PS (passive serial) mode. JTAG mode is used in FPGA logic debugging, while the PS mode is used in normal operation.

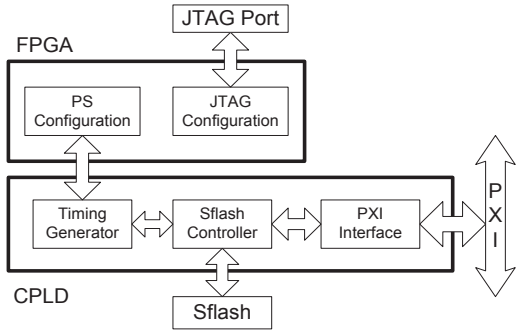


Fig. 9. Configuration of the FPGA.

To enhance the flexibility of the system design, the on-line modification of the FPGA logic is considered. As shown in Fig. 9, the CPLD controls the transfer of the configuration data from a storage device (a Sflash memory) to the FPGA. In the on-line modification process, the Sflash Controller section erases the Sflash and reads new configuration data from the PXI bus, and then the Timing Generator section generates the necessary timing to read data from the Sflash and configure the FPGA.

6. Test results

The performance of this time measurement module was evaluated both in the laboratory and commissioning tests.

6.1. Laboratory test results

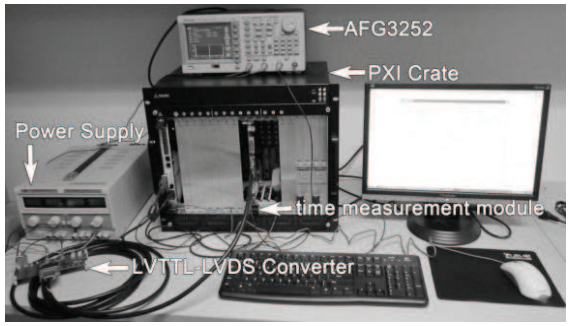


Fig. 10. System under test.

Fig. 10 shows the system under test. The pulse signals from the signal generator AFG3252 pass through the LVTTL-LVDS Converter board, and then are imported to this time measurement module. The output data from the system is transferred to the remote PC for further analysis.

6.1.1. Nonlinearity tests

The nonlinearity tests include DNL (Differential Nonlinearity) and INL tests based on the "code density test" technique mentioned above.

a) The DNL (LSB) b) The INL (LSB)

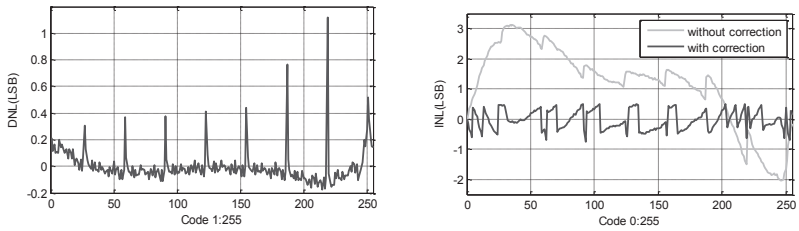


Fig. 11. Nonlinearity test results.

Fig.11. shows the typical test results. As shown in Fig. 11b), the INL nonlinearity test results are improved significantly after the correction process. The enhancement of the INL parameters has a direct influence on the system time resolution, which will be presented as follows.

6.1.2. Time resolution test

A "cable delay test" technique is conducted in this test. The signal generator generates two output signals with a fixed time delay. With a large enough recorded data number, a precise RMS value of the time delay can be obtained. Supposing that the time test results of the two signals are not interrelated, the single channel time resolution can be approximately calculated by dividing the RMS by $2^{1/2}$.

a)Without INL correction b) With INL correction

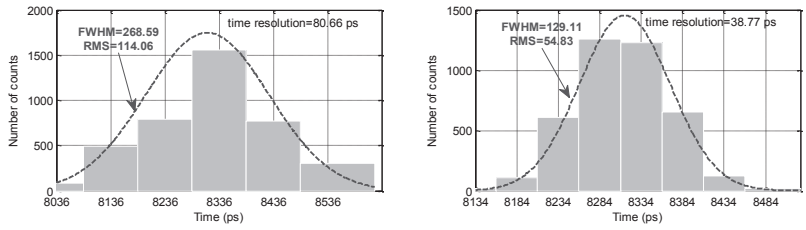


Fig. 12. Time resolution results with a -8 ns delay.

Fig. 12 shows the time resolution with a -8 ns delay, the time resolution is around 80 ps and enhanced to 38 ps with INL correction. The FWHM (Full Width at Half Maximum) decreases obviously with INL correction.

By tuning the delay of the two channels, we can obtain a series of time resolution test results. As shown in Fig. 13, in the delay range from -53 ns to 2 ns, the time resolution is better than 90 ps and further improved to 40 ps with INL correction. Since the HPTDC works with a clock frequency of 40 MHz, the time resolution exhibits a period pattern of 25 ns, which was confirmed in tests.

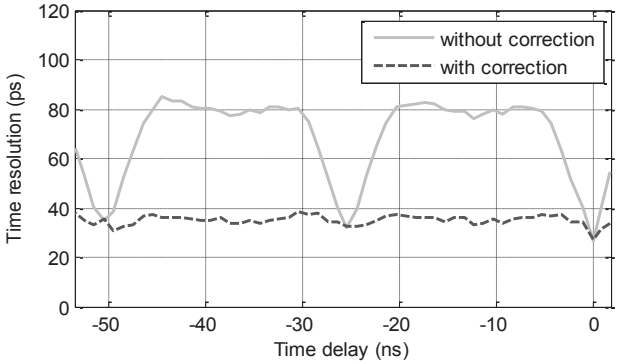


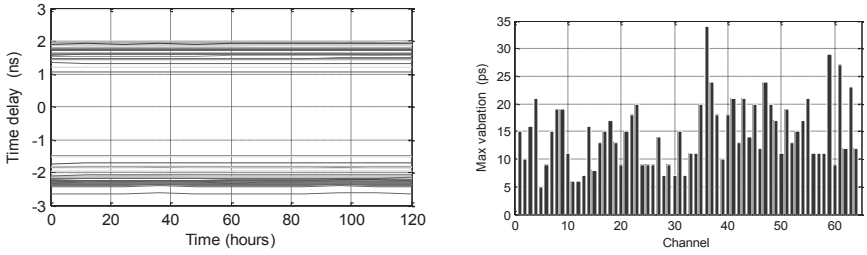
Fig. 13. Time resolution test results with different time delays.

6.1.3. Long-term stability test

We have also conducted long-term stability tests as long as 120 hours. The data was acquired every 12 hours, with the results shown in Fig. 14. As shown in Fig.14a), the time delay test results are quite stable, with a maximum fluctuation of 34 ps. The time resolution of all channels also stays constant, and the maximum vibration is 3.3 ps.

a) Time delay at different test time,

b) Max fluctuation of time delay,



c) Time resolution at different test time,

d) Max fluctuation of time resolution.

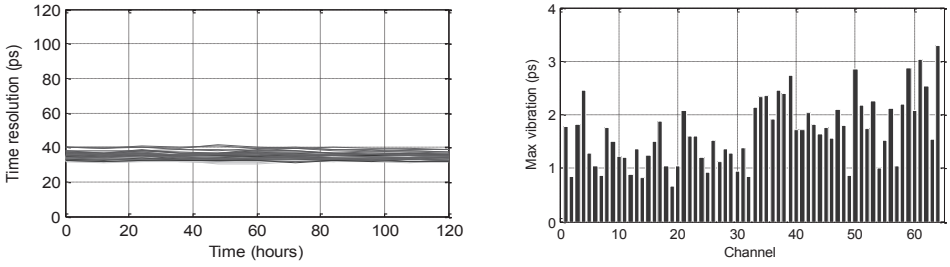


Fig. 14. Results of long term stability test.

6.1.4. Data transfer speed test

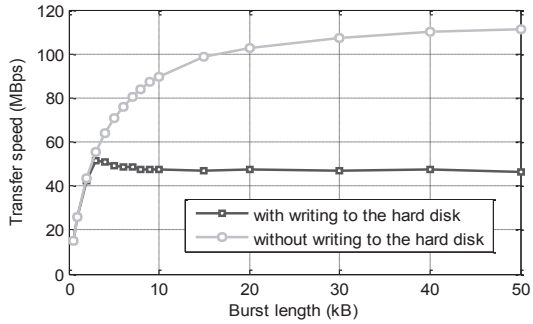


Fig. 15. Data transfer speed test results with different DMA burst lengths.

As discussed above, the average transfer speed varies with different burst lengths. As shown in Fig. 15, without writing to the hard disk, the transfer speed increases with bigger burst lengths and a maximum speed around 110 MBps is achieved; considering the time cost of writing to the hard disk, the transfer speed increases to a peak value of 50 MBps with a 4 kByte burst length, which is probably due to the limit caused by the communication between the hard disk and the CPU of the PC. The test results indicate that an overall transfer speed better than 40 MBps is achieved, which is beyond the requirement.

6.2. Commissioning test

Tests were also conducted on this time measurement module together with the SFE16 front end module and the MWDC detector.

6.2.1. Test with the SFE16 front end module

Two channel signals generated by the signal source AFG3252 are first imported to the SFE16 front end module, in which the signals are processed based on the TOT method.With this time measurement module, the time information is obtained by measuring the leading edge of the output pulse signal from the SFE16 module, while the charge information can be calculated with the trailing time.

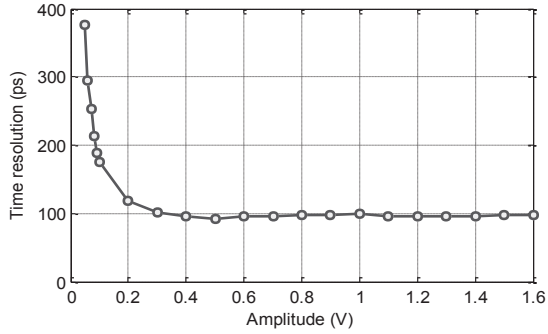


Fig. 16. Time resolution with different amplitude.

Fig.16 shows the time resolution result in the input amplitude range from 50 mV to 1.65 V. Compared with the resolution of the time measurement module itself, the deterioration is due

to the SFE16 module which outputs a signal with a long rise time. The overall time resolution is better than 400 ps, which satisfies the requirement of the experiment.

a) Relationship of the TOT width and the input charge b) Charge measurement resolution

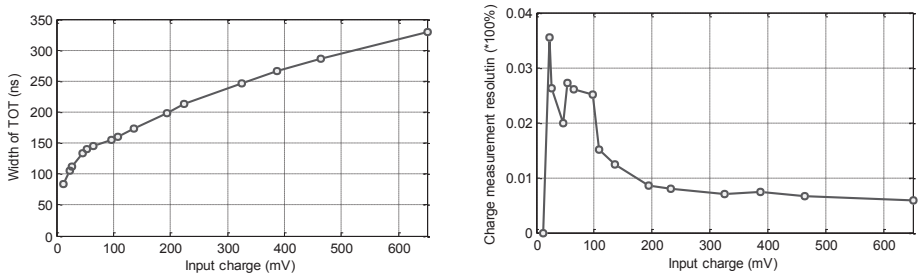


Fig. 17. Results of the charge measurement test.

Fig.17a) shows the tested pulse widths with different input charges. Fig.17b) shows the charge measurement resolution which is better than 4%, also beyond the application requirement.

6.2.2. Test with the MWDC

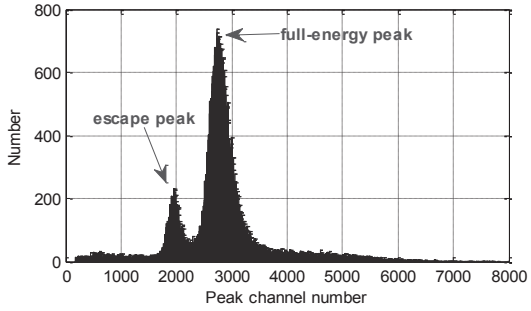


Fig. 18. Histogram of pulse distribution.

Fig. 18 shows the commissioning test results with the Fe55 used as the radiation source of the MWDC. Two peaks can be observed and the higher peak corresponds to the full-energy peak of the X-ray of Fe55 with energy of 5.9 keV, while the lower one is the escape peak of Ar with an energy of 3 keV. There exists a relationship that the energy of the full-energy peak is about twice that of the escape peak. The peak channel number of the full-energy peak is at Bin 2740 (268.5 ns), and the charge can be calculated to be around 400 fC. With the same calculation process, the charge of the escape peak is around 200 fC, which agrees well with the expected relationship between these two peaks.

7. Conclusion

A 128 channel high density measurement module was designed for the MWDC readout in the external target experiment of HIRFL-CSR. According to the test results, an overall time resolution of better than 50 ps is achieved, with a data transfer rate around 40 MBps, which is beyond the application requirement. This measurement module has also been proven to function well in the long-term stability tests as well as in the commissioning tests.

Acknowledgements

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