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A novel quasi-resonant ZVS boost converter with tapped inductor

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Abstract. The purpose of this paper is to propose a model of a novel quasi-resonant boost converter with a tapped inductor. This converter combines the advantages of zero voltage quasi-resonant techniques and different conduction modes with the possibility of obtaining a high voltage conversion ratio by using a tapped inductor, which results in high converter efficiency and soft switching in the whole output power range. The paper contains an analysis of converter operation, a determination of voltage conversion ratio and the maximum voltage across power semiconductor switches as well as a discussion of control methods in discontinuous, critical, and continuous conduction modes. In order to verify the novelty of the proposed converter, a laboratory prototype of 300 W power was built. The highest efficiency $\eta = 94.7\%$ was measured with the output power $P_o = 260$ W and the input voltage $V_{in} = 50$ V. The lowest efficiency of 90.7% was obtained for the input voltage $V_{in} = 30$ V and the output power $P_o = 75$ W. The model was tested at input voltages (30–50) V, output voltage 380 V and maximum switching frequency 100 kHz.

Key words: tapped inductor; boost converter; DC/DC converter; zero voltage switching.

1. Introduction

Switched-mode power supplies (SMPSs) are widely used in industrial, medical, residential, and aerospace environments. Moreover, an interest in DC-DC converters, especially voltage boosting techniques, is constantly growing [1]. Modern SMPSs nowadays are dominated by a trend to achieve high efficiency, high power density and in many cases, they use a DC-DC converter with a high voltage conversion ratio. This is due to the fact that the full utilization of renewable sources requires a converting stage to match the demanded voltage for effective grid connection. One option to reduce the size of storage energy elements is to increase the converter switching frequency. However, in hard switching converters the increase in the switching frequency results in increased switching losses. The use of soft switching techniques reduces switching losses, increases efficiency, and reduces EMI.

Compared to conventional PWM converters, the converters with tapped-inductor configurations permit the duty cycle to be adjusted to the values which are neither close to 0 nor 1. Furthermore, a better utilization of switching and passive components can be achieved. The coupled inductor techniques provide solutions to achieve a high voltage conversion ratio, a low voltage stress on the active switch, and high efficiency without the penalty of high duty ratio [2–4]. Furthermore, utilizing a coupled inductor to boost the voltage makes leakage inductance reduce recovery problem by limits di/dt of the output diode. Simultaneously, in a boost converter with a coupled inductor when the transistor is turned off, leakage inductance leads to voltage spikes across the switches [5], which increases energy losses and EMI. In such topologies clamp circuits are required.

To solve the problem of increasing switching losses as the frequency increases, soft switching techniques should be used. The zero-voltage switching (ZVS), and the zero-current switching (ZCS) techniques are two commonly used soft switching methods. By adopting these techniques, either the voltage or the current is zero during the switching transitions, which largely reduces the switching losses and also increases the reliability of power supplies.

Quasi-resonant converters (QRCs) were introduced in [6–8] to overcome the disadvantage of PWM converters operating at a high switching frequency. In QRCs, switches can be turned on at a zero voltage or turned off at a zero current so that the switching losses are zero and the switching frequency could be high. However, the switches in QRCs have to withstand the high voltage or the current stress. These techniques are used in low power applications.

In active clamp flyback converters, the leakage energy is recovered, and voltage ratings of semiconductors are reduced [9, 10]. In those converters, the soft-switching technique could be used with leakage inductance or an additional inductor. However, the implementation of this technique reduces the effective duty cycle; hence, a coupled inductor with higher turns ratio is required.

High efficiency and soft switching are achieved in zero voltage/current transition [11, 12] and resonant switched capacitor [13] techniques. However, in such a circuit the converter is complex and needs additional components.

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The article proposes a new type of quasi-resonant ZVS boost converter with a tapped inductor and an active-edge resonant cell (AERC), which develops the family of novel topologies described in [8, 14, 15].

2. Two-Transistor Tapped-Inductor ZVS Quasi-Resonant Boost Converter

Figure 1 shows a single switch quasi-resonant converter with a tapped inductor [8]. In this circuit, the transistor is soft switched over a narrow range of output power. The maximum output power is limited by the output resistance, which increases the voltage V_{DS} across the transistor T.

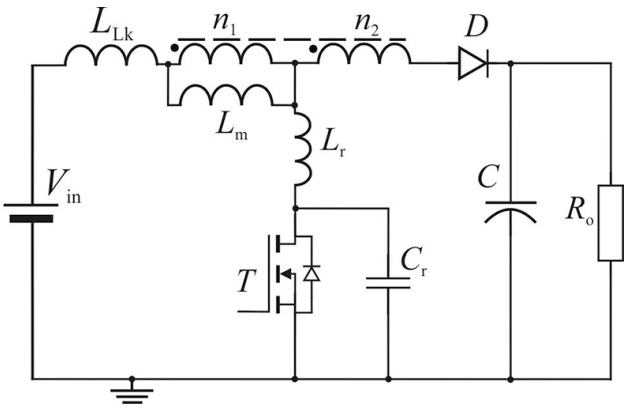

Fig. 1. Simplified converter scheme presented in [8]

In order to improve the technical parameters, a two-transistor tapped-inductor ZVS-AERC boost converter is proposed, shown in Fig. 2. The addition of the transistor T_2 enables us to achieve higher efficiency and soft switching in a wider range of output power. Tapped inductors provide a high voltage ratio and high efficiency. The two windings, n_1 and n_2, of the tapped inductor are on the same core and magnetically coupled. Tapping the inductor is beneficial because it optimizes the duty cycle of the converter to achieve the maximum efficiency.

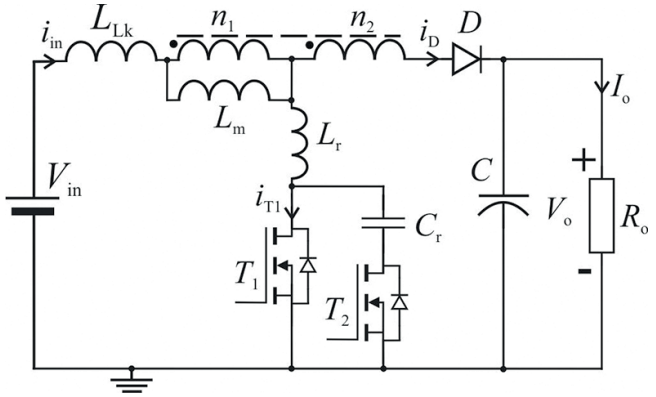

Fig. 2. Simplified circuit scheme of the proposed converter

Tapping the inductor also allows for reducing voltage and current ratings of semiconductors power elements. The leakage inductance L_{Lk} of the coupled inductor with the resonant inductance L_r form equivalent inductance of the resonant circuit L_{eq} described by the equation:

$$L_{eq} = L_r + L_{Lk}\left(\frac{N}{N+1}\right)^2, \tag{1}$$

where $N = n_2/n_1$ is the turns ratio of the tapped inductor; n_1 is the turns of primary winding and n_2 is the turns of secondary winding.

The equivalent inductance L_{eq} together with the capacitor C_r forms a resonant circuit. The resonant circuit can be implemented without an additional resonant inductor, which is the main advantage compared to the circuit presented in [14]. Additionally, in the ZVS converter reverse recovery problems caused by transistors body diodes are reduced.

In the presented converter, the transistors are controlled with a variable frequency and a constant value of the current, at which the transistor T_1 is turned off, thus making the maximum voltage values on the switches independent of load changes. This facilitates the use of transistors with a lower resistance $R_{DS(on)}$, which reduces conduction losses and increases efficiency. The losses in the transistor T_2 are much lower than in the transistor T_1 due to the short conduction time of switch T_2. Moreover, as a result of lowering the relative frequency f_s/f_r, the capacitor rms current and the equivalent inductance were reduced.

The additional transistor T_2, connected in a series with the capacitor C_r, initiates a soft switching (ZVS) of the transistor T_1. Turning on the T_2 transistor enables parallel to the transistor T_1 discharged resonant capacitor C_r and allows us to turn off the transistor T_1 at zero voltage.

In CCM, the transistor T_1 is turned on at zero current and turned off at zero voltage, in DCM both transistors are switched at zero voltage. The voltage conversion ratio k_v is determined by the duty cycle D of the transistor T_1. The resonant operation of the converter facilitates the elimination of the negative impact of leakage inductance on voltage spikes, efficiency, and EMI emission.

In order to explain the principle of operation of this converter, it is analyzed in steady-state and different conduction modes: the critical conduction mode (CRM), the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM).

Experimental results and waveforms at 300 W illustrate the performances of the proposed Two-Transistor Tapped-Inductor ZVS-AERC Boost Converter.

3. Principle of operation

Key waveforms are shown in Fig. 3. The circuit operation can be divided into six modes (intervals), whose equivalent circuits are shown in Fig. 4. They are described as follows:

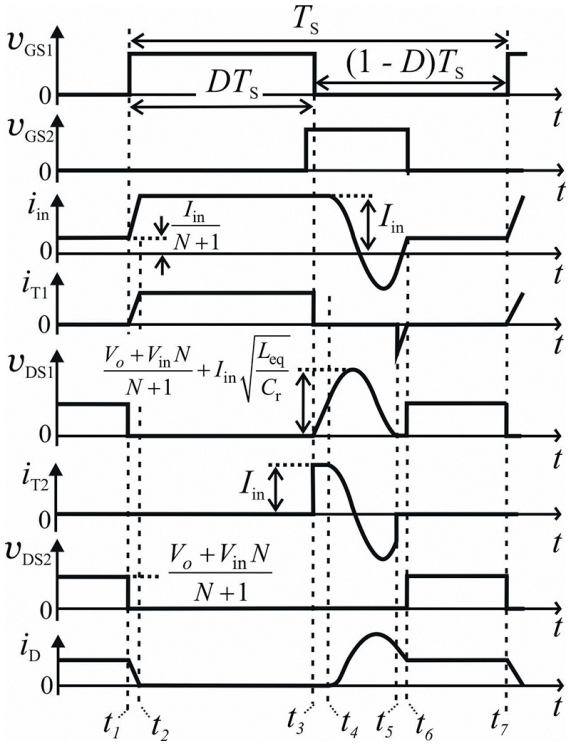

Fig. 3. Key waveforms of the proposed converter

Interval 1 ($t_1 - t_2$) Fig. 4a. Before this interval, the switches T_1, T_2 are off, the output diode D is forward biased. The energy from source V_{in} and the energy accumulated in the tapped inductor are transferred to the load. At t_1 the transistor T_1 is turned on – the transistor current increases and the output diode D current decreases. The transistor current i_{T1} increases linearly; the slope of that current is limited by the equivalent inductance L_{eq}. This facilitates turning on the transistor at zero current and reducing the reverse recovery current of the output diode. In this mode the voltage on equivalent inductance is given by:

$$v_{eq}(t - t_1) = \frac{V_o + NV_{in}}{N+1}. \tag{2}$$

The interval $t_1 - t_2$ can be defined as:

$$t_2 - t_1 = \frac{L_{eq} I_{in}(N+1)}{V_o + NV_{in}}. \tag{3}$$

Interval 2 ($t_2 - t_3$) Fig. 4b. In this interval the transistor T_1 remains switched on, and the diode D is reverse biased. The energy from the voltage source V_{in} is accumulated in the tapped inductor. In this interval, the transistor T_2 is switched on at zero current and zero voltage. This interval is given by:

$$t_3 - t_2 = DT_s - (t_2 - t_1), \tag{4}$$

where D is the duty cycle of the transistor T_1.

Interval 3 ($t_3 - t_4$) Fig. 4c. At t_3 the transistor T_1 is turned off at zero voltage. In this interval, the capacitor C_r is charged with a constant current I_{in} to the level at which the diode D is forward biased. The voltage on capacitor C_r and the interval $t_3 - t_4$ can be described by the following equations:

$$v_{Cr}(t_4) = \frac{V_o + NV_{in}}{N+1}, \tag{5}$$

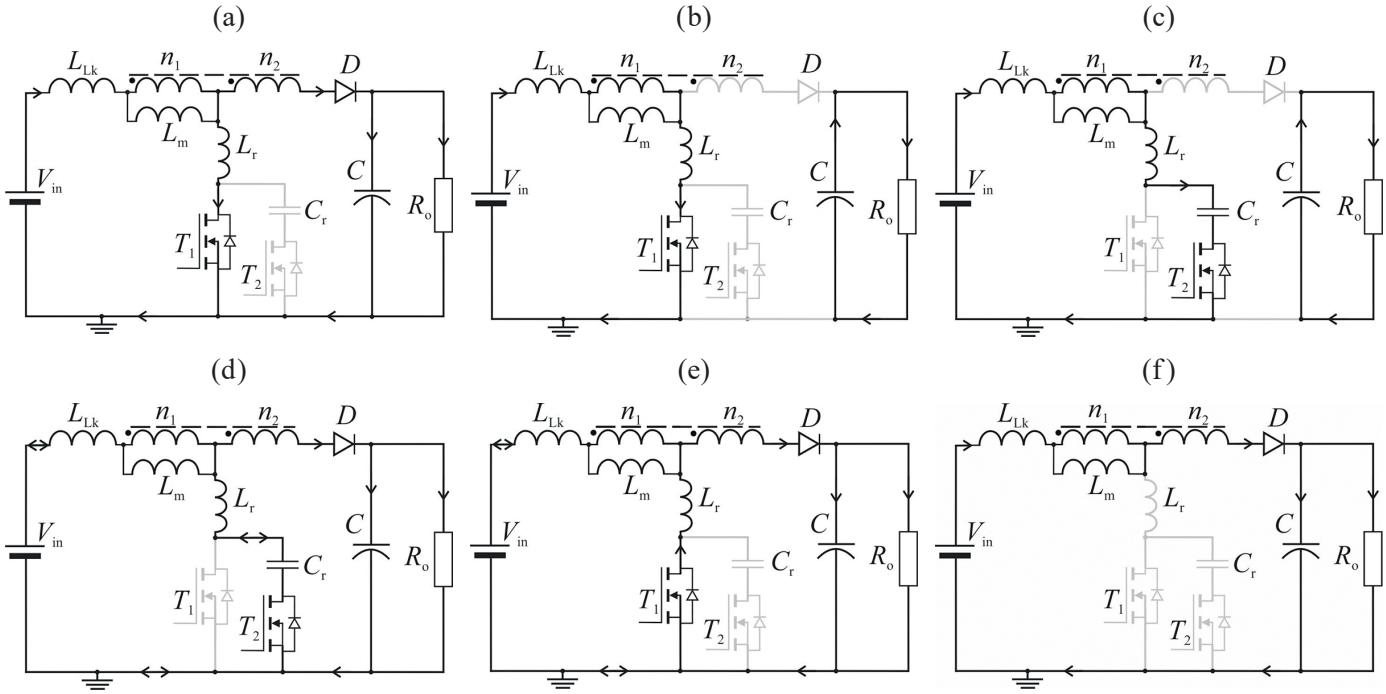

Fig. 4. Equivalent diagrams of the converter in six characteristic intervals

$$t_4 - t_3 = \frac{C_r \upsilon_{Cr}(t_4)}{I_{in}} = \frac{C_r(V_o + NV_{in})}{I_{in}(N+1)}. \quad (6)$$

Interval 4 ($t_4 - t_5$) Fig. 4d. In this interval inductance L_{eq} and capacitor C_r resonate. The principal equations describing voltages and currents in this interval can be defined as follows:

$$i_{Cr}(t - t_4) = i_{Lr}(t - t_4) = I_{in}\cos\left[\omega_r(t - t_4)\right], \quad (7)$$

$$i_D(t - t_4) = \frac{I_{in}}{N+1}\left\{1 - \cos\left[\omega_r(t - t_4)\right]\right\}, \quad (8)$$

$$i_{in}(t - t_4) = \frac{I_{in}\left\{N\cos\left[\omega_r(t - t_4)\right] + 1\right\}}{N+1}, \quad (9)$$

$$\psi = \frac{\upsilon_{Cr}(t_4)}{I_{in}Z} = \frac{V_o + NV_{in}}{I_{in}Z(N+1)}, \quad (10)$$

$$t_5 - t_4 = \frac{\pi + \arcsin(\psi)}{I_{in}(N+1)}, \quad (11)$$

where Ψ specifies the soft switching condition; $Z = (L_{eq}/C_r)^{1/2}$; $\omega_r = 1/(L_{eq}C_r)^{1/2}$.

To achieve the soft switching of transistors the following inequality must be satisfied:

$$\frac{V_o + NV_{in}}{N+1} \le I_{in}Z \Rightarrow \psi \le 1. \quad (12)$$

Interval 5 ($t_5 - t_6$) Fig. 4e. In this interval the body diode of the transistor T_1 is conducting. The negative current i_{T1} of the transistor T_1 increases to zero. The output diode current i_D decreases, and the input current i_{in} increases to the same value $I_{in}/(N+1)$. The capacitor C_r remains discharged, allowing the transistor T_2 to turn off at zero voltage. The inductor current at t_5 may be described by the following equation:

$$i_{Lr}(t_5) = -I_{in}\sqrt{1 - \psi^2}. \quad (13)$$

The duration of this interval depends on current $i_{Lr}(t_5)$ equivalent inductance and constant voltage on that inductance during the analyzed interval:

$$t_6 - t_5 = \frac{L_{eq}i_{Lr}(t_5)}{\upsilon_{Cr}(t_4)} = \frac{L_{eq}(N+1)I_{in}\sqrt{1 - \psi^2}}{V_o + NV_{in}}. \quad (14)$$

Considering Eqs. (7–11), the diode current and the input current at t_5 are given by:

$$i_D(t_5) = \frac{I_{in}\left(1 + \sqrt{1 - \psi^2}\right)}{N+1}, \quad (15)$$

$$i_{in}(t_5) = \frac{I_{in}\left(1 - N\sqrt{1 - \psi^2}\right)}{N+1}. \quad (16)$$

Interval 6 ($t_6 - t_7$) Fig. 4f. In this interval, both transistors are turned off, and the diode D is forward biased. The energy from the voltage source V_{in} and the tapped inductor is transferred to the load. The duration of the interval depends on the transistor T_1 turn-off time according to the equation:

$$t_7 - t_6 = T_s(1 - D) - (t_4 - t_3) - (t_5 - t_4) - (t_6 - t_5), \quad (17)$$

where $T_s(1 - D)$ is the transistor T_1 turn-off time.

4. Voltage conversion ratio

The voltage conversion ratio was determined by comparing the converter input power with the output power:

$$V_{in}I_{in(av)} = V_oI_o,\ k_u = \frac{V_o}{V_i} \Rightarrow k_u = \frac{I_{in(av)}}{I_o}. \quad (18)$$

The average input current was determined on the basis of Eqs. (1–18) and described by the following equation:

$$I_{in(av)} = \frac{1}{T_S}\left(\begin{array}{l} I_{in}\left(T_sD - \dfrac{N}{2(N+1)}(t_2 - t_1) + (t_4 - t_3)\right) + \\ + \dfrac{I_{in}}{N+1}\left(\displaystyle\int_{t_4}^{t_5}\left(N\cos(\omega_r t) + 1\right)dt\right) + \\ + \dfrac{i_{in}(t_5)(t_6 - t_5)}{2} + \dfrac{I_{in}}{N+1}(t_7 - t_6) \end{array}\right), \quad (19)$$

$$I_{in(av)} = I_{in}\left(\frac{DN+1}{N+1} - \frac{N(2 - \psi^2)}{4\pi\psi(N+1)}\frac{f_s}{f_r}\right). \quad (20)$$

The output current I_o is equal to the average current of the diode D, according to the following equations:

$$I_o = \left(\begin{array}{l} \dfrac{I_{in}}{N+1}\displaystyle\int_{t_4}^{t_5}\left(1 - \cos(\omega_r t)\right)dt + \\ + \left(i_D(t_5) + \dfrac{I_{in}}{N+1}\right)\dfrac{(t_6 - t_5)}{2} + \\ + I_{in}\dfrac{(t_7 - t_6) + (t_2 - t_1)/2}{N+1} \end{array}\right)\frac{1}{T_S}, \quad (21)$$

$$I_o = \frac{I_{in}\left(1 - D + \dfrac{2 - \psi^2}{4\pi\psi}\dfrac{f_s}{f_r}\right)}{N+1}. \quad (22)$$

With regard to Eqs. (18–22), the voltage conversion ratio is given by:

$$k_\upsilon = \frac{ND + 1 - N\dfrac{2 - \psi^2}{4\pi\psi}\dfrac{f_s}{f_r}}{1 - D + \dfrac{2 - \psi^2}{4\pi\psi}\dfrac{f_s}{f_r}} \approx \frac{ND + 1}{1 - D}. \quad (23)$$

5. Control and analysis of converter operating modes

Usually, in resonant converter soft switching region and voltage ratings of semiconductors depend on output resistance and characteristic impedance. In the proposed converter utilization different control methods depending on output resistance facilitate obtaining soft switching in a wide power range and constant voltages on switches.

This section presents a discussion on the control method of the converter in three conduction modes. If the resonant frequency f_r is significantly higher than the control frequency f_s, it may be assumed that $i_{in}(t_3) = i_{in}(t_4) = i_{in}(t_5) + Ni_D(t_5) = I_{in(max)}$. The idea behind the proposed control method relies on turning off the main transistor T_1 at a constant current described by the following equation:

$$I_{in(max)} = \frac{V_o + NV_{in}}{Z(N+1)} \Rightarrow \psi = 1, \tag{24}$$

which ensures a constant voltage on the capacitor C_r (constant voltage on v_{DS1}), independent of output resistance.

5.1. Critical conduction mode. The critical conduction mode occurs when the main transistor T_1 turns on and the tapped inductor current reaches zero. The maximum current of the transistor in that mode can be given by:

$$I_{in(CRM)} = \frac{(V_o - V_{in})(1-D)T_s}{L_m(N+1)}, \tag{25}$$

In that mode the transistors are switched with a fixed frequency described by:

$$f_{s(CRM)} = \frac{R_o(k_\upsilon - 1)}{2L_m k_\upsilon (N+k_\upsilon)^2}. \tag{26}$$

On the basis on Eq. (24), in order to ensure the soft switching of transistors, the value of characteristic impedance should be in accordance with the equation:

$$Z = \frac{R_o}{2k_\upsilon(N+1)}. \tag{27}$$

5.2. Continuous conduction mode. In this mode, the transistors are switched at a frequency higher than the frequency described by Eq. (26). The maximum input current in this mode can be given by:

$$I_{in(CCM)} = \frac{I_o(N+1)}{1-D} + \frac{(V_o - V_{in})(1-D)T_s}{2L_m(N+1)}. \tag{28}$$

Assuming that $i_{in}(t_3) = i_{in}(t_4) = i_{in}(t_5) + Ni_D(t_5) = I_{in(CCM)}$, and using Eq. (24), the operating frequency of the analyzed converter in CCM is given by:

$$f_{s(CCM)} = \frac{R_o Z(N+1)(k_\upsilon - 1)}{2L_m(N+k_\upsilon)^2\left[R_o - k_\upsilon Z(N+1)\right]}. \tag{29}$$

In order to ensure the soft switching of transistors, the value of characteristic impedance is given by:

$$Z \le \frac{2L_m R_o f_s (N+k_\upsilon)^2}{(N+1)\left[2L_m f_s k_\upsilon (N+k_\upsilon)^2 + R_o(k_\upsilon - 1)\right]}. \tag{30}$$

5.3. Discontinuous conduction mode. In the discontinuous conduction mode, the transistors are switched at a frequency lower than the frequency described by Eq. (26). Unlike CRM and CCM, the voltage conversion ratio is not described by Eq. (23). To calculate it, the input power was compared with the output power of the converter in accordance with the following equations:

$$I_{in(av)} = \frac{1}{T_S}\frac{V_{in}DT_S}{2L_m} + I_o, \tag{31}$$

$$P_{in} = V_{in}\left(\frac{DV_{in}}{2L_m} + I_o\right), \tag{32}$$

$$P_o = V_o I_o, \tag{33}$$

$$k_\upsilon = \sqrt{\frac{D^2 R_o}{2L_m f_s} + \frac{1}{4}} + \frac{1}{2}. \tag{34}$$

In CRM, the soft switching of transistors can be achieved by maintaining the minimum turn on time of the transistor T_1, as follows:

$$DT_s \ge \frac{L_m I_{in(DCM)}}{V_{in}}. \tag{35}$$

On the basis on Eqs. (24) and (35) the switching frequency may be described by:

$$f_{s(DCM)} = \frac{2Z^2 k_\upsilon (N+1)^2 (k_\upsilon - 1)}{L_m R_o (N+k_\upsilon)^2}. \tag{36}$$

In CCM, during switching on the transistor T_1 the slope of the currents change in the transistor and the output diode are limited by the equivalent inductance. In DCM, the transistor is switched on when the D diode is not conducting, and this completely eliminates the diode reverse recovery problem. Moreover, in this mode the transistor T_1 may be turned on at zero voltage. After the current in magnetizing inductance reaches zero, the output capacitance of transistors and magnetizing inductance resonate. The sinusoidal voltage V_{DS1} enables us to turn on the transistor T_1 at a voltage much lower than the input voltage (Fig. 5).

To obtain the minimum V_{DS} voltage on transistor T_1, it should be switched with certain frequency and duty cycle

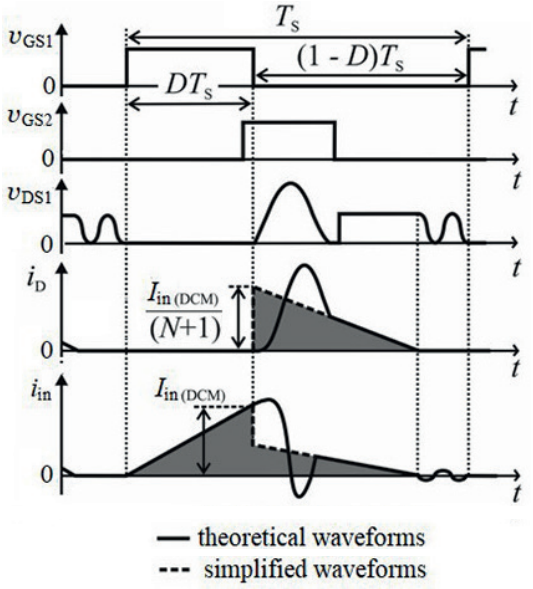

Fig. 5. Theoretical and simplified waveforms of voltages and currents in DCM

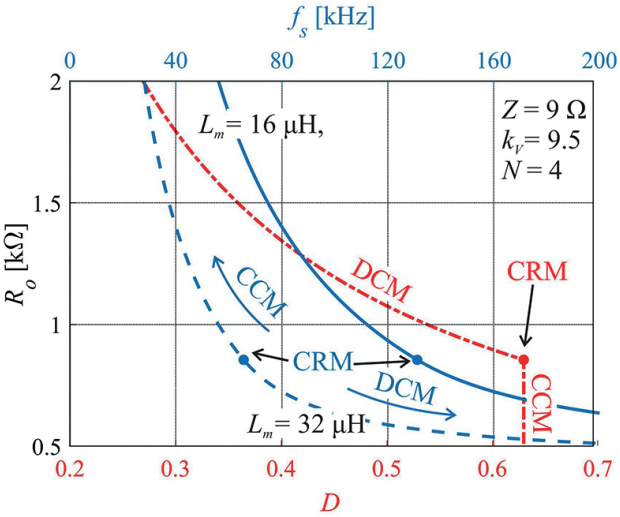

Fig. 7. Load resistance R_o as a function of switching frequency and duty cycle for $\psi = 1$

where $\psi = 1$ (Eq. (24)). Voltage conversion ratio as a function of switching frequency f_s and duty cycle D for three different turn ratio n and $\psi = 1$ with marked different conduction mode is presented on Fig. 6. In the converter, ψ may be less than one, which increases the maximum V_{DS1} voltage. In this case switching frequency is lower than the frequency on Fig. 6. Figure 7 shows output resistance as a function of switching frequency and duty cycle for two different magnetizing inductance L_m. Duty cycle curve is independent of the magnetizing inductance. In based on the characteristics presented on Fig. 7, it can be observed that the switching frequency depends on output resistance and magnetizing inductance.

In DCM duty cycle increases with increasing frequency (Eq. (34)), in CCM duty cycle is constant (Eq. (23)). A slight increase the output power in CCM forces a high frequency increase. Theoretical maximum output power of the converter is doubled than the output power in CRM mode (for $\psi = 1$).

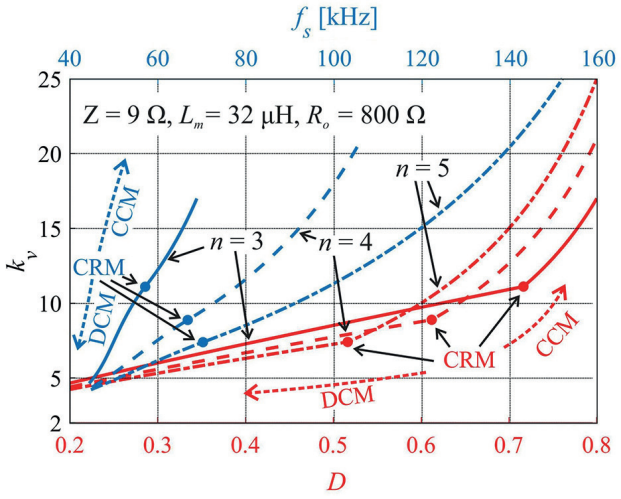

Fig. 6. Voltage conversion ratio as a function of switching frequency and duty cycle of the proposed converter for $\psi = 1$

6. Voltage and current stress of power devices

The maximum voltage v_{DS1} on transistor T_1 occurs in the interval $t_4 - t_5$. Assuming that the transistor is switched at a frequency determined by Eq. (24), the maximum voltage is given by:

$$V_{DS1(max)} = \frac{2(V_o + NV_{in})}{N+1}. \tag{37}$$

The maximum voltage v_{DS2} on the transistor T_2 occurs in the interval $t_6 - t_7$ and is determined by:

$$V_{DS2(max)} = \frac{V_o + NV_{in}}{N+1}. \tag{38}$$

Similarly, the maximum voltage across the diode D occurs in the same interval, and it can be calculated in accordance with the following equation:

$$V_{D(max)} = V_o + NV_{in}. \tag{39}$$

In order to calculate current stress of the converter components, a constant current in magnetizing inductance in interval $(t_3 - t_6)$, and fixed duration of intervals $(t_4 - t_3) = 1/\omega_r$, $(t_5 - t_4) = 3/(4f_r)$ were assumed. Derivations include the effect of current ripple in magnetizing inductance in intervals $(t_2 - t_3)$ and $(t_6 - t_7)$. Interval $(t_1 - t_2)$ was omitted. Parameter A (44) was defined to simplified RMS current descriptions. RMS currents were calculated for DCM and CCM accordance with Eqs. (40–48).

$$I_{\mathrm{D(RMS,\,CCM)}} = \frac{I_\mathrm{o}}{N+1}\sqrt{\left(\left[N+k_v\right]^2+\frac{A^2}{3}\right)\left(\frac{N+1}{N+k_v}-\frac{f_\mathrm{s}}{f_\mathrm{r}}\frac{3\pi+2}{4\pi}\right)+\frac{f_\mathrm{s}}{f_\mathrm{r}}\left(A+N+k_v\right)^2\left(\frac{1}{\pi}+\frac{9}{8}\right)}, \tag{40}$$

$$I_{\mathrm{in(RMS,\,CCM)}} = \frac{I_\mathrm{o}}{N+1}\sqrt{\left(\left[N+k_v\right]^2+\frac{A^2}{3}\right)\left(\frac{\left[N+1\right]^2\left[k_v-1\right]+N+1}{N+k_v}-\frac{f_\mathrm{s}}{f_\mathrm{r}}\frac{3\pi+2}{4\pi}\right)+\frac{f_\mathrm{s}}{f_\mathrm{r}}\left(A+N+k_v\right)^2\left(\frac{N^2+1}{2\pi}+\frac{3N^2}{4}+\frac{3}{4}\right)}, \tag{41}$$

$$I_{\mathrm{D(RMS,\,DCM)}} = \frac{I_\mathrm{o}}{N+1}\sqrt{\frac{R_o(k_v-1)}{L_m k_v}\left(\frac{2\sqrt{2}\left[N+1\right]}{3}\sqrt{\frac{L_\mathrm{m}k_v}{R_\mathrm{o}f_\mathrm{s}(k_v-1)}}+\frac{1}{f_\mathrm{r}}\left[\frac{5}{3\pi}+\frac{7}{4}\right]\right)}, \tag{42}$$

$$I_{\mathrm{in(RMS,\,DCM)}} = \frac{I_\mathrm{o}}{N+1}\sqrt{\frac{R_\mathrm{o}(k_v-1)}{L_\mathrm{m}k_v}\left(\frac{2}{3}\left[\frac{1}{\{N+1\}\{k_v-1\}}+1\right]\sqrt{\frac{2L_\mathrm{m}k_v(k_v-1)}{R_\mathrm{o}f_\mathrm{s}}}\right)+\frac{1}{4(N+1)^2f_\mathrm{r}}\left(\frac{4N^2}{\pi}+\frac{8}{3\pi}+3N^2+4\right)}, \tag{43}$$

$$A = \frac{R_o(k_v-1)}{2L_\mathrm{m}f_\mathrm{s}k_v(k_v+N)}, \tag{44}$$

$$I_{\mathrm{T1(RMS,\,CCM)}} = I_\mathrm{o}\sqrt{(k_v-1)\left(\frac{A^2}{3(N+k_v)}+N+k_v\right)}, \tag{45}$$

$$I_{\mathrm{T2(RMS,\,CCM)}} = I_\mathrm{o}\left(A+N+k_v\right)\sqrt{\frac{f_\mathrm{s}}{f_\mathrm{r}}\left(\frac{1}{2\pi}+\frac{3}{8}\right)}, \tag{46}$$

$$I_{\mathrm{T1(RMS,\,DCM)}} = \frac{I_\mathrm{o}}{\sqrt{3}}\sqrt[4]{\frac{8R_o(k_v-1)^3}{L_\mathrm{m}f_\mathrm{s}k_v}}, \tag{47}$$

$$I_{\mathrm{T2(RMS,\,DCM)}} = \frac{I_o}{2}\sqrt{\frac{R_o(k_v-1)(3\pi+4)}{\pi L_\mathrm{m}f_\mathrm{r}k_v}}. \tag{48}$$

7. Laboratory model design and experimental results

The converter was subject to experimental tests. The ultimate goal of the design laboratory model is to achieve high efficiency and high-power density while reaching the voltage conversion ratio requirement for all load conditions. Equation (23)was used to calculate the turns ratio N to achieve the required voltage conversion ratio of approximately 7.6 at the duty ratio $D = 0.6$. Another important parameter is magnetizing inductance because of the ripple of the current effects on turn-off conditions of the transistor T_2. Using the simplified current waveform in Fig. 5, the current ripple in the magnetizing inductance and the maximum input current value for data $V_\mathrm{in} = 50$ V, $k_v = 7.6$, $\eta = 0.9$, $f_\mathrm{s} = 100$ kHz, $I_\mathrm{o} = V_\mathrm{o}/R_{\mathrm{o(min)}}$, $R_{\mathrm{o(min)}} = 480\ \Omega$ were calculated based on Eq. (23) as follows:

$$\frac{\Delta I_\mathrm{Lm}}{2} = \frac{V_\mathrm{in}DT_s}{2L_\mathrm{m}} = \frac{V_\mathrm{in}\left(k_\upsilon/\eta-1\right)}{2L_\mathrm{m}\left(N+k_\upsilon/\eta\right)f_\mathrm{s}} = 5.5\ \mathrm{A}, \tag{49}$$

$$I_{\mathrm{in(max)}} = I_\mathrm{in}+\frac{\Delta I_\mathrm{Lm}}{2} = I_\mathrm{o}\left(N+\frac{k_\upsilon}{\eta}\right)+\frac{\Delta I_\mathrm{Lm}}{2} = 15.4\ \mathrm{A}. \tag{50}$$

The parameters of the resonant circuit were calculated based on Eq. (30) for the maximum output power $P_\mathrm{o} = 300$ W, the maximum transistor switching frequency $f_\mathrm{s} = 100$ kHz and input voltage $V_\mathrm{in} = 50$ V. In the laboratory model the resonant inductor was placed in series with the secondary winding of the tapped inductor and with leakage inductance forms equivalent inductance. The maximum voltages of switches were calculated using Eqs. (37–39). The specifications and parameters of the converter are provided in Table 1.

Table 1
List of power components and parameters of the laboratory model of the converter

Description	Values
Input voltage V_in	(30–50) V
Output voltage V_o	380 V
Switching frequency f_s	(25–100) kHz
Maximum output power P_o	300 W
Transistor T_1	IRFB4332 (250 V/29 mΩ)
Transistor T_2	IRFB4228 (150 V/12 mΩ)
Diode D	C4D05120A (1.4 V/1.2 kV)
Resonant inductance L_r	38 µH (core MS-130026)
Resonant capacity C_r	37.6 nF (ceramic COG)
Equivalent inductance L_eq	2.3 µH
Resonant frequency f_r	515 kHz
Magnetizing inductance L_m	27 µH (core MS-432115)
Coupling coefficient k	0.97
Turns ratio $N = n_2/n_1$	53/13

The Arnold Magnetic cores were used to build tapped (MS-432115) and resonant (MS-130026) inductors. The laboratory model with power density 1.06 kW/dm^3 and dimensions 93×66×46 mm of the proposed converter is shown in Fig. 8.

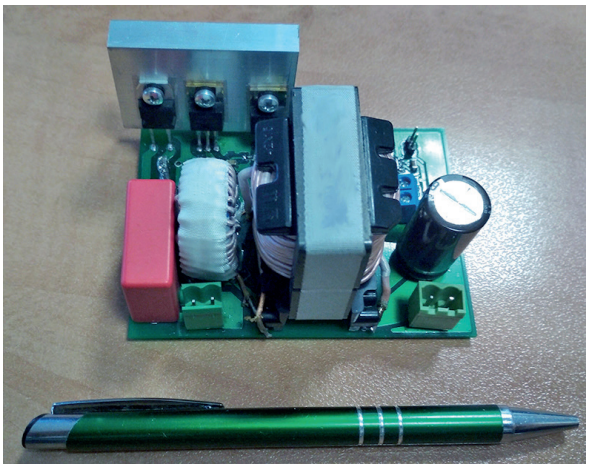

Fig. 8. Laboratory model of the proposed converter

The efficiency of the converter was measured by the digital multimeter Brymen 857s, and the waveforms were measured by the digital oscilloscope Tektronix DPO5034. Tests were carried out in open loop system; transistors were switched by Cyclon II FPGA module. Figures 9–14 show experimental waveforms of the converter laboratory model for the input voltage $V_{in} = 40$ V and the output voltage $V_o = 380$ V. For the duty cycle $D \approx 0.6$, the voltage and current waveforms are shown in Figs. 9, 10 at

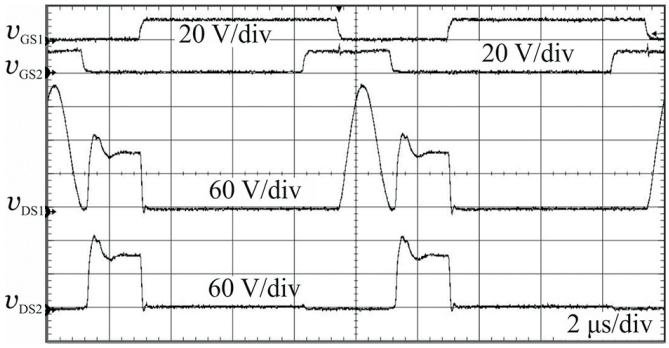

Fig. 9. Transistors voltages V_{GS1}, V_{GS2}, V_{DS1} and V_{DS2} ($P_o = 300$ W, $f_s = 100$ kHz, $R_o = 480\ \Omega$, $V_{DS1(max)} = 215$ V, $V_{DS2(max)} = 125$ V)

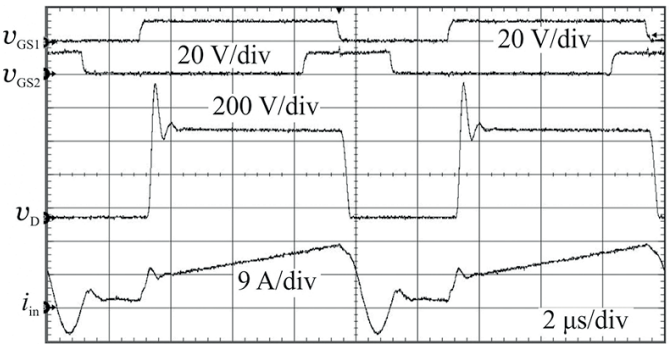

Fig. 10. Transistors voltages V_{GS1} and V_{GS2}, diode voltage V_D and input current i_{in} ($P_o = 300$ W, $f_s = 100$ kHz, $R_o = 480\ \Omega$, $V_{D(max)} = 800$ V, $i_{in(max)} = 16.8$ A)

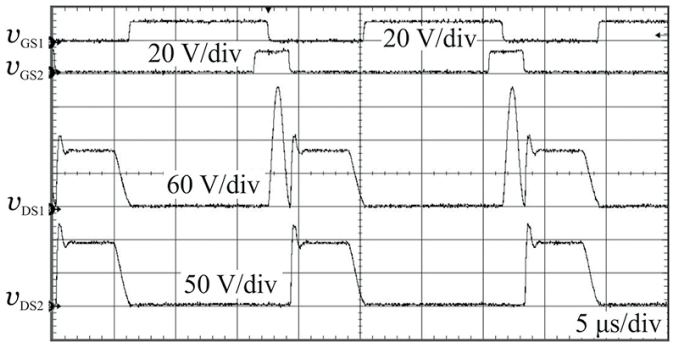

Fig. 11. Transistors voltages V_{GS1}, V_{GS2}, V_{DS1} and V_{DS2} ($P_o = 183$ W, $f_s = 52$ kHz, $R_o = 790\ \Omega$, $V_{DS1(max)} = 215$ V, $V_{DS2(max)} = 120$ V)

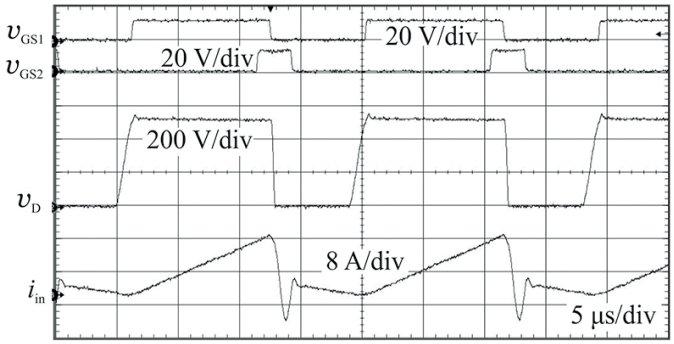

Fig. 12. Transistors voltages V_{GS1} and V_{GS2}, diode voltage V_D and input current i_{in} ($P_o = 183$ W, $f_s = 52$ kHz, $R_o = 790\ \Omega$, $V_{D(max)} = 520$ V, $i_{in(max)} = 16$ A)

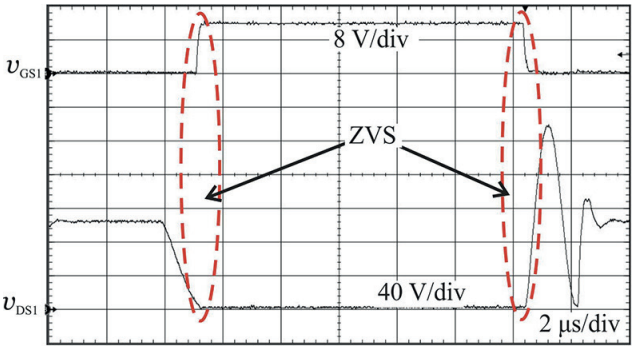

Fig. 13. Transistor T_1 voltages V_{GS1} and V_{DS1} during turn-on and turn-off at zero voltage

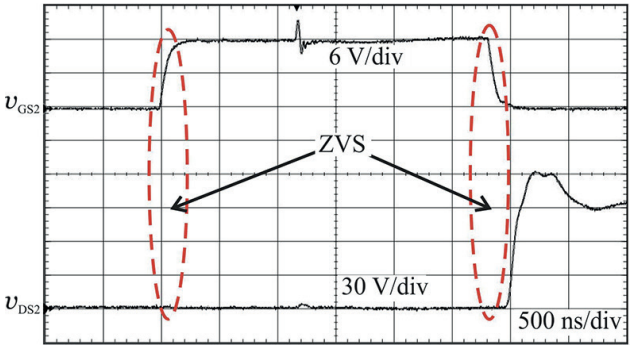

Fig. 14. Transistor T_2 voltages V_{GS2} and voltage V_{DS2} during turn-on and turn-off at zero voltage

maximum output power $P_o = 300$ W, and in Figs. 11, 12 at the output power 183 W, at which the converter works in DCM. When the transistor T_2 is turned off, there appears resonance between the equivalent inductance and the resonant capacitor (Figs. 9–11).

Figures 13, 14 illustrate the soft switching of the transistors T_1 and T_2. Both transistors are turned on and off at zero voltage. To provide ZVS, the transistors must be turned off before changing the direction of the flowing current. In the case when the transistors are turned off, the current starts to flow through their forward biased body diodes.

To suppress spikes on transistors V_{DS} voltages after turn-off transistor T_2 and diode V_D voltage after turn-on transistor T_1, parallel with those components were connected RC snubber circuits ($C_{SNUB(T1)} = 2.2$ nF, $R_{SNUB(T1)} = 47\ \Omega$, $C_{SNUB(D)} = 47$ pF, $R_{SNUB(D)} = 1$ kΩ).

Figure 15 shows a switching frequency comparison of the experiment with theory. Theoretical curves were determined for Table 1 data in accordance with Eqs. (29) and (36). The curves obtained experimentally are similar to theoretical ones. The differences occur at high output power and high voltage gain. They result from the non-constant current in magnetizing inductance in interval $t_3 - t_6$ (in theoretical derivations was assumed constant current in this interval) and the power losses in the converter.

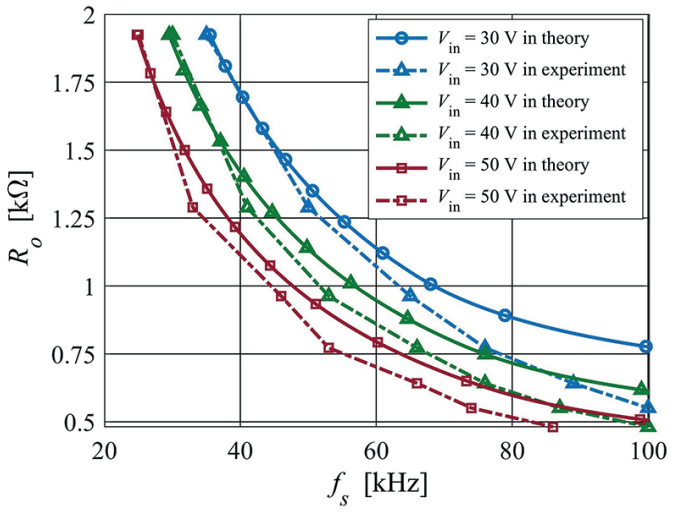

Fig. 15. Switching frequency comparison of experiment with theory

Figure 16 shows a comparison of the measured and theoretical efficiency of the proposed converter for the output voltage 380 V and the input voltages 30, 40, 50 V. The output load changed at a constant output voltage, thereby changing the output power, switching frequency and duty ratio while maintaining the same output voltage.

The theoretical efficiency was calculated according to the following equations:

$$\eta = \frac{P_{out} \cdot 100\%}{P_{out} + P_{loss}}, \tag{51}$$

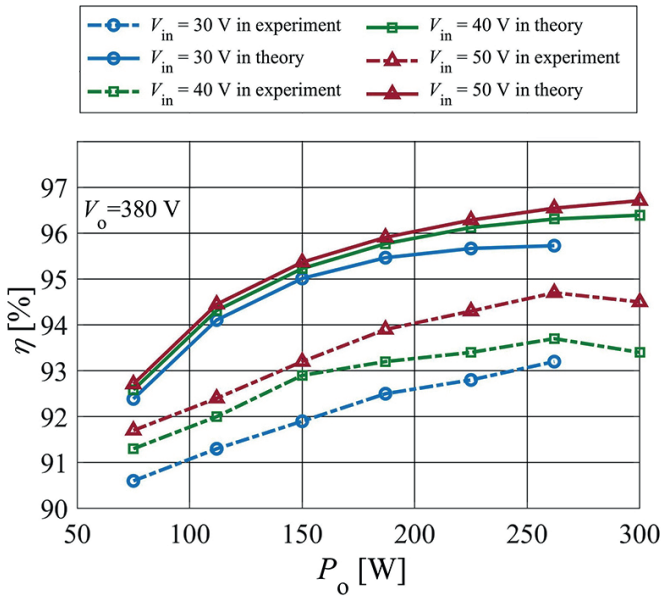

Fig. 16. Measured and theoretical converter efficiency as a function of the output power

$$P_{loss} = P_{T1} + P_{T2} + P_D + P_{WIRE(T)} + P_{WIRE(R)} + P_{CORE(T)} + P_{CORE(R)} + P_{SNUB}, \tag{52}$$

where P_{loss} is calculated power losses; P_{T1}, P_{T2}, P_D are conduction losses in transistors and diode; $P_{WIRE(T)}$, $P_{WIRE(R)}$ are conduction losses in wires of tapped and resonant inductors; $P_{CORE(T)} = 3$ W and $P_{CORE(R)} = 1.5$ W are estimated power losses in cores of tapped and resonant inductors; P_{SNUB} are power losses in snubbers.

The theoretical conduction losses in semiconductors and power losses in snubbers are given by:

$$P_{T1} = I_{T1(RMS)}{}^2 R_{DS1(on)}, \tag{53}$$

$$P_{T2} = I_{T2(RMS)}{}^2 R_{DS2(on)}, \tag{54}$$

$$P_D = I_{D(RMS)}{}^2 R_D + I_o V_{TO}, \tag{55}$$

$$P_{WIRE(T)} = I_{in(RMS)}{}^2 R_{PW} + I_{D(RMS)}{}^2 R_{SW}, \tag{56}$$

$$P_{WIRE(R)} = I_{D(RMS)}{}^2 R_{Lr}, \tag{57}$$

$$P_{SNUB} = f_s \left(C_{SNUB(T2)} V_{DS2(max)}{}^2 + C_{SNUB(D)} V_{D(max)}{}^2 \right) / 2, \tag{58}$$

where $R_{DS1(on)} = 29$ mΩ, $R_{DS2(on)} = 12$ mΩ are drain-source on resistances of switches T_1, T_2; $V_{TO} = 0.93$ V is the threshold voltage of diode D; $R_D = 101$ mΩ is the series resistance of diode D; $R_{PW} = 12$ mΩ and $R_{SW} = 150$ mΩ are primary and secondary windings resistances; $R_{Lr} = 50$ mΩ is resonant inductor resistance.

At low output power, efficiency is lower and increases with the load. The decrease in efficiency at low power levels is due to losses in inductors cores. Deformed currents in DCM increase its RMS values (Eqs. (40–48)) which causes the share of conduction losses in the total power losses at low power to remain high. For example, the calculated conduction losses for $P_o = 300$ W and $V_{in} = 40$ V in semiconductors power components and inductors wires are 5.5 W (1.8% of output power), for $P_o = 75$ W and $V_{in} = 40$ V are 1.1 W (1.5% of output power). The highest efficiency $\eta = 94.7\%$ was obtained with the output power $P_o = 260$ W and the input voltage $V_{in} = 50$ V. The lowest efficiency 90.7% was obtained for the input voltage $V_{in} = 30$ V and the output power $P_o = 75$ W. Reducing the input voltage (increasing the voltage transformation ratio) while maintaining a constant voltage at the output reduces the efficiency of energy conversion.

8. Performance comparison

Figure 17 shows the comparison of the theoretical voltage conversion ratio between the proposed converter and other converters. The proposed converter uses a soft switching technique similar to the basic ZVS QR boost converter with a tapped inductor [8, 15]. However, in [8] the maximum voltage on the main transistor and the voltage conversion ratio are high and depend on the output resistance R_o and the characteristic impedance Z. Furthermore, the transistor is soft switched only in a narrow power range. In the proposed converter, by using an additional transistor connected in series with the resonant capacitor, the main transistor is soft switching in a wide output power range; the maximum voltage on the main transistor is lower and the voltage conversion ratio is higher.

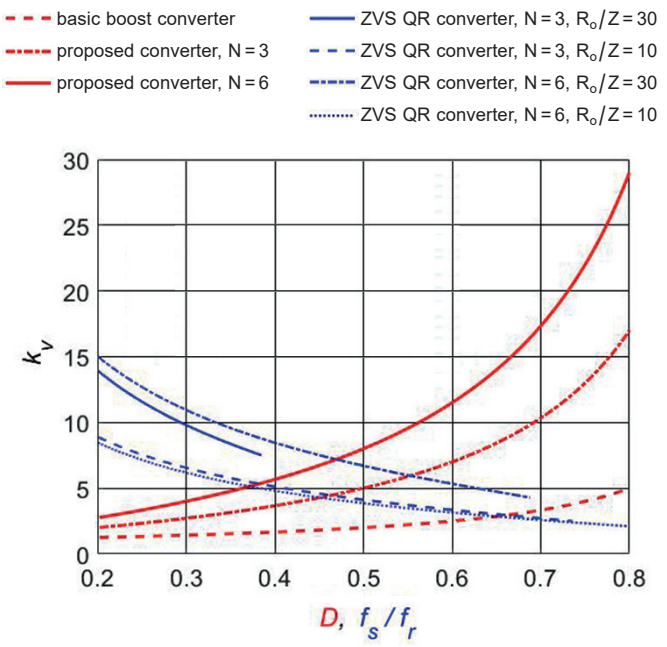

Fig. 17. Comparison of the proposed converter, basic boost converter and [8] converters with regard to voltage conversion ratio

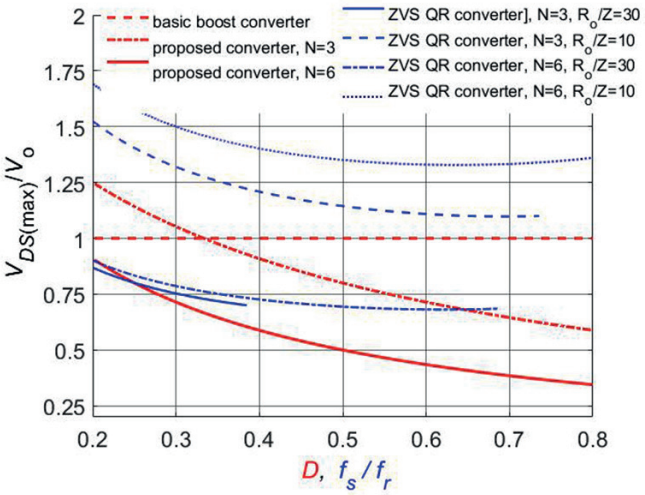

Fig. 18. Comparison of the proposed converter, basic boost converter and [8] converters with regard to transistor voltage stress

Figure 18 shows the comparison of the theoretical main switch voltage stress between the proposed converter and other converters.

Table 2 shows a comparison of performance parameters between the proposed converter, basic boost converter and ZVS quasi-resonant boost converter with a tapped inductor [8]. In the proposed converter relative frequency (f_s/f_r) may be much lower than [8], which ensures much lower conduction losses. Furthermore, in the proposed converter the voltage conversion

Table 2
Performance comparison

Converter	Basic boost converter	Converter in [8]	Proposed converter
Active switches	1	1	2
Diodes	1	1	1
Voltage conversion ratio	$\frac{1}{1-D}$	$f\left(\frac{Q, n,}{f_s/f_r}\right)$	$\frac{ND+1}{1-D}$*
Voltage stress of main active switch	V_{out}	$f\left(\frac{Q, n,}{f_s/f_r}\right)$	$\frac{2V_{in}}{1-D}$
Voltage stress of output diode	V_{out}	$f\left(\frac{Q, n,}{f_s/f_r}\right)$	$V_{out} + nV_{in}$
Reverse recovery problem	serious	small	small
Conduction losses	medium	large	small
Turn-on condition of main active switch	hard	ZVS	ZCS*, ZVS**
Turn-off condition of main active switch	hard	ZVS	ZVS

*CCM, **DCM

ratio and the voltage stress on power semiconductors do not depend on the parameters of the resonant circuit and the output resistance.

9. Conclusion

This paper presents a discussion of a novel cost-effective quasi-resonant boost converter with a tapped inductor. This converter combines zero voltage quasi-resonant techniques and different conduction modes with the possibility to obtain a high voltage conversion ratio. This results in high converter efficiency and the soft switching of transistors in the whole output power range. Simultaneously, it is built using a small number of power components and the tapped inductor with a small number of turns.

This topology utilizes the tapped inductor, reduces voltage stress on switches and increases the voltage conversion ratio. However, there exist voltage overshoots caused by leakage inductance in the practical circuit. It induces additional voltage stresses and necessitates the use of switches with higher blocking voltage, leading to more losses and reduced efficiency. The proposed converter effectively uses leakage inductance by making it part of the quasi-resonant circuit. As a result, leakage inductance is no longer a problem, and it actually helps to provide zero-voltage and zero-current switching.

The examined and described non-isolated DC/DC converter can operate at a high voltage conversion ratio in such a manner as transformer-isolated converters, without the necessity to work at extreme values of the duty cycle.

The ZVS-AERC converter, in comparison to its counterparts with a transistor switched with fixed an on/off time, needs one additional transistor connected in series with the resonant capacitor to increase the resonant frequency with regard to the switching frequency and, consequently, to reduce the conduction losses. In the proposed converter, voltage rating of main transistor, size of resonant inductor and conduction losses in resonant capacitor are reduced, which is why these systems can achieve higher efficiency then in [8] at the significant output power.

The handling of very large input currents from low-input voltage sources remains a practical issue for high power applications.

Finally, it was definitely confirmed that the proposed converter has a simple structure, is low-cost and compact, and offers high efficiency and high frequency soft-switching at the expense of minimum circuit components.

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