Calibration of a Mixed-Signal Power Network Transient Stability Analysis Emulator

Guillaume Lanz, Laurent Fabre, Georgios Lilis, Theodoros Kyriakidis,
Denis Sallin, Rachid Cherkaoui, and Maher Kayal

***Abstract*—The emerging field of power system emulation for real time smart grid management is very demanding in terms of speed and accuracy. This paper provides detailed information about the electronics calibration process of a high-speed power network emulator dedicated to the transient stability analysis of power systems. This emulator uses mixed-signal hardware to model the dynamic behavior of a power network. Special design allows the self-calibration of the analog electronics through successive measurements and correction steps. The calibration operation guarantees high resolution of the transient stability analysis results, so that they can be reliably used for operational planning and control on real power networks.**

***Index Terms*—Analog computer; calibration; FPGA; mixed-signal; power system dynamics**

I. Introduction

NOWADAYS, power networks work increasingly closer to their operational limits, due to constantly increasing power demand and due to the replacement of conventional energy sources by the so called "green" energy ones. The latter are of smaller inertia and thus, decrease the robustness of the power systems and therefore, their stability. A lot of effort has been put in the field of power system dynamic analysis. Recent research has demonstrated the computation speed benefits of analog solutions for solving the Kirchhoff grid equations [1-3].

The mixed-signal solver presented in this paper, studies the transient stability analysis (TSA) of power systems. It deals with the ability of the power production units to keep their synchronism with the rest of the network. It involves large angle excursions of synchronous machines, due to anomalies that appear in the network.

The major challenge that needs to be addressed when developing such a tool is its computation speed. In fact, the grid modeling requires a large matrix equation operation, which slows down conventional digital solvers considerably. Therefore, the platform developed in this project uses dedicated analog hardware that allows the emulation of the power grid.

The analog side of the mixed-signal platform is based on programmable resistances that represent the impedance of the transmission power network lines. The relative precision of these resistances is in the range of 20%. Analog to digital (ADC) and digital to analog (DAC) converters are the interface between the digital and the analog parts of the platform. These components also suffer from imprecision. In order to reach an acceptable resolution for TSA use, the above mentioned analog components of the mixed mode solver need to be calibrated.

This paper is organized as follows. Short description of the mixed-signal platform is presented in section II. Section III covers the calibration hardware. Section IV describes the test benches used to calibrate the analog components. Section V contains a description of the hardware implementation of the emulator. Section VI compares TSA results on a sample power system case, considering the influence of the calibration process on this solver.

G. Lanz, L. Fabre, G. Lilis, T. Kyriakidis, D. Sallin, R. Cherkaoui and M. Kayal are with Electronics Laboratory & Power Systems Group, École Polytechnique Fédérale de Lausanne, Switzerland (e-mail: guillaume.lanz@epfl.ch)

II. Mixed-Signal Solver

The top part of fig. 1 shows a synoptic view of the modeling of power systems. It consists of an interconnected grid to which components such as generators and loads are connected. Conventional power network simulators use the representation given in the bottom part of fig. 1. In the proposed platform, the grid is computed by the means of an analog programmable impedance network representing this matrix; equations of the other components (loads, generators, etc.) are solved in parallel digitally using an FPGA implementation.

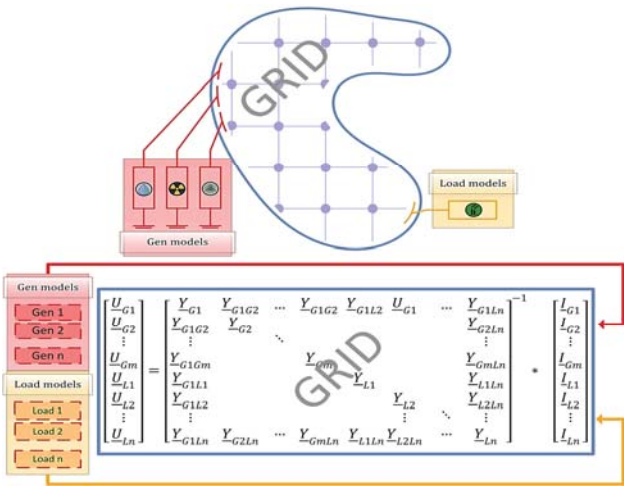

Figure 1. Power network simulator representation

Therefore, the realized emulator uses analog and digital electronics to represent the power networks dynamic behavior. The analog electronics allows a large computation time reduction with respect to the fully digital implementation. However, due to the finite precision of the analog components, a calibration process becomes mandatory.

A. Analog Grid Model

The concept of the *grid emulation* uses analog resistive networks to represent the power grid. This modeling uses the phasor representation of power system quantities [1-2]. The system allows solving the current injection equation almost instantaneously. It avoids the solution of the time consuming linear system that links voltages (U) to current injections (I) at each node of an *n x n* size power network through the admittance matrix (Y) in conventional power network simulators.

$$[\underline{I}_i]_{(i=1\ldots n)} = [\underline{Y}_{ij}]_{(i=1\ldots n)*(j=1\ldots n)} * [\underline{U}_j]_{(j=1\ldots n)} \quad (1)$$

B. Digital Component Model

This part of the mixed-signal platform solves the equations of different power system components (generators and loads). The required computations are less critical in terms of speed compared to the grid equations described above, because equations for each element can be computed independently. An FPGA is used to model these grid elements. The use of a pipelined architecture allows the tradeoff between speed and resources usage [1].

C. Overall System

The overall mixed-signal architecture is shown in fig. 2. It allows fast transient stability analysis on power systems with respect to conventional digital simulators. Analog to digital and digital to analog converters are the interface between the digital and analog circuits.

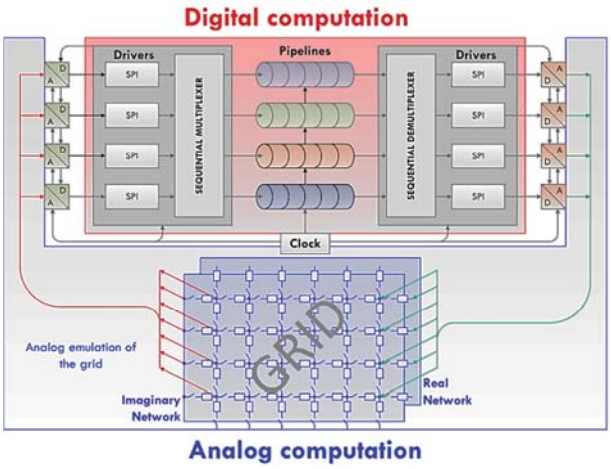

Figure 2. Mixed-signal emulator architecture

The platform emulates the dynamic phenomena by numerical integration. A typical iteration consists of a grid voltage measurement by the ADCs, a digital computation which mimics the behavior of network components, a current injection feedback through the DACs, and the analog grid settling down to its new quiescent state.

The hardware implementation of this solver is presented in section V.

III. Calibration Circuit

One of the 2 analog circuits[1] used to represent 1 node of the power network is shown in fig. 3. It consists of the analog representation (in blue in fig.3) of the macroscopic network and of the circuit used to inject current at each node (in green in fig.3). All the mismatch issues considered in the calibration process are highlighted in red in fig.3.

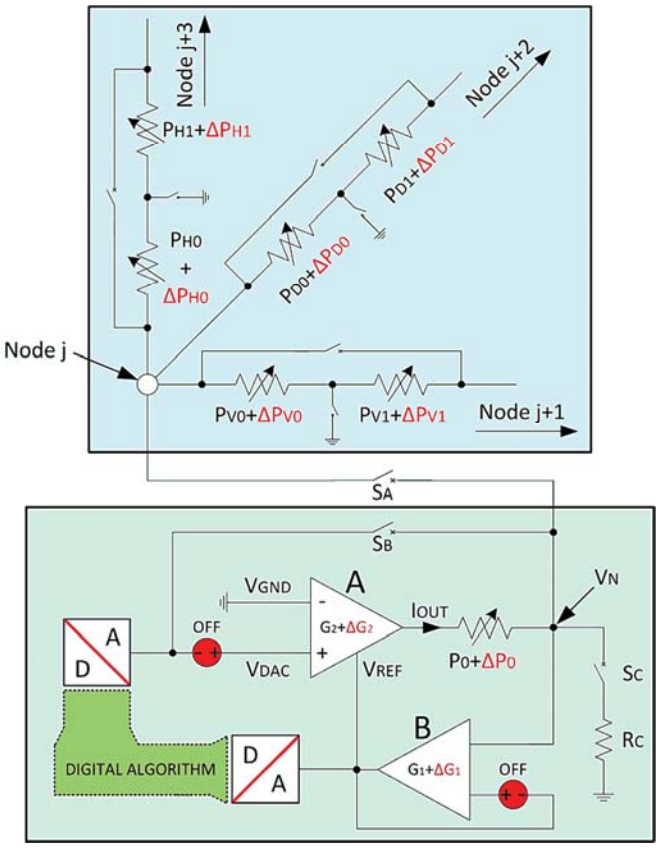

Figure 3. Analog representation of 1 node and dedicated driving circuit

In its standard use, this circuit operates as follows. The digital part of the platform receives node voltage measurements through the ADCs and outputs current injection feedbacks through the DACs, depending on the component that is modeled. The voltage is measured through an operational amplifier (B) connected as voltage follower that drives the input of the ADC. The output voltage of the DAC is converted to a current injection by the use of an instrumentation amplifier (A) connected in series with a programmable conversion potentiometer (P_0). The equations of this closed loop amplifier are the following:

[1] The phasor approach uses 2 identical and independent hardware circuits to represent the real and imaginary part of the network.

$$V_{out} = G * (V_{in+} - V_{in-}) + V_{REF} \quad (2)$$

$$V_{REF} = V_{out} - I_{out} * P_0. \quad (3)$$

G is the variable gain of the amplifier that is fixed to 1 and V_{in-} is directly connected to the ground, so that:

$$I_{out} = (V_{in+} - V_{GND})/P_0. \quad (4)$$

In order to calibrate this circuit, additional switches allow the isolation of the various different analog components. It was found that the resistance of these switches is in the range of 2-3Ω, that is orders of magnitude lower than the resistance of other relevant components. Therefore, the resistance of these switches is neglected in this process.

IV. Calibration Test-Benches

A. Calibration Strategy

The calibration that is required in this application addresses static gain and offset correction [5]. Because all components suffer from such errors, the calibration considers a perfect static gain for the ADC. All other components are calibrated using measurements done by this module. The results described below are obtained by an average over multiple voltage measurements to reduce the global noise influence. The integral and differential non-linearity is assumed to be low. Thus, a least square linearization is done on measurements in order to correct their output behavior.

Fig. 4 describes the different steps of a component output characteristic calibration. These correction steps are used for all the calibration processes described below.

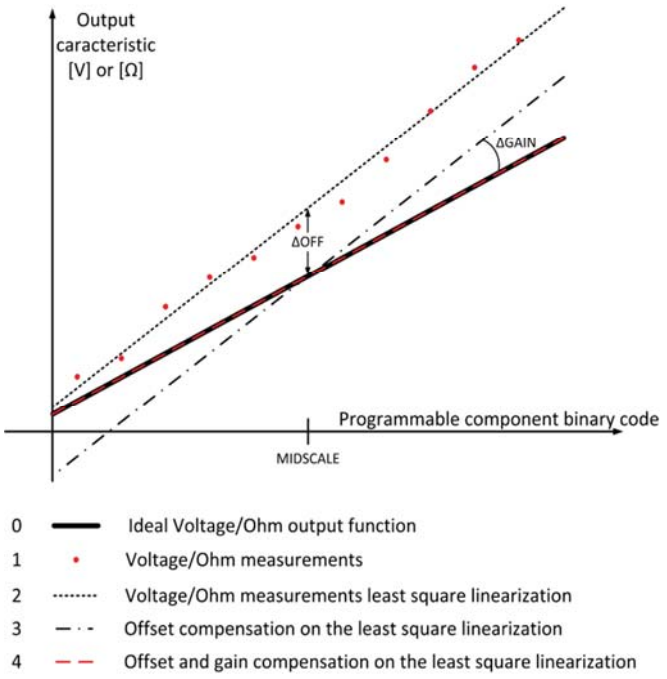

Figure 4. Analog components calibration sequence

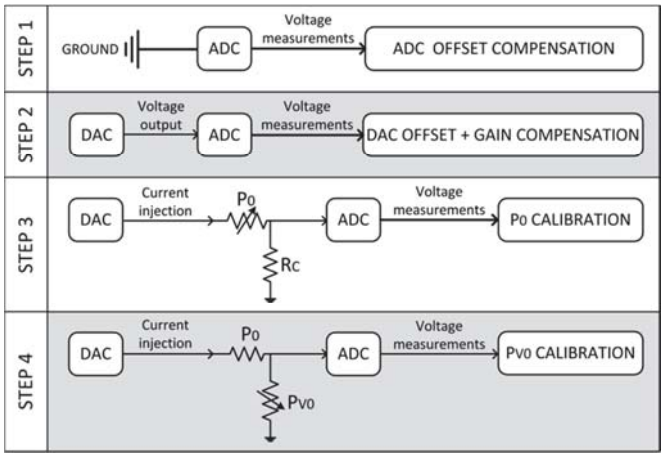

Figure 5. Power network emulator calibration steps

B. Calibration Process

Fig. 5 summarizes the different steps of the power network emulator calibration.

1) ADC stage static offset compensation

This test allows an offset compensation via a ground measurement. The ground is fixed by a 16-bit reference DAC which is calibrated using local measurements.

This step is an open loop test bench that connects the ground to the ADC input using the S_C switch and the operational amplifier (B). All other switches are opened and P_0 is not connected. This step rectifies the offset of the pair composed by the B amplifier and the converter.

2) DAC static gain and offset correction

This test aims to compensate the static gain and the offset of the digital to analog converter. It's a closed loop test for which switch S_B is closed while all others are open. P_0 is not connected. A voltage ramp is output by the DAC and is measured via the calibrated ADC stage. The result measurements are processed by a least square linearization to match the nature of the ideal corrected behavior. The offset is extracted at the middle of the full range of the converter. The slope ratio between the ideal output function and the least square measured one allows finding the gain correction factor.

3) Conversion Resistor Calibration

The trimming of the programmable potentiometer P_0 is a key operation, since the result of this analysis will be used for all the grid resistors corrections. Therefore, an accurate voltage divider circuit is built using a constant resistor R_C. This resistor is of 1‰ exactitude. For this analysis, the S_C switch is closed while all others are opened. P_0 is obviously connected. The DAC output fixes the circuit current injection. The voltage measurement provided by the ADC allows the extraction of the P_0 value according to (5) and (6).

$$I = \frac{V_{DAC} - V_{GND}}{P_0} = \frac{V_N - V_{GND}}{R_C} \quad (5)$$

$$\Rightarrow P_0 = \frac{V_{DAC} - V_{GND}}{V_N - V_{GND}} * R_C \quad (6)$$

The effectiveness of this calibration operation can be illustrated by comparing compensated P_0 values, with manual voltage measurements using a high resolution multimeter. Typical results of this calibration operation indicate a maximum residual relative error of less than 1%. The relative average error is in the order of 0.1%.

4) Grid Resistor Calibration

This test uses the same methodology as the P_0 calibration sequence. This time, P_0 is used as reference value and switch S_A is closed while S_B and S_C are opened. The tested resistor can be isolated in the grid by the use of the circuit shown in blue in fig.3. For example, during the calibration process of P_{V0}, all other resistors are disconnected, while the switch located between P_{V0} and P_{V1} is closed. All remaining switches are opened. The voltage divider that is obtained is exactly the opposite of the one used for the previous test, so that (5) and (6) become:

$$I = \frac{V_{DAC}-V_{GND}}{P_0} = \frac{V_N-V_{GND}}{P_{V0}} \quad (7)$$

$$\Rightarrow P_{V0} = \frac{V_N-V_{GND}}{V_{DAC}-V_{GND}} * P_0 \quad (8)$$

The residual relative error after calibration is increased with respect to the previous test, since this calibration operation uses measurements done for the P_0 calibration as reference. The residual maximum relative error is of less than 3%. The average relative error is of 0.5%.

V. Hardware Implementation

The power network emulator is built out of 4 printed circuit boards (PCB) that are stacked together in a 3D connection fashion. Each of these boards represents 24 nodes, so that the maximum topology size that can be represented is of 96 nodes [2]. Fig. 6 depicts one of these PCBs.

This figure represents the hardware implementation of the architecture presented in fig. 2. The digital and analog parts of the solver are highlighted in red and blue respectively. The converters are located all around the analog grid.

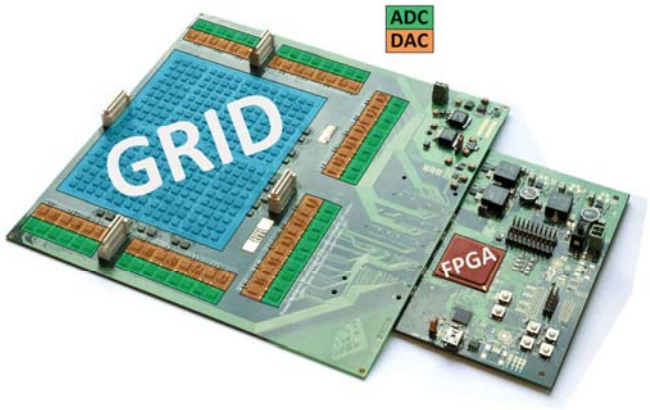

Figure 6. PCB slice of the power network emulator

The bottom slice of the emulator is considered as the master board while the 3 others are slaves. The master sends and receives state signals to and from the other boards, which allow the synchronization of all the computational units. This aspect is highly important, since the stabilization of the analog grid suffers a lot from current injections updates done asynchronously. It helps among others to increase the accuracy of the resulting voltage measurements, and therefore of the stability analysis of the power system.

This hardware platform is interfaced by dedicated software. It allows an easy access to all the power network emulator features. Thanks to this graphical user interface, all the pre- and post-transient stability analysis operations such as the calibration process described above, the mapping of the power network topology, the steady state solution determination, are fully automatized. A dedicated Cypress micro-controller is used to share data between the FPGA and the host computer. This micro-controller translates USB data into FPGA understandable information.

VI. Power Network Emulation Testcase

The use of the above mentioned calibration sequence can be illustrated by comparing transient stability analysis (TSA) results on a 57 bus topology (fig. 7). Inaccuracies in the potentiometer values lead to power flow variations in the power system. Because the angle of synchronous machines is related to this power flow, TSA study can be altered by this effect, when it analyses a system that undergoes disturbances. Indeed, the angle excursion with respect to the steady state value is used as information to determine the stability of the system.

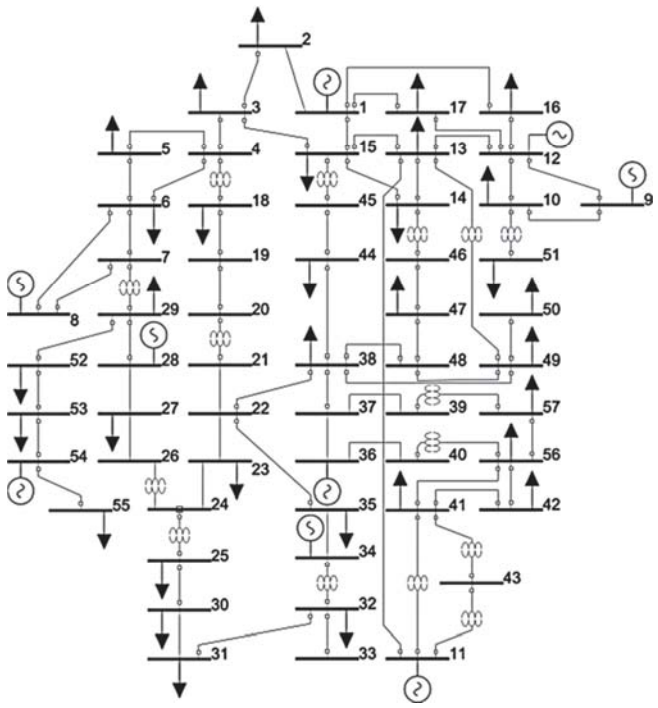

Figure 7. 57-bus IEEE test case power network

The scenario that is applied to the 57 bus power system is illustrated in fig. 8. A three phase short circuit connection appears in the middle of a branch connecting a generator to a load. This fault could be caused by a tree that would touch this transmission line. After 200ms, the fault is cleared and the transmission line remains connected. The topology comes back to its initial state. The energy mismatch during the fault forces the generators angles to move. If the mismatch is too high, the machine will lose it synchronism with the rest of the network and the system will not manage to recover to a steady state.

Angles results for two generators are shown in fig. 9. Three different generator angle results are provided. The first one is a conventional simulator analysis result (in red and yellow in fig.9) which considers the exact line impedance values. Thus, it has to be considered as reference. The second and third correspond to the emulator result obtained with (in green and purple in fig.9) and without (in blue and brown in fig.9) the calibration sequence respectively.

The difference between the results obtained with and without the calibration demonstrates the usefulness of the calibration process described in this document.

While conventional simulators require few seconds to run such an analysis (of 5 simulated seconds), the mixed-signal solver described in this paper performs the same study in few milliseconds. Therefore, it computes power system TSA 1000 times faster than real time. The computation time reduction is essentially due to the use of analog electronics that allow the modeling of the grid connections in a speed-optimized way.

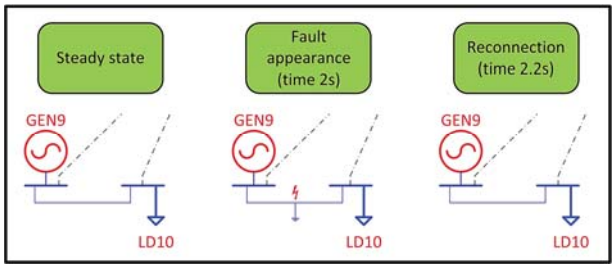

Figure 8. Emulation fault scenario

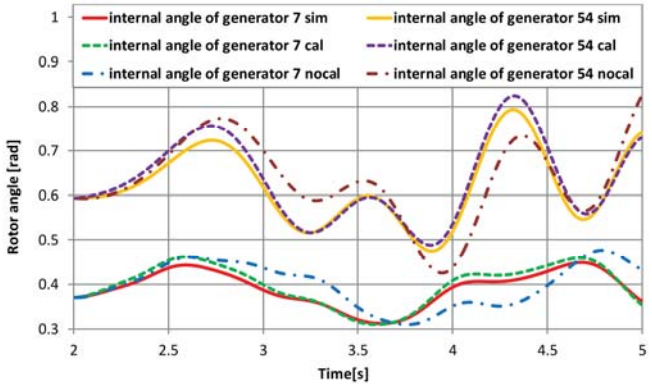

Figure 9. Internal angle of generators located at bus 7 and 54

VII. Conclusion

This paper presents the calibration process used to increase the accuracy of the transient stability analysis realized using a mixed-signal power network emulator. This tool determines the dynamic stability of an arbitrary power system that is subjected to severe disturbances. These perturbations are typically short circuit connections or loss of a transmission line.

The major advantage of such a platform is its computation speed. However the use of low precision analog electronic to emulate the network grid equations leads to large deviations in the angle results. These deviations may cause the power network emulator to misclassify unstable scenarios as stable. Therefore, a calibration procedure is required in order to provide accurate analyses which enable safe decision-making in power network operational planning and control.

The development of such a solver is inspired by the advent of the smart grids in addition to the trends for the use of decentralized green energy sources in power networks. This tendency forces the transmission system operators (TSOs) to find solutions to increase the security and the reliability in power systems, due to the fragile stability of these new types of power systems. This constraint can be met by the use of the high-speed power network transient stability analyzer described in this paper.

Typical TSA uses of this solver are multiple contingency analysis and critical clearing time analysis. Both of these studies give information about the overall reliability of a particular power network, and thus reduce the risk taken by the TSO.

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Guillaume Lanz received his B.Sc. and M.Sc. degree in Micro Engineering from the Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland, in 2008 and 2010. In 2010 he joined the Electronic Laboratory at EPFL, where he co-developed a mixed-signal high-speed power network emulator. His major contributions to this project are in the digital resource development and applications. He started a Ph.D. in microsystems and microelectronics in 2012. His research interests are in high-speed power network stability studies, fault detection, and loadflow analysis.

Laurent Fabre received a B.S. degree in Microengineering from the school of Business and engineering Vaud, Switzerland, in 2000. He worked for three years as an R&D engineer in blood separation tools for Biofluid Systems (Nyon, Switzerland). He received B.S. and M.S. degrees in electrical engineering from the Ecole Polytechnique Fédérale de Lausanne, Switzerland in 2005 and 2007 respectively. He is currently working towards a Ph.D. degree at the same institute. His research is related to high-speed mixed-signal power system emulation.

Georgios Lilis received his joint B.Sc. and M.Sc. diploma in Electrical and Computer Engineering from Aristotle University of Thessaloniki in 2012. He is pursuing his PhD degree in Electronics Laboratory, EPFL since 2013. His main research interests are: smart grid, smart building management and optimization, embedded system design and programming.

Theodoros Kyriakidis received his engineering Diploma in Electrical Engineering and Computer Science in 2010 from the Aristotle University of Thessaloniki. Theodoros is now a Research Assistant with the Electronics Laboratory at the Ecole Polytechnique Fédérale de Lausanne, where he is pursuing his PhDs in the cross-field between electronics, power systems and computer science. His research interests include non-conventional architectures for scientific computations, reconfigurable computing, intelligent systems, power system dynamics, and numerical analysis.

Denis Sallin received the B.Sc. degree in electrical engineering in 2009 and the M.Sc. degree in electronics and microelectronics in 2011, both from Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland. His diploma project was the design, manufacturing, and testing of a high speed mixed-signal printed circuit board for a power network emulator. Since 2012, he has been pursuing the Ph.D. degree in the field of photodetection at the Electronics Laboratory (Elab).

Rachid Cherkaoui (M'05-SM'07) received both M.Sc. and Ph.D. degrees in electrical engineering in 1983 and 1992, respectively, from Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland. Since 1992, he has been senior scientist at EPFL. His research and teaching interests are in electricity market deregulation, in distributed generation and storage and in power system vulnerability.

Maher Kayal received M.S. and Ph.D degrees in electrical engineering from the Ecole Polytechnique Fédérale de Lausanne (EPFL, Switzerland) in 1983 and 1989 respectively. He has been with the Electronics laboratories of the Ecole Polytechnique Fédérale de Lausanne (EPFL, Switzerland) since 1990, where he is currently a professor and director of the "Energy Management and Sustainability" section. He has published many scientific papers, coauthor of three text books dedicated to mixed-mode CMOS design and he holds seven patents. His technical contributions have been in the area of analog and Mixed-signal circuits design including highly linear and tunable sensors microsystems, signal processing and green energy management. M. Kayal is a recipient of the Swiss Ascom award in 1990 for the best work in telecommunication fields; He is Author and co-author of the following paper award in: ED&TC conference in 1997, IEEE-AQTR in 2006, Mixdes conference in 2007 & 2009, Power tech conference in 2009 and Poland Section IEEE ED Chapter special award in 2011. M. Kayal receive in 2009 the Swiss credit award for best teaching.